

N-CHANNEL 1500V - 5Ω - 4A TO-220/TO-220FP/TO-247 Very High Voltage PowerMESH™ MOSFET

PRODUCT PREVIEW

Table 1: General Features

TYPE	V _{DSS}	R _{DS(on)}	I _D	P _w
STF4N150	1500 V	< 7 Ω	4 A (*)	40 W
STP4N150	1500 V	< 7 Ω	4 A	160 W
STW4N150	1500 V	< 7 Ω	4 A	160 W

- TYPICAL R_{DS(on)} = 5 Ω
- AVALANCHE RUGGEDNESS
- GATE CHARGE MINIMIZED
- VERY LOW INTRINSIC CAPACITANCES
- HIGH SPEED SWITCHING

DESCRIPTION

Using the well consolidated high voltage MESH OVERLAY™ process, STMicroelectronics has designed an advanced family of Power MOSFETs with outstanding performances. The strengthened layout coupled with the Company's proprietary edge termination structure, gives the lowest RDS(on) per area, unrivalled gate charge and switching characteristics.

APPLICATIONS

- SWITCH MODE POWER SUPPLIES

Figure 1: Package

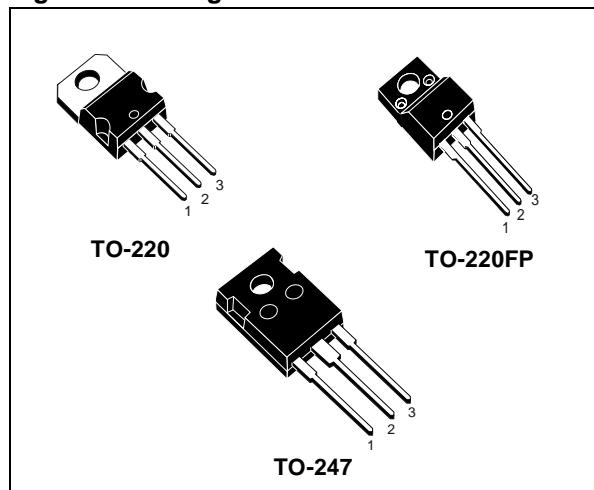


Figure 2: Internal Schematic Diagram

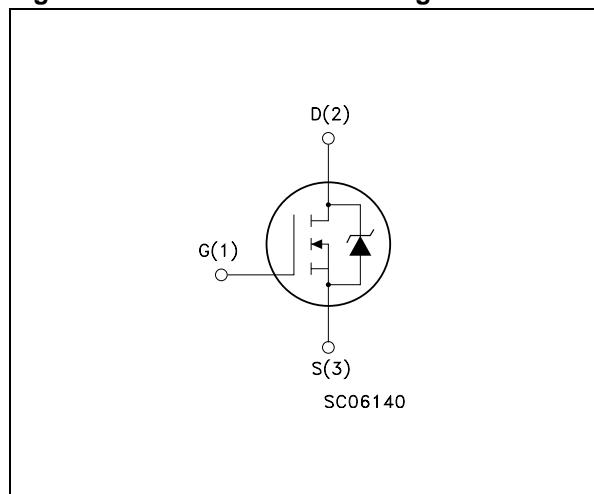


Table 2: Order Codes

SALES TYPE	MARKING	PACKAGE	PACKAGING
STF4N150	F4N150	TO-220FP	TUBE
STP4N150	P4N150	TO-220	TUBE
STW4N150	W4N150	TO-247	TUBE

Table 3: Absolute Maximum ratings

Symbol	Parameter	Value		Unit
		STP4N150 STW4N150	STF4N150	
V _{DS}	Drain-source Voltage ($V_{GS} = 0$)	1500		V
V _{DGR}	Drain-gate Voltage ($R_{GS} = 20 \text{ k}\Omega$)	1500		V
V _{GS}	Gate- source Voltage	± 30		V
I _D	Drain Current (continuous) at $T_C = 25^\circ\text{C}$	4	4 (*)	A
I _D	Drain Current (continuous) at $T_C = 100^\circ\text{C}$	2.5	2.5 (*)	A
I _{DM} (•)	Drain Current (pulsed)	12	12 (*)	A
P _{TOT}	Total Dissipation at $T_C = 25^\circ\text{C}$	160	40	W
	Derating Factor	1	0.24	W/°C
V _{ISO}	Insulation Withstand Voltage (DC)	-	2500	V
T _j T _{stg}	Operating Junction Temperature Storage Temperature	-55 to 150 -55 to 150		°C °C

(•) Pulse width limited by safe operating area

(*) Limited only by maximum temperature allowed

Table 4: Thermal Data

		TO-220	TO-220FP	TO-247	
R _{thj-case}	Thermal Resistance Junction-case Max	0.78	3.1	0.78	°C/W
R _{thj-amb}	Thermal Resistance Junction-ambient Max	62.5		50	°C/W

ELECTRICAL CHARACTERISTICS (T_{CASE} =25°C UNLESS OTHERWISE SPECIFIED)**Table 5: On /Off**

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V _{(BR)DSS}	Drain-source Breakdown Voltage	I _D = 1 mA, V _{GS} = 0	1500			V
I _{DSS}	Zero Gate Voltage Drain Current (V _{GS} = 0)	V _{DS} = Max Rating V _{DS} = Max Rating, T _C = 125°C			10 500	µA µA
I _{GSS}	Gate-body Leakage Current (V _{DS} = 0)	V _{GS} = ± 30 V			± 100	nA
V _{GS(th)}	Gate Threshold Voltage	V _{DS} = V _{GS} , I _D = 250 µA	3	4	5	V
R _{DS(on)}	Static Drain-source On Resistance	V _{GS} = 10 V, I _D = 2 A		5	7	Ω

ELECTRICAL CHARACTERISTICS (CONTINUED)

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Table 6: Dynamic

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
g_{fs} (1)	Forward Transconductance	$V_{DS} = 30 \text{ V}$, $I_D = 2 \text{ A}$		TBD		S
C_{iss} C_{oss} C_{rss}	Input Capacitance Output Capacitance Reverse Transfer Capacitance	$V_{DS} = 25 \text{ V}$, $f = 1 \text{ MHz}$, $V_{GS} = 0$		1300 120 12		pF pF pF
$t_{d(on)}$ t_r $t_{d(off)}$ t_f	Turn-on Delay Time Rise Time Turn-off-Delay Time Fall Time	$V_{DD} = 750 \text{ V}$, $I_D = 2 \text{ A}$, $R_G = 4.7 \Omega$, $V_{GS} = 10 \text{ V}$ (see Figure 4)		35 30 45 45		ns ns ns ns
Q_g Q_{gs} Q_{gd}	Total Gate Charge Gate-Source Charge Gate-Drain Charge	$V_{DD} = 600 \text{ V}$, $I_D = 4 \text{ A}$, $V_{GS} = 10 \text{ V}$ (see Figure 7)		30 10 9	50	nC nC nC

Table 7: Source Drain Diode

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_{SD} I_{SDM} (2)	Source-drain Current Source-drain Current (pulsed)				4 12	A A
V_{SD} (1)	Forward On Voltage	$I_{SD} = 4 \text{ A}$, $V_{GS} = 0$			2	V
t_{rr} Q_{rr} I_{RRM}	Reverse Recovery Time Reverse Recovery Charge Reverse Recovery Current	$I_{SD} = 4 \text{ A}$, $di/dt = 100 \text{ A}/\mu\text{s}$ $V_{DD} = 45V$ (see Figure 5)		510 3 12		ns μC A
t_{rr} Q_{rr} I_{RRM}	Reverse Recovery Time Reverse Recovery Charge Reverse Recovery Current	$I_{SD} = 4 \text{ A}$, $di/dt = 100 \text{ A}/\mu\text{s}$ $V_{DD} = 45V$, $T_j = 150^\circ\text{C}$ (see Figure 5)		650 4 12.6		ns μC A

(1) Pulsed: Pulse duration = 300 μs , duty cycle 1.5 %.

(2) Pulse width limited by safe operating area.

Figure 3: Unclamped Inductive Load Test Circuit

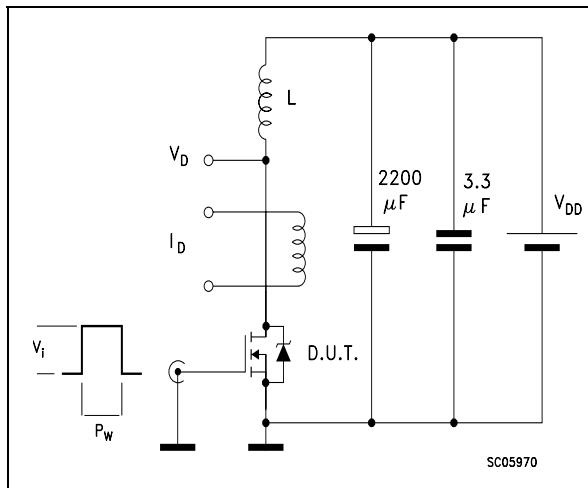


Figure 4: Switching Times Test Circuit For Resistive Load

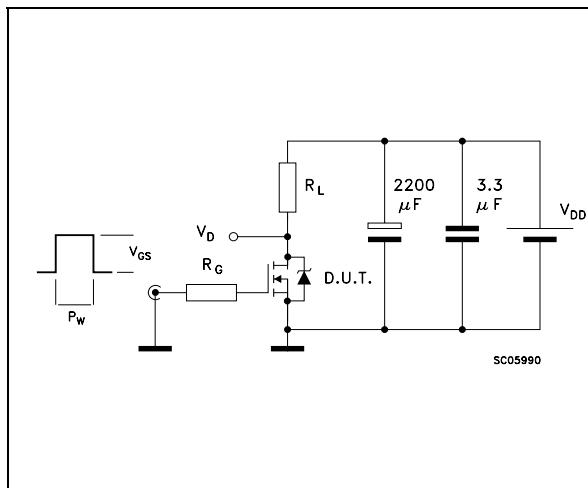


Figure 5: Test Circuit For Inductive Load Switching and Diode Recovery Times

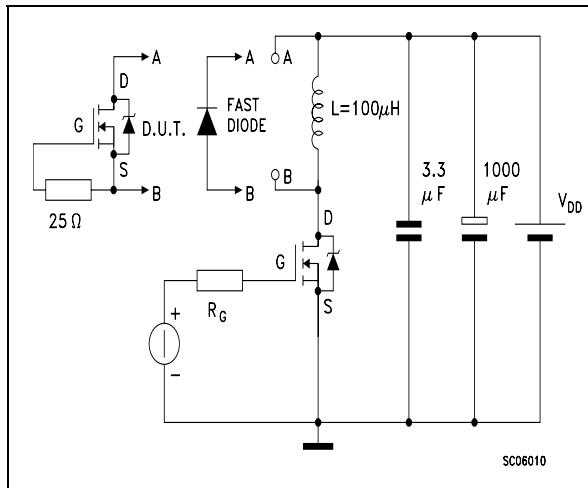


Figure 6: Unclamped Inductive Waveform

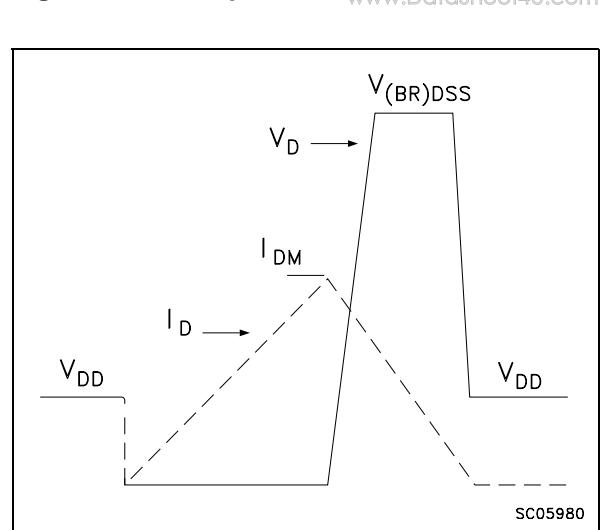
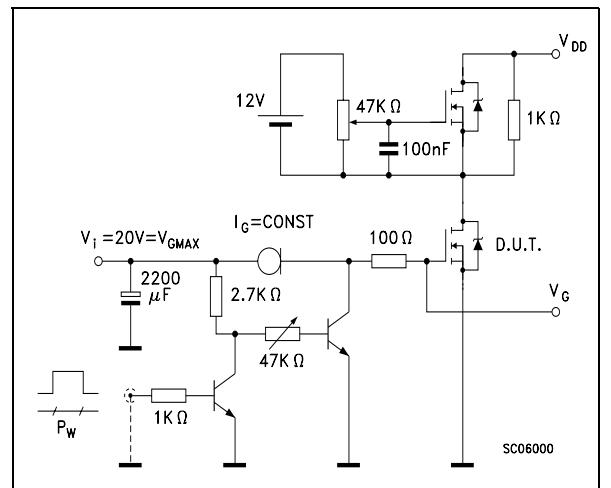
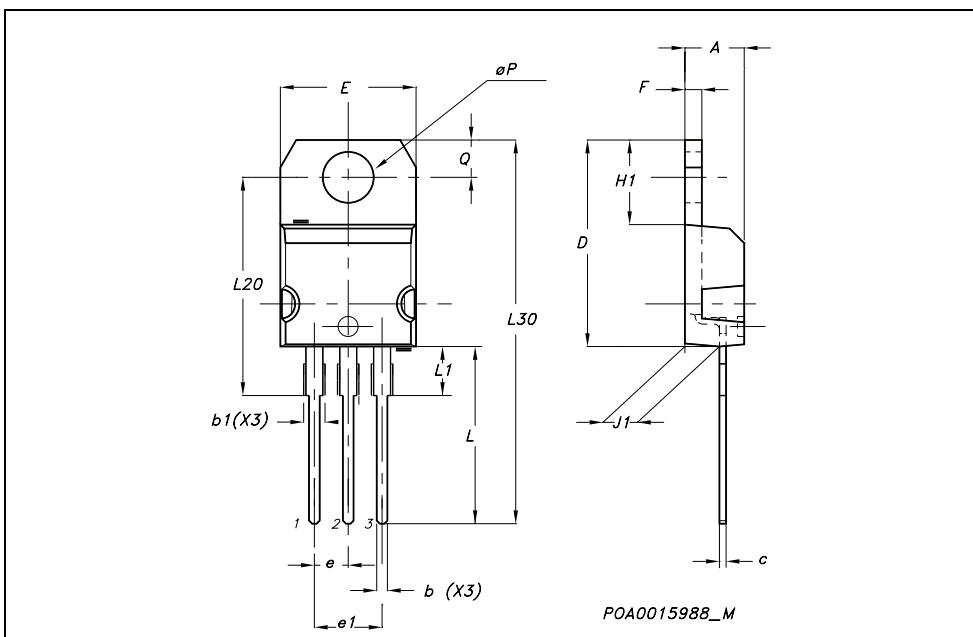


Figure 7: Gate Charge Test Circuit



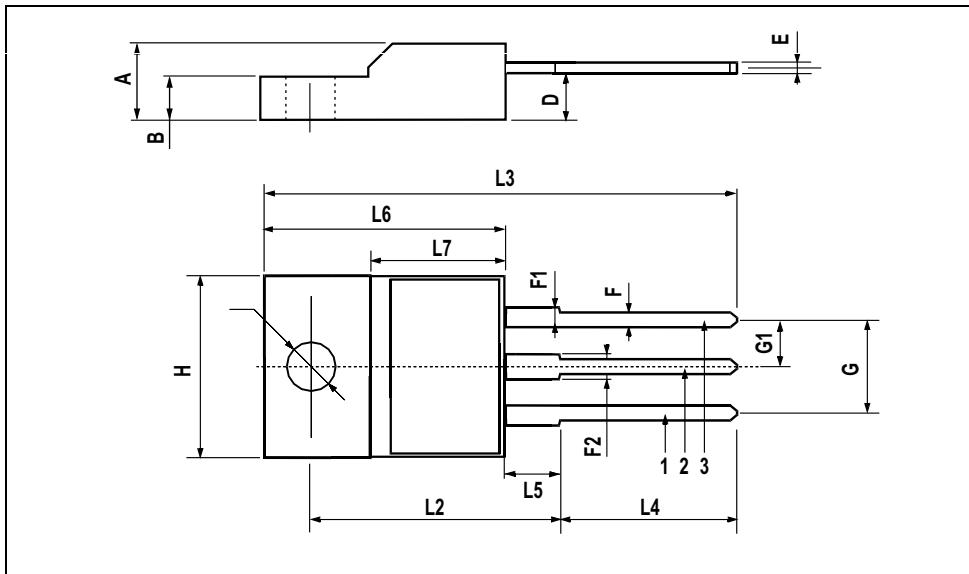
TO-220 MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	4.40		4.60	0.173		0.181
b	0.61		0.88	0.024		0.034
b1	1.15		1.70	0.045		0.066
c	0.49		0.70	0.019		0.027
D	15.25		15.75	0.60		0.620
E	10		10.40	0.393		0.409
e	2.40		2.70	0.094		0.106
e1	4.95		5.15	0.194		0.202
F	1.23		1.32	0.048		0.052
H1	6.20		6.60	0.244		0.256
J1	2.40		2.72	0.094		0.107
L	13		14	0.511		0.551
L1	3.50		3.93	0.137		0.154
L20		16.40			0.645	
L30		28.90			1.137	
ϕP	3.75		3.85	0.147		0.151
Q	2.65		2.95	0.104		0.116



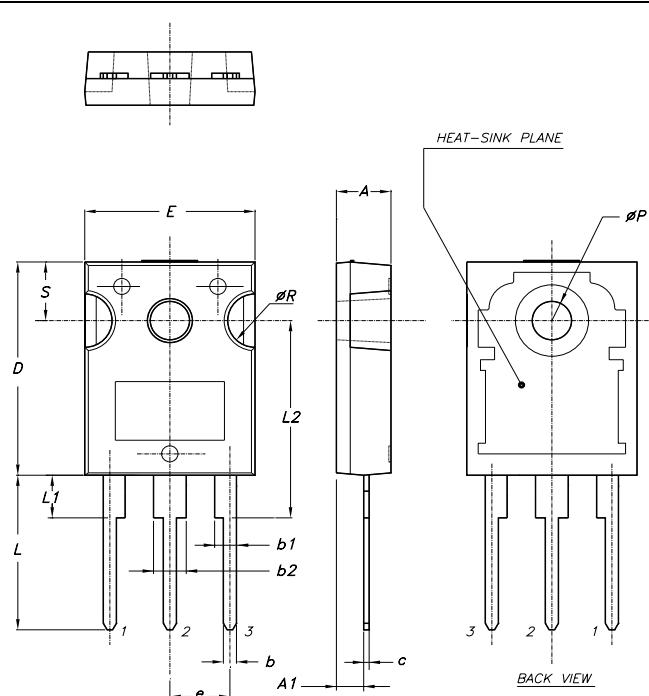
TO-220FP MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	4.4		4.6	0.173		0.181
B	2.5		2.7	0.098		0.106
D	2.5		2.75	0.098		0.108
E	0.45		0.7	0.017		0.027
F	0.75		1	0.030		0.039
F1	1.15		1.7	0.045		0.067
F2	1.15		1.7	0.045		0.067
G	4.95		5.2	0.195		0.204
G1	2.4		2.7	0.094		0.106
H	10		10.4	0.393		0.409
L2		16			0.630	
L3	28.6		30.6	1.126		1.204
L4	9.8		10.6	.0385		0.417
L5	2.9		3.6	0.114		0.141
L6	15.9		16.4	0.626		0.645
L7	9		9.3	0.354		0.366
Ø	3		3.2	0.118		0.126



TO-247 MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	4.85		5.15	0.19		0.20
A1	2.20		2.60	0.086		0.102
b	1.0		1.40	0.039		0.055
b1	2.0		2.40	0.079		0.094
b2	3.0		3.40	0.118		0.134
c	0.40		0.80	0.015		0.03
D	19.85		20.15	0.781		0.793
E	15.45		15.75	0.608		0.620
e		5.45			0.214	
L	14.20		14.80	0.560		0.582
L1	3.70		4.30	0.14		0.17
L2		18.50			0.728	
ϕP	3.55		3.65	0.140		0.143
ϕR	4.50		5.50	0.177		0.216
S		5.50			0.216	



Rev.E

Table 8: Revision History

Date	Revision	Description of Changes
11-Mar-2005	1	First release.

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