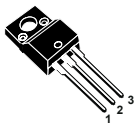
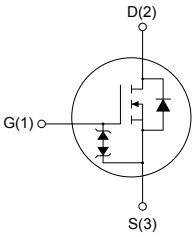
N-channel 525 V, 2.1 Ω typ., 2.5 A MDmesh™ K3 Power MOSFET in a TO-220FP package



TO-220FP



NG1D2S3Z

Features

Order code	V_{DS}	$R_{DS(on)}$ max.	I_D	Package
STF4N52K3	525 V	2.6 Ω	2.5 A	TO-220FP

- 100% avalanche tested
- Extremely high dv/dt capability
- Very low intrinsic capacitance
- Improved diode reverse recovery characteristics
- Zener-protected

Applications

- Switching applications

Description

This MDmesh™ K3 Power MOSFET is the result of improvements applied to STMicroelectronics' MDmesh™ technology, combined with a new optimized vertical structure. This device boasts an extremely low on-resistance, superior dynamic performance and high avalanche capability, rendering it suitable for the most demanding applications.

Product status link
STF4N52K3

Product summary	
Order code	STF4N52K3
Marking	4N52K3
Package	TO-220FP
Packing	Tube

1 Electrical ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage	525	V
V_{GS}	Gate-source voltage	±30	V
I_D	Drain current (continuous) at T_C = 25 °C	2.5 (1)	A
I_D	Drain current (continuous) at T_C = 100 °C	2 (1)	A
I_{DM} (2)	Drain current (pulsed)	10	A
P_{TOT}	Total dissipation at T_C = 25 °C	20	W
dv/dt (3)	Peak diode recovery voltage slope	12	V/ns
V_{ISO}	Insulation withstand voltage (RMS) from all three leads to external heat sink (t = 1 s, T_C = 25 °C)	2.5	kV
T_j	Operating junction temperature range	-55 to 150	°C
T_{stg}	Storage temperature range		

1. *Limited by package.*
2. *Pulse width limited by safe operating area.*
3. *I_{SD} ≤ 2.5 A, di/dt ≤ 400 A/µs, V_{DSpeak} ≤ $V_{(BR)DSS}$, V_{DD} = 80% $V_{(BR)DSS}$.*

Table 2. Thermal data

Symbol	Parameter	Value	Unit
$R_{thj\text{-}case}$	Thermal resistance junction-case	6.25	°C/W
$R_{thj\text{-}amb}$	Thermal resistance junction-ambient	62.5	°C/W

Table 3. Avalanche characteristics

Symbol	Parameter	Value	Unit
I_{AR} (1)	Avalanche current, repetitive or not-repetitive	1.3	A
E_{AS} (2)	Single pulse avalanche energy	110	mJ

1. *Pulse width limited by T_j max.*
2. *Starting T_j = 25 °C, I_D = I_{AR}, V_{DD} = 50 V.*

2 Electrical characteristics

(T_{CASE} = 25 °C unless otherwise specified)

Table 4. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	I_D = 1 mA, V_{GS} = 0 V	525			V
I_{DSS}	Zero gate voltage drain current	V_{GS} = 0 V, V_{DS} = 525 V			1	µA
		V_{GS} = 0 V, V_{DS} = 525 V, T_C = 125 °C (1)			50	µA
I_{GSS}	Gate body leakage current	V_{DS} = 0 V, V_{GS} = ±20 V			±10	µA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 50 µA	3	3.75	4.5	V
$R_{DS(on)}$	Static drain-source on resistance	V_{GS} = 10 V, I_D = 1.25 A		2.1	2.6	Ω

1. *Defined by design, not subject to production test.*

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	V_{DS} = 100 V, f = 1 MHz, V_{GS} = 0 V	-	334	-	pF
C_{oss}	Output capacitance			28		
C_{rss}	Reverse transfer capacitance			5		
$C_{oss\ eq.}$ (1)	Equivalent output capacitance	V_{DS} = 0 to 420 V, V_{GS} = 0 V	-	20	-	pF
R_G	Intrinsic gate resistance	f = 1 MHz open drain	-	4	-	Ω
Q_g	Total gate charge	V_{DD} = 420 V, I_D = 2.5 A, V_{GS} = 0 to 10 V (see Figure 14. Test circuit for gate charge behavior)	-	11	-	nC
Q_{gs}	Gate-source charge			2		
Q_{gd}	Gate-drain charge			7		

1. *$C_{oss\ eq.}$ is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 420 V.*

Table 6. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	V_{DD} = 260 V, I_D = 1.25 A, R_G = 4.7 Ω, V_{GS} = 10 V (see Figure 13. Test circuit for resistive load switching times and Figure 18. Switching time waveform)	-	8	-	ns
t_r	Rise time			7		
$t_{d(off)}$	Turn-off delay time			21		
t_f	Fall time			14		

Table 7. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		2.5	A
I_{SDM} (1)	Source-drain current (pulsed)				10	
V_{SD} (2)	Forward on voltage	I_{SD} = 2.5 A, V_{GS} = 0 V	-		1.6	V
t_{rr}	Reverse recovery time	I_{SD} = 2.5 A, di/dt = 100 A/µs	-	173		ns
Q_{rr}	Reverse recovery charge	V_{DD} = 60 V (see Figure 15. Test circuit for inductive load switching and diode recovery times)		778		nC
I_{RRM}	Reverse recovery current			9		A
t_{rr}	Reverse recovery time	I_{SD} = 2.5 A, di/dt = 100 A/µs	-	196		ns
Q_{rr}	Reverse recovery charge	V_{DD} = 60 V, T_j = 150 °C (see Figure 15. Test circuit for inductive load switching and diode recovery times)		941		nC
I_{RRM}	Reverse recovery current			10		A

1. *Pulse width limited by safe operating area.*
2. *Pulsed: pulse duration = 300 µs, duty cycle 1.5%.*

Table 8. Gate-source Zener diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)GSO}$	Gate-source breakdown voltage	I_{GS} = ±1 mA, I_D = 0 A	30	-	-	V

The built-in back-to-back Zener diodes are specifically designed to enhance the ESD performance of the device. The Zener voltage facilitates efficient and cost-effective device integrity protection, thus eliminating the need for additional external componentry.

2.1 Electrical characteristics curves

Figure 1. Safe operating area

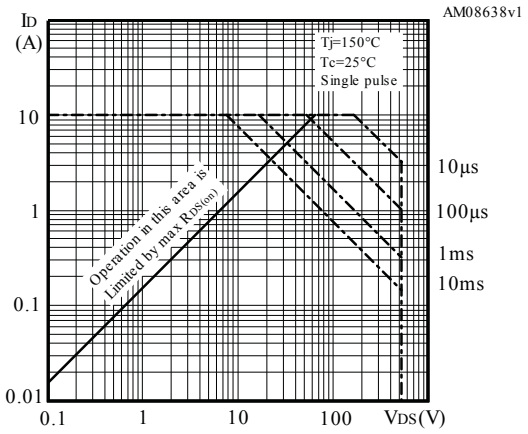


Figure 2. Thermal impedance

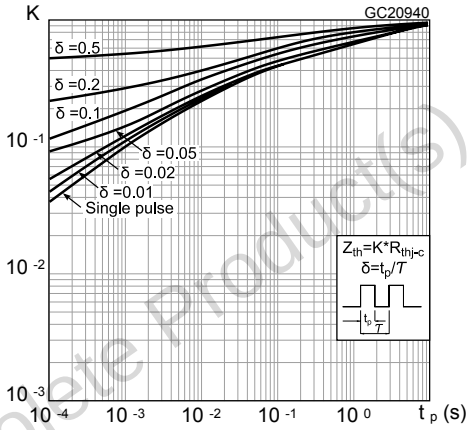


Figure 3. Output characterisics

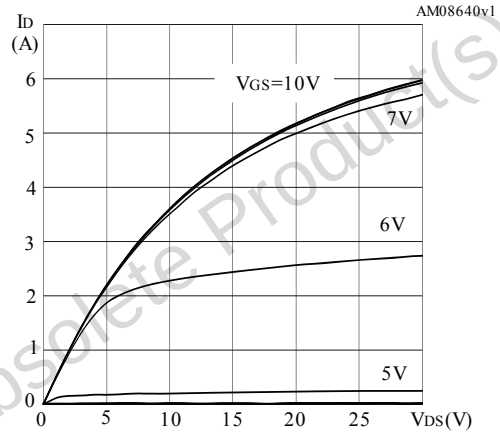


Figure 4. Transfer characteristics

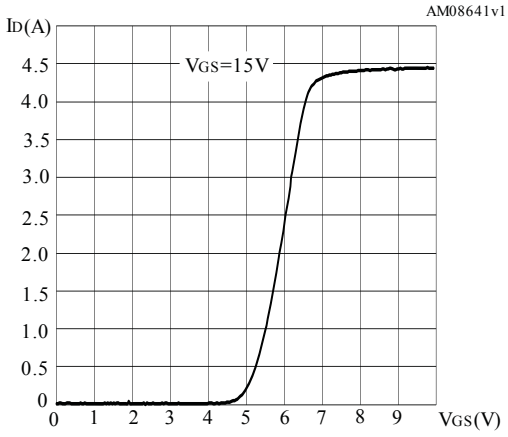


Figure 5. Normalized $V_{(BR)DSS}$ vs temperature

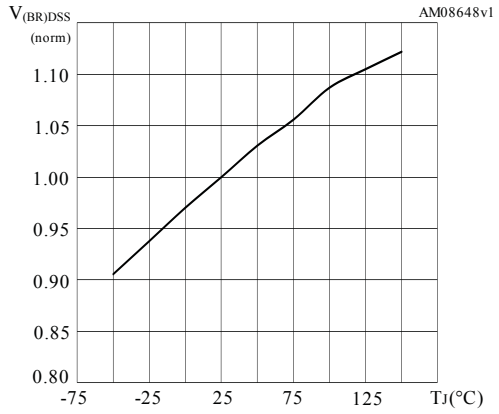


Figure 6. Static drain-source on-resistance

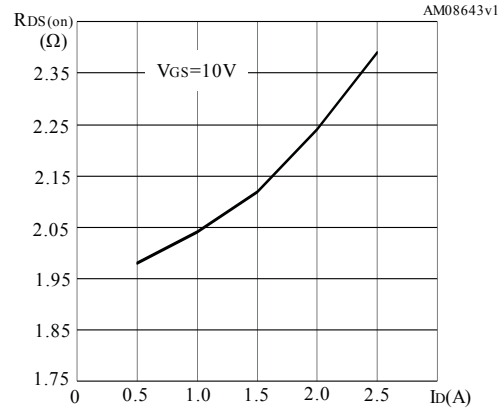


Figure 7. Gate charge vs gate-source voltage

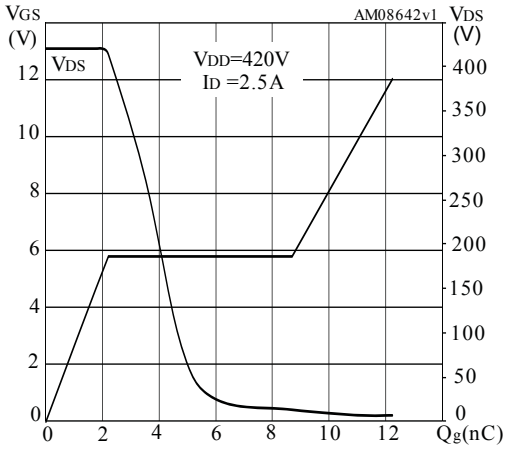


Figure 8. Capacitance variations

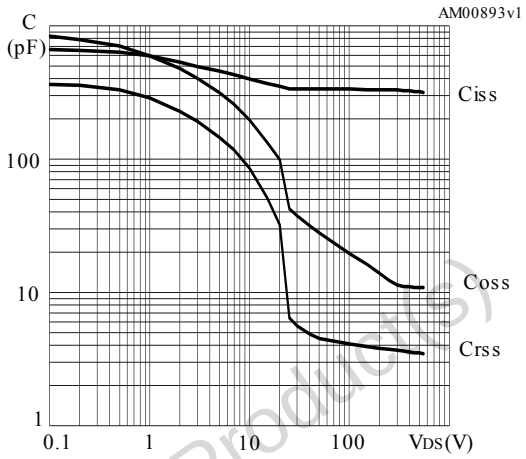


Figure 9. Normalized gate threshold voltage vs temperature

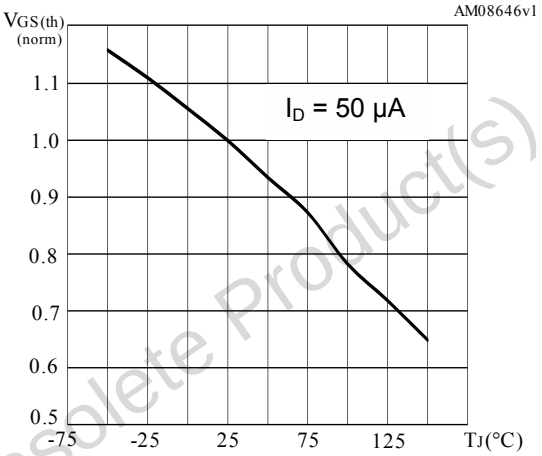


Figure 10. Normalized on-resistance vs temperature

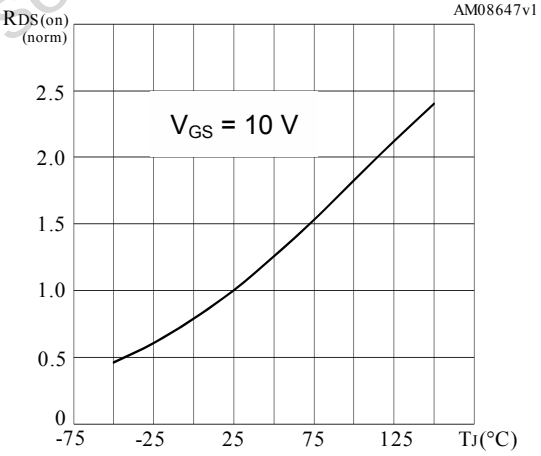


Figure 11. Source-drain diode forward characteristics

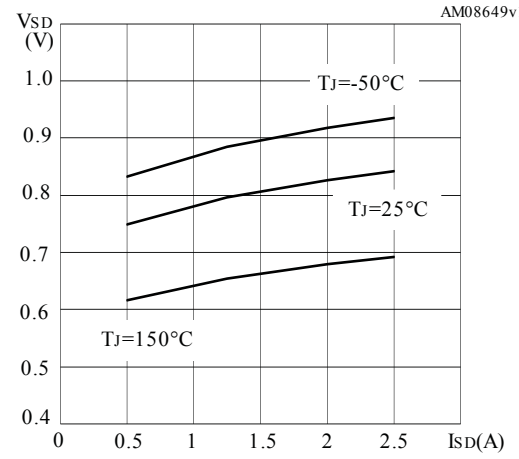
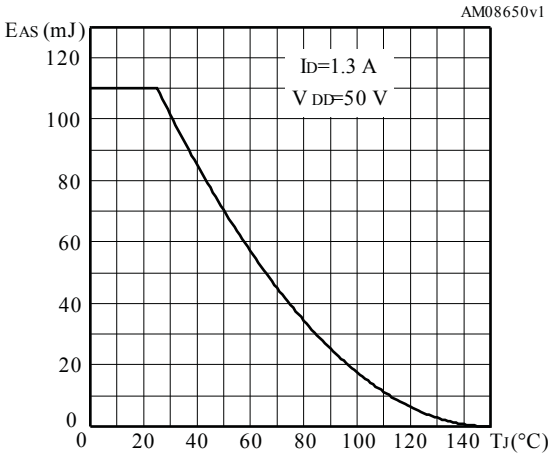


Figure 12. Maximum avalanche energy vs temperature



3 Test circuits

Figure 13. Test circuit for resistive load switching times

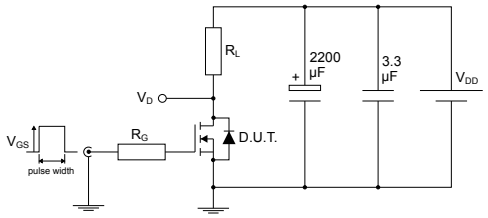


Figure 14. Test circuit for gate charge behavior

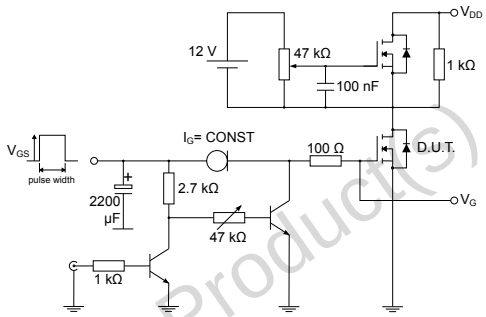


Figure 15. Test circuit for inductive load switching and diode recovery times

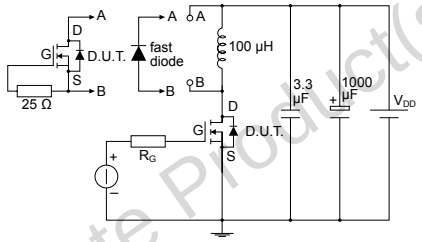


Figure 16. Unclamped inductive load test circuit

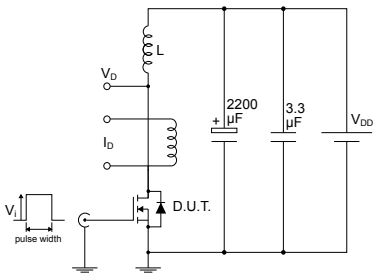


Figure 17. Unclamped inductive waveform

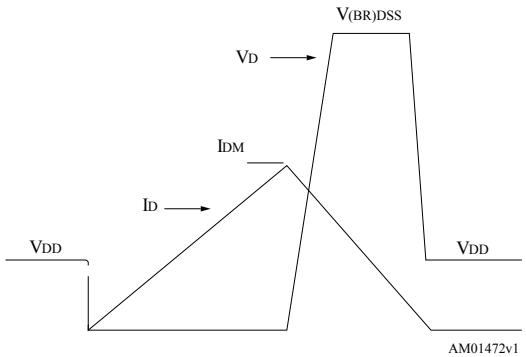
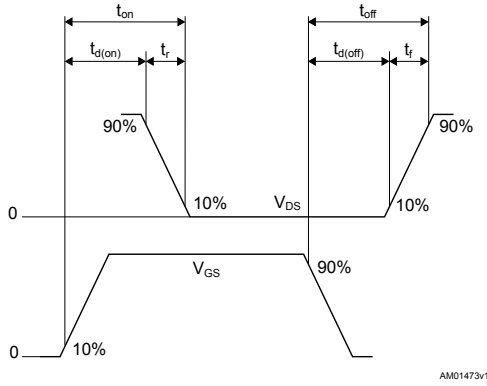


Figure 18. Switching time waveform



4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

4.1 TO-220FP package information

Figure 19. **TO-220FP package outline**

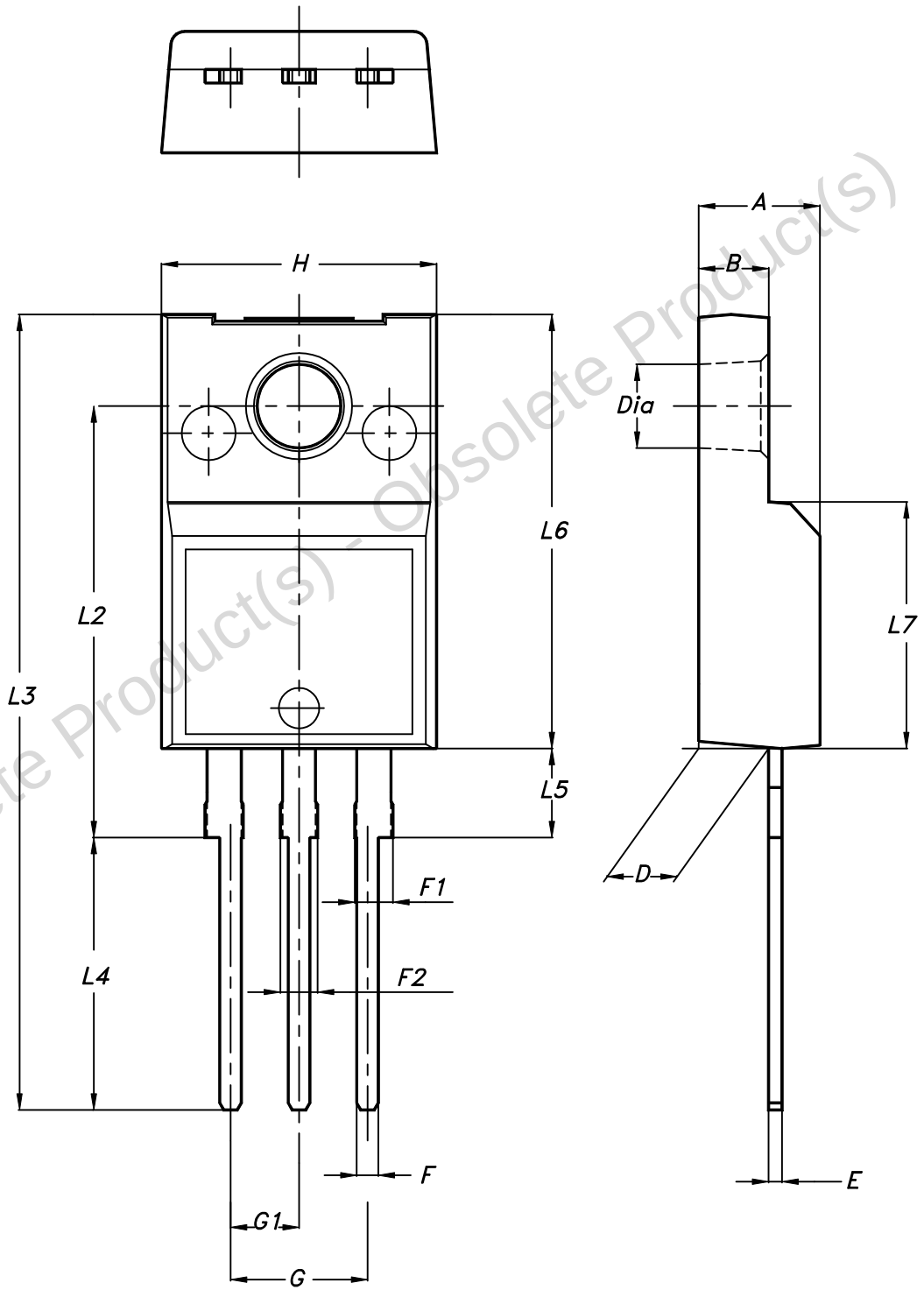


Table 9. **TO-220FP package mechanical data**

Dim.	mm		
	Min.	Typ.	Max.
A	4.4		4.6
B	2.5		2.7
D	2.5		2.75
E	0.45		0.7
F	0.75		1
F1	1.15		1.70
F2	1.15		1.70
G	4.95		5.2
G1	2.4		2.7
H	10		10.4
L2		16	
L3	28.6		30.6
L4	9.8		10.6
L5	2.9		3.6
L6	15.9		16.4
L7	9		9.3
Dia	3		3.2

Revision history

Table 10. **Document revision history**

Date	Version	Changes
27-Aug-2018	1	First release. Part number previously included in datasheet DocID18206.

Contents