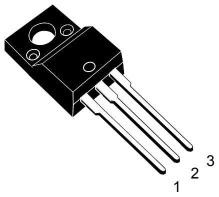
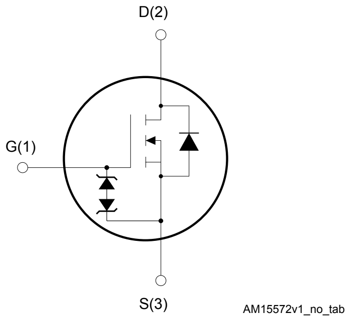
STF5N52U

Datasheet

N-channel 525 V, 1.25 Ω typ., 4.4 A, UltraFASTmesh™ Power MOSFET in a TO-220FP package



TO-220FP



Features

Order code	V_{DS}	$R_{DS(on)}$ max.	I_D	P_{TOT}
STF5N52U	525 V	1.50 Ω	4.4 A	25 W

- Outstanding dv/dt capability
- Gate charge minimized
- Very low intrinsic capacitances
- Very low $R_{DS(on)}$
- Extremely low t_{rr}

Applications

- Switching applications

Description

This device is N-channel Power MOSFET developed using UltraFASTmesh™ technology, which combines the advantages of reduced on resistance, Zener gate protection and very high dv/dt capability with an enhanced fast body-drain recovery diode.

Product status link
STF5N52U

Product summary	
Order code	STF5N52U
Marking	5N52U
Package	TO-220FP
Packing	Tube

1 Electrical ratings

Table 1. **Absolute maximum ratings**

Symbol	Parameter	Value	Unit
V_{GS}	Gate- source voltage	±30	V
I_D	Drain current (continuous) at T_C = 25 °C	4.4	A
I_D	Drain current (continuous) at T_C= 100 °C	2.8	
I_{DM} (1)	Drain current (pulsed)	17.6	A
P_{TOT}	Total power dissipation at T_C = 25 °C	25	W
dv/dt (2)	Peak diode recovery voltage slope	20	V/ns
V_{ISO}	Insulation withstand voltage (RMS) from all three leads to external heat sink (t=1 s; T_C=25 °C)	2.5	kV
T_{stg}	Storage temperature range	-55 to 150	°C
T_j	Operating junction temperature range		
ESD	Gate-source human body model (R = 1.5 kΩ, C = 100 pF)	2.8	kV

1. *Pulse width limited by safe operating area.*
2. $I_{SD} \leq 4.4$ *A, di/dt* $\leq$ *400 A/µs,* $V_{DS\ peak} < V_{(BR)DSS}$, V_{DD} = *80%* $V_{(BR)DSS}$

Table 2. **Thermal data**

Symbol	Parameter	Value	Unit
$R_{thj\text{-}case}$	Thermal resistance junction-case	5	°C/W
$R_{thj\text{-}amb}$	Thermal resistance junction-ambient	62.5	

Table 3. **Avalanche characteristics**

Symbol	Parameter	Value	Unit
I_{AR}	Avalanche current, repetitive or non-repetitive (pulse width limited by T_{jmax})	4.4	A
E_{AS}	Single pulse avalanche energy (starting T_j = 25 °C, I_D = I_{AR}, V_{DD} = 50 V)	170	mJ

2 Electrical characteristics

(T_C = 25 °C unless otherwise specified).

Table 4. **On/off states**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V, I_D = 1 mA	525			V
I_{DSS}	Zero gate voltage drain current	V_{GS} = 0 V, V_{DS} = 525 V			10	µA
		V_{GS} = 0 V, V_{DS} = 525 V, T_C = 125 °C[1]			500	µA
I_{GSS}	Gate-body leakage current	V_{DS} = 0 V, V_{GS} = ±20 V			±10	µA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 50 µA	3	3.75	4.5	V
$R_{DS(on)}$	Static drain-source on-resistance	V_{GS} = 10 V, I_D = 2.2 A		1.25	1.50	Ω

1. *Defined by design, not subject to production test.*

Table 5. **Dynamic**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	V_{DS}= 25 V, f = 1 MHz, V_{GS} = 0 V	-	529	-	pF
C_{oss}	Output capacitance		-	71	-	pF
C_{rss}	Reverse transfer capacitance		-	13.4	-	pF
$C_{oss\ eq.}$ [1]	Equivalent output capacitance	V_{DS} = 0 V to 420 V, V_{GS} = 0 V	-	11	-	pF
R_G	Intrinsic gate resistance	f = 1 MHz, I_D = 0 A	-	6	-	Ω
Q_g	Total gate charge	V_{DD} = 416 V, I_D = 4.4 A, V_{GS} = 0 to 10 V (see Figure 14. Test circuit for gate charge behavior)	-	16.9	-	nC
Q_{gs}	Gate-source charge		-	4.2	-	nC
Q_{gd}	Gate-drain charge		-	8.4	-	nC

1. *$C_{oss\ eq.}$ is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}*

Table 6. **Switching times**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	V_{DD} = 260 V, I_D = 2.2 A, R_G = 4.7 Ω, V_{GS} = 10 V (see Figure 13. Test circuit for resistive load switching times and Figure 18. Switching time waveform)	-	11.4	-	ns
t_r	Rise time		-	13.6	-	
$t_{d(off)}$	Turn-off delay time		-	23.1	-	
t_f	Fall time		-	15	-	

Table 7. **Source drain diode**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		4.4	A
I_{SDM}(1)	Source-drain current (pulsed)		-		17.6	A
V_{SD}	Forward on voltage	V_{GS} = 0 V, I_{SD} = 4.4 A	-		1.6	V
t_{rr}	Reverse recovery time	I_{SD} = 4.4 A, di/dt = 100 A/µs, V_{DD} = 60 V (see Figure 15. Test circuit for inductive load switching and diode recovery times)	-	55		ns
Q_{rr}	Reverse recovery charge		-	95		nC
I_{RRM}	Reverse recovery current		-	3.5		A
t_{rr}	Reverse recovery time	I_{SD} = 4.4 A, di/dt = 100 A/µs, V_{DD} = 60 V, T_j = 150 °C (see Figure 15. Test circuit for inductive load switching and diode recovery times)	-	120		ns
Q_{rr}	Reverse recovery charge		-	266		nC
I_{RRM}	Reverse recovery current		-	4.5		A

1. *Pulse width is limited by safe operating area*
2. *Pulse test: pulse duration = 300 µs, duty cycle 1.5%*

Table 8. **Source drain diode**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)GSO}$	Gate-source breakdown voltage	I_{GS} = ± 1mA, I_D = 0 V	30	-	-	V

The built-in back-to-back Zener diodes have specifically been designed to enhance the device's ESD capability. In this respect the Zener voltage is appropriate to achieve an efficient and cost-effective intervention to protect the device's integrity. These integrated Zener diodes thus avoid the usage of external components.

2.1 Electrical characteristics (curves)

Figure 1. Safe operating area

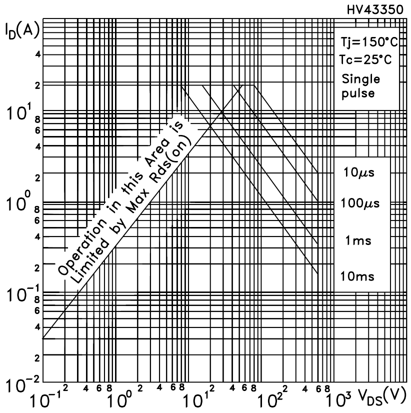


Figure 2. Thermal impedance

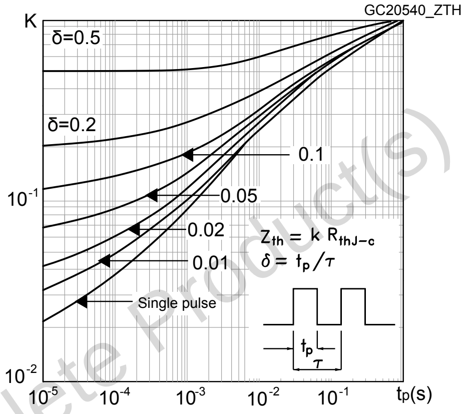


Figure 3. Output characteristics

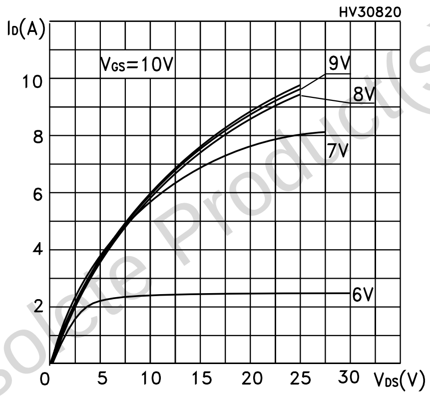


Figure 4. Transfer characteristics

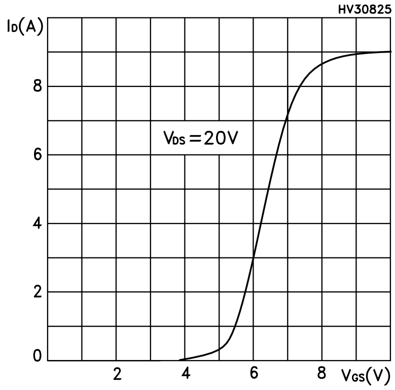


Figure 5. Normalized $V_{(BR)DSS}$ vs temperature

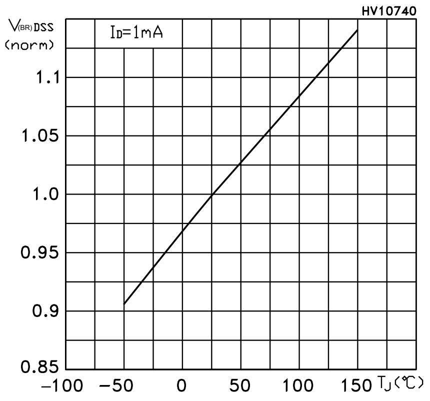


Figure 6. Static drain-source on-resistance

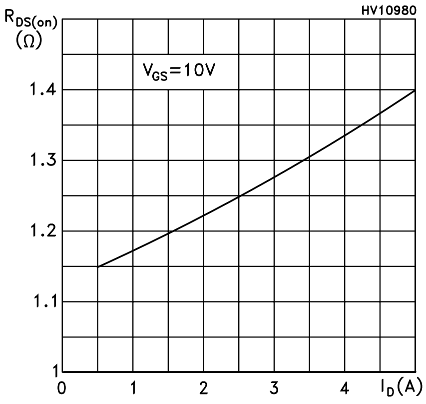


Figure 7. Gate charge vs gate-source voltage

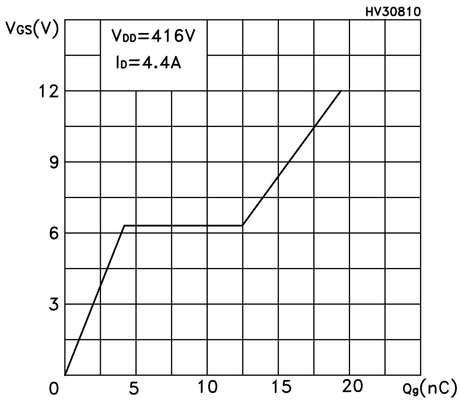


Figure 8. Capacitance variations

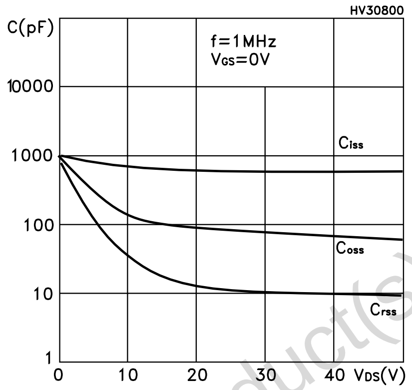


Figure 9. Normalized gate threshold voltage vs temperature

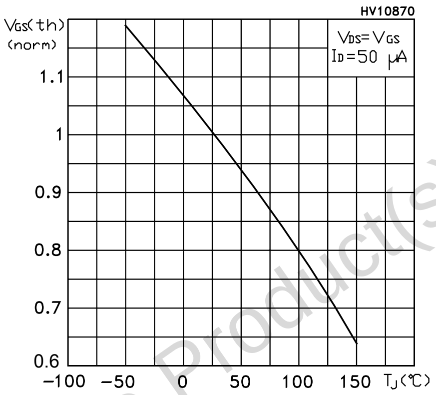


Figure 10. Normalized on-resistance vs temperature

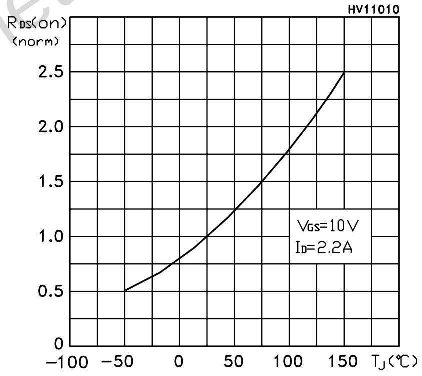


Figure 11. Source-drain diode forward characteristics

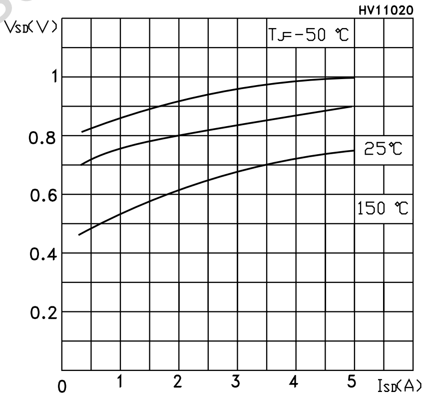
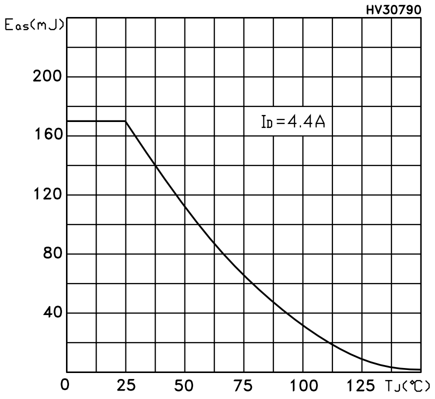


Figure 12. Maximum avalanche energy vs temperature



3 Test circuits

Figure 13. Test circuit for resistive load switching times

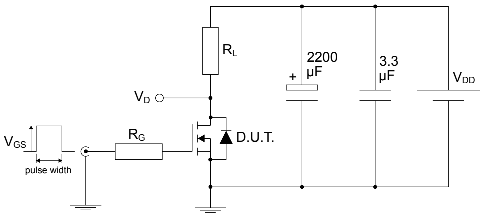


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Figure 14. Test circuit for gate charge behavior

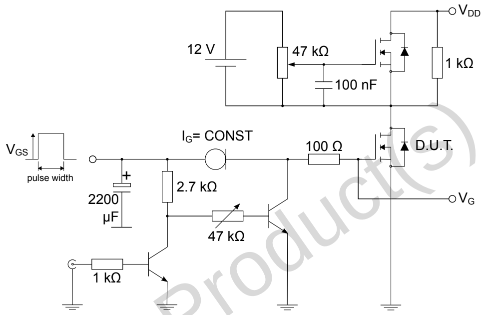

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Figure 15. Test circuit for inductive load switching and diode recovery times

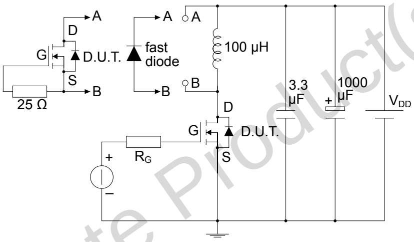

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Figure 16. Unclamped inductive load test circuit

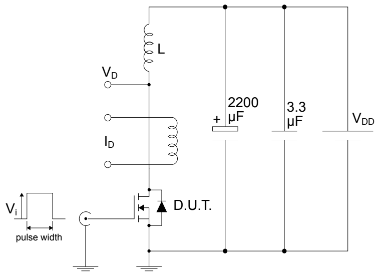

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Figure 17. Unclamped inductive waveform

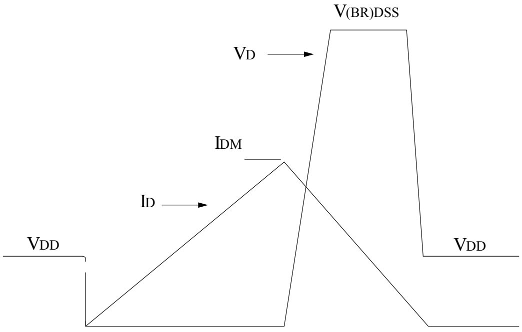

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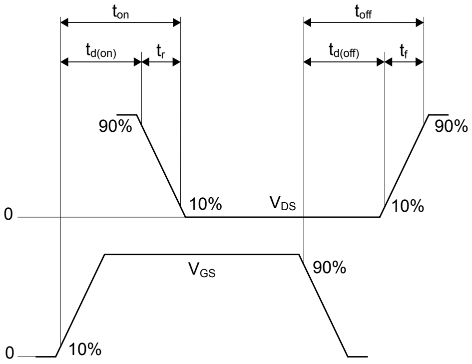
Figure 18. Switching time waveform



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4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

4.1 TO-220FP package information

Figure 19. **TO-220FP package outline**

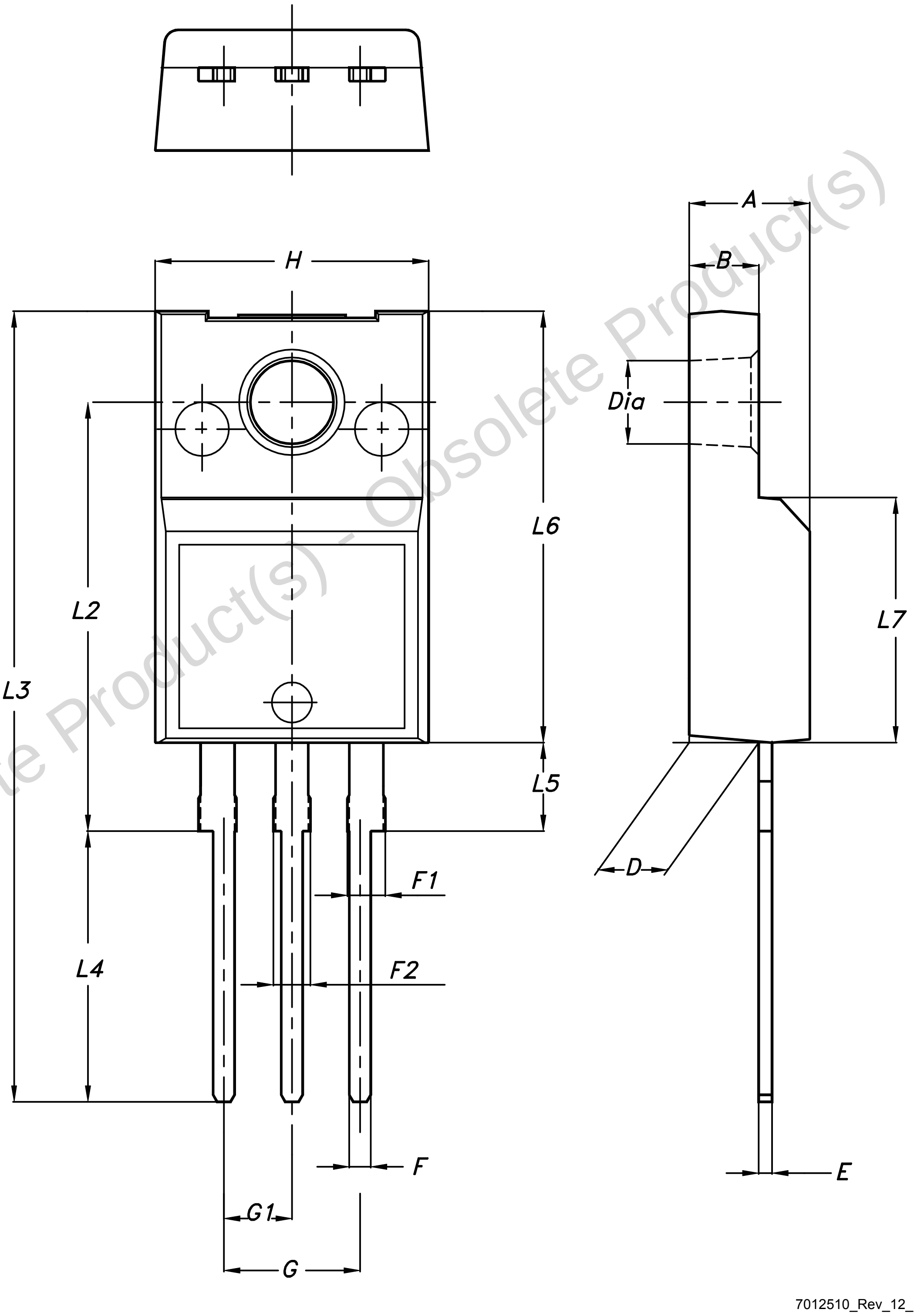

Table 9. **TO-220FP package mechanical data**

Dim.	mm		
	Min.	Typ.	Max.
A	4.4		4.6
B	2.5		2.7
D	2.5		2.75
E	0.45		0.7
F	0.75		1
F1	1.15		1.70
F2	1.15		1.70
G	4.95		5.2
G1	2.4		2.7
H	10		10.4
L2		16	
L3	28.6		30.6
L4	9.8		10.6
L5	2.9		3.6
L6	15.9		16.4
L7	9		9.3
Dia	3		3.2

Revision history

Table 10. Document revision history

Date	Version	Changes
05-Mar-2019	1	First release. Part number previously included in datasheet DocID15684.

Contents