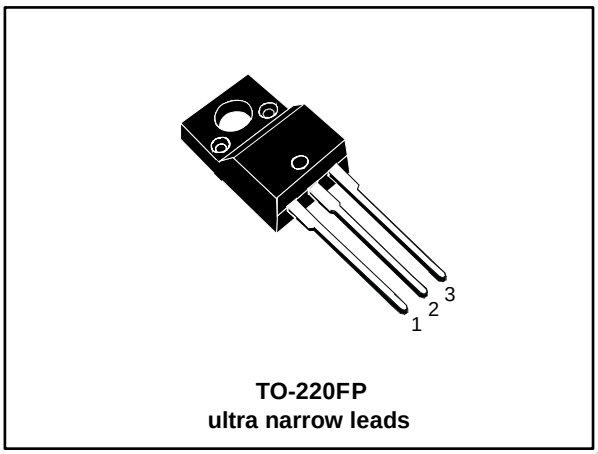
STFU260N4F7

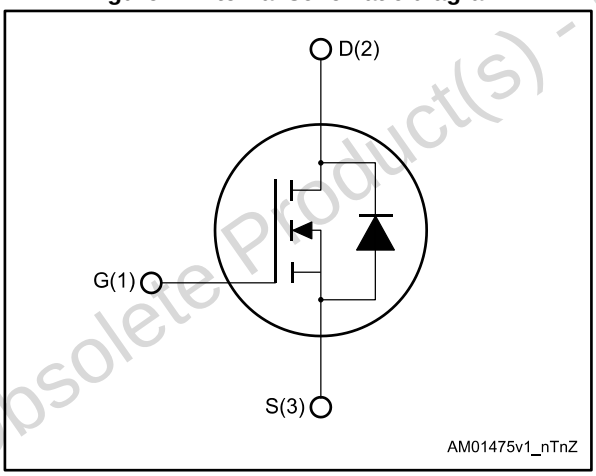
N-channel 40 V, 1.95 mΩ typ., 90 A, STripFET™ F7 Power MOSFET in a TO-220FP ultra narrow leads package

Datasheet - preliminary data



TO-220FP
ultra narrow leads

Figure 1: Internal schematic diagram



Features

Order code	V_{DS}	$R_{DS(on)}$ max.	I_D
STFU260N4F7	40 V	2.5 mΩ	35 W

- Among the lowest $R_{DS(on)}$ on the market
- Excellent figure of merit (FoM)
- Low C_{rss}/C_{iss} ratio for EMI immunity
- High avalanche ruggedness

Applications

- Switching applications

Description

This N-channel Power MOSFET utilizes STripFET™ F7 technology with an enhanced trench gate structure that results in very low on-state resistance, while also reducing internal capacitance and gate charge for faster and more efficient switching.

Table 1: Device summary

Order code	Marking	Package	Packing
STFU260N4F7	260N4F7	TO-220FP ultra narrow leads	Tube

Contents

1 Electrical ratings

Table 2: Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage	40	V
V_{GS}	Gate-source voltage	±20	V
I_D	Drain current (continuous) at T_C= 25 °C	90	A
I_D	Drain current (continuous) at T_C = 100 °C	64	A
I_{DM} (1)	Drain current (pulsed)	360	A
P_{TOT}	Total dissipation at T_C = 25 °C	35	W
V_{iso}	Insulation withstand voltage (RMS) from all three leads to external heat sink (t = 1s; T_C= 25 °C)	2.5	kV
T_{stg}	Storage temperature	-55 to 175	°C
T_J	Operation junction temperature		

Notes:

(1)Pulse width limited by safe operating area

Table 3: Thermal data

Symbol	Parameter	Value	Unit
$R_{thj\text{-}case}$	Thermal resistance junction-case max	4.29	°C/W
$R_{thj\text{-}amb}$	Thermal resistance junction-ambient max	62.5	°C/W

2 Electrical characteristics

(T_C = 25 °C unless otherwise specified)

Table 4: On /off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V, I_D = 250 µA	40			V
I_{DSS}	Zero gate voltage drain current	V_{GS} = 0 V, V_{DS} = 40 V			1	µA
		V_{GS} = 0 V, V_{DS} = 40 V, T_C = 125 °C			100	µA
I_{GSS}	Gate-body leakage current	V_{DS} = 0 V, V_{GS} = + 20 V			100	nA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 250 µA	2		4	V
$R_{DS(on)}$	Static drain-source on-resistance	V_{GS} = 10 V, I_D = 60 A		1.95	2.5	mΩ

Table 5: Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	V_{GS} = 0 V, V_{DS} = 25 V, f = 1 MHz	-	5640	-	pF
C_{oss}	Output capacitance		-	2370	-	pF
C_{rss}	Reverse transfer capacitance		-	34	-	pF
Q_g	Total gate charge	V_{DD} = 20 V, I_D = 120 A, V_{GS} = 10 V (see *Figure 3: "Test circuit for gate charge behavior"*)	-	67	-	nC
Q_{gs}	Gate-source charge		-	31	-	nC
Q_{gd}	Gate-drain charge		-	10	-	nC

Table 6: Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	V_{DD} = 20 V, I_D = 60 A, R_G = 4.7 Ω, V_{GS} = 10 V (see *Figure 2: "Test circuit for resistive load switching times"* and *Figure 7: "Switching time waveform"*	-	30	-	ns
t_r	Rise time		-	21	-	ns
$t_{d(off)}$	Turn-off delay time		-	42	-	ns
t_f	Fall time		-	13	-	ns

Table 7: Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{SD} (1)	Forward on voltage	V_{GS} = 0 V, I_{SD} = 120 A	-	-	1.1	V
t_{rr}	Reverse recovery time	I_{SD} = 120 A, di/dt = 100 A/µs V_{DD} = 32 V (see *Figure 4: "Test circuit for inductive load switching and diode recovery times"*)	-	68		ns
Q_{rr}	Reverse recovery charge		-	98		nC
I_{RRM}	Reverse recovery current		-	3		A

Notes:

(1)Pulsed: pulse duration = 300 µs, duty cycle 1.5%

3 Test circuits

Figure 2: Test circuit for resistive load switching times

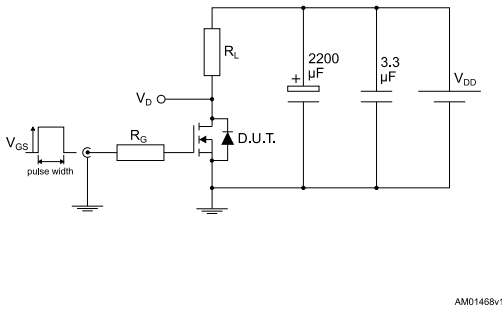


Figure 3: Test circuit for gate charge behavior

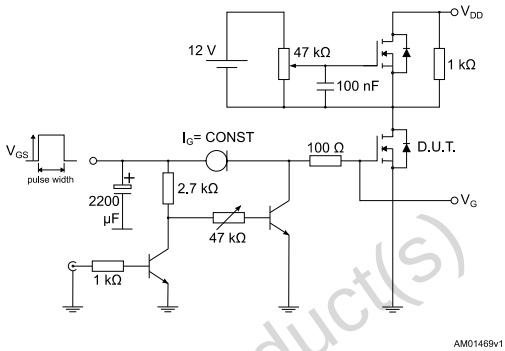


Figure 4: Test circuit for inductive load switching and diode recovery times

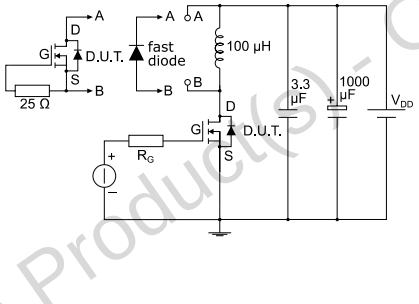


Figure 5: Unclamped inductive load test circuit

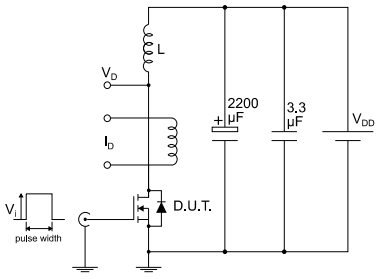


Figure 6: Unclamped inductive waveform

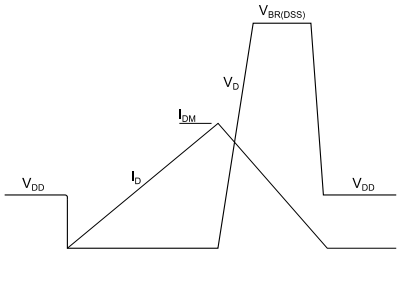
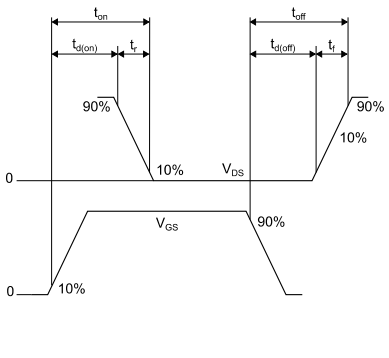


Figure 7: Switching time waveform



4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: ***www.st.com***. ECOPACK® is an ST trademark.

4.1 TO-220FP ultra narrow leads package information

Figure 8: TO-220FP ultra narrow leads package outline

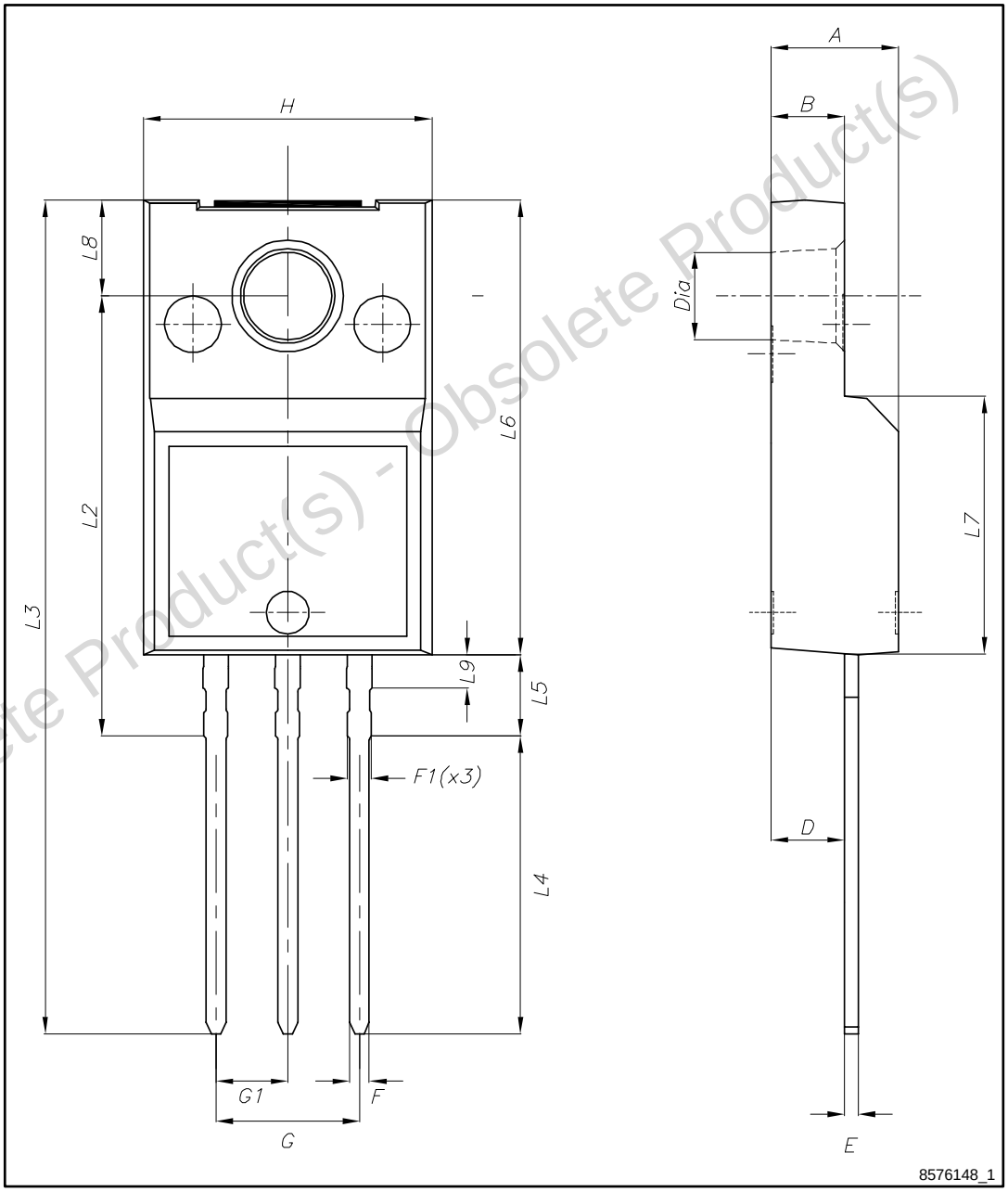


Table 8: TO-220FP ultra narrow leads mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.40		4.60
B	2.50		2.70
D	2.50		2.75
E	0.45		0.60
F	0.65		0.75
F1	-		0.90
G	4.95		5.20
G1	2.40	2.54	2.70
H	10.00		10.40
L2	15.10		15.90
L3	28.50		30.50
L4	10.20		11.00
L5	2.50		3.10
L6	15.60		16.40
L7	9.00		9.30
L8	3.20		3.60
L9	-		1.30
Dia.	3.00		3.20

5 Revision history

Table 9: Document revision history

Date	Revision	Changes
11-Nov-2015	1	Initial release.

IMPORTANT NOTICE – PLEASE READ CAREFULLY

STMicroelectronics NV and its subsidiaries (“ST”) reserve the right to make changes, corrections, enhancements, modifications, and improvements to ST products and/or to this document at any time without notice. Purchasers should obtain the latest relevant information on ST products before placing orders. ST products are sold pursuant to ST’s terms and conditions of sale in place at the time of order acknowledgement.

Purchasers are solely responsible for the choice, selection, and use of ST products and ST assumes no liability for application assistance or the design of Purchasers’ products.

No license, express or implied, to any intellectual property right is granted by ST herein.

Resale of ST products with provisions different from the information set forth herein shall void any warranty granted by ST for such product.

ST and the ST logo are trademarks of ST. All other product or service names are the property of their respective owners.

Information in this document supersedes and replaces information previously supplied in any prior versions of this document.