STFW69N65M5
STW69N65M5

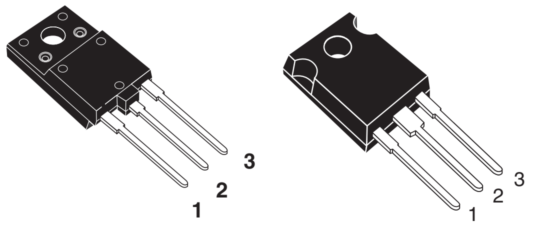
N-channel 650 V, 0.037 Ω typ., 58 A MDmesh™ V Power MOSFET in TO-3PF and TO-247 packages

Datasheet — production data

Features

Order codes	V_{DSS} @ T_{Jmax}	$R_{DS(on)}$ max	I_D
STFW69N65M5	710 V	< 0.045 Ω	58 A
STW69N65M5			

- Worldwide best $R_{DS(on)}$ * area
- Higher V_{DSS} rating and high dv/dt capability
- Excellent switching performance
- 100% avalanche tested



TO-3PF TO-247

Applications

- Switching applications

Description

These devices are N-channel MDmesh™ V Power MOSFETs based on an innovative proprietary vertical process technology, which is combined with STMicroelectronics' well-known PowerMESH™ horizontal layout structure. The resulting product has extremely low on-resistance, which is unmatched among silicon-based Power MOSFETs, making it especially suitable for applications which require superior power density and outstanding efficiency.

Figure 1. Internal schematic diagram

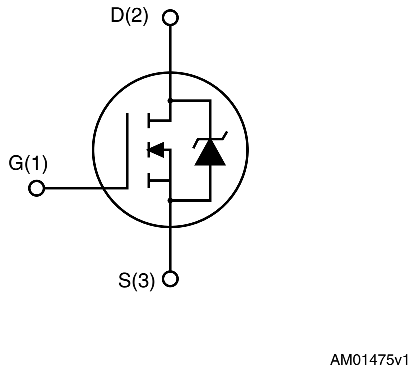


Table 1. Device summary

Order codes	Marking	Package	Packaging
STFW69N65M5	69N65M5	TO-3PF	Tube
STW69N65M5		TO-247	

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1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value		Unit
		TO-3PF	TO-247	
V_{GS}	Gate-source voltage	± 25		V
I_D	Drain current (continuous) at T_C = 25 °C	58[(1)]	58	A
I_D	Drain current (continuous) at T_C = 100 °C	36.5 [(1)]	36.5	A
I_{DM} [(2)]	Drain current (pulsed)	232 [(1)]	232	A
P_{TOT}	Total dissipation at T_C = 25 °C	79	330	W
dv/dt [(3)]	Peak diode recovery voltage slope	15		V/ns
V_{ISO}	Insulation withstand voltage (RMS) from all three leads to external heat sink (t=1s; Tc=25°C)	3500		V
T_{stg}	Storage temperature	- 55 to 150		°C
T_j	Max. operating junction temperature	150		°C

1. Limited by maximum junction temperature.
2. Pulse width limited by safe operating area
3. $I_{SD} \leq 58$ A, di/dt ≤400 A/µs; $V_{DS\ peak} < V_{(BR)DSS}$, V_{DD}=400 V

Table 3. Thermal data

Symbol	Parameter	Value		Unit
		TO-3PF	TO-247	
$R_{thj\text{-}case}$	Thermal resistance junction-case max	1.58	0.38	°C/W
$R_{thj\text{-}amb}$	Thermal resistance junction-ambient max	50		°C/W

Table 4. Avalanche characteristics

Symbol	Parameter	Value	Unit
I_{AR}	Avalanche current, repetetive or not repetetive (pulse width limited by T_{jmax})	12	A
E_{AS}	Single pulse avalanche energy (starting t_j=25°C, I_d= I_{AR}; V_{dd}=50)	1410	mJ

2 Electrical characteristics

(T_C = 25 °C unless otherwise specified)

Table 5. On /off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	I_D = 1 mA, V_{GS} = 0	650			V
I_{DSS}	Zero gate voltage drain current (V_{GS} = 0)	V_{DS} = 650 V V_{DS} = 650 V, T_C=125 °C			1 100	µA µA
I_{GSS}	Gate-body leakage current (V_{DS} = 0)	V_{GS} = ± 25 V			± 100	nA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 250 µA	3	4	5	V
$R_{DS(on)}$	Static drain-source on-resistance	V_{GS} = 10 V, I_D = 29 A		0.037	0.045	Ω

Table 6. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss} C_{oss} C_{rss}	Input capacitance Output capacitance Reverse transfer capacitance	V_{DS} = 100 V, f = 1 MHz, V_{GS} = 0	-	6420 170 11	-	pF pF pF
$C_{o(tr)}$(1)	Equivalent capacitance time related	V_{DS} = 0 to 520 V, V_{GS} = 0	-	536	-	pF
$C_{o(er)}$(2)	Equivalent capacitance energy related		-	146	-	pF
R_G	Intrinsic gate resistance	f = 1 MHz open drain	-	1.2	-	Ω
Q_g Q_{gs} Q_{gd}	Total gate charge Gate-source charge Gate-drain charge	V_{DD} = 520 V, I_D = 29 A, V_{GS} = 10 V (see *Figure 18*)	-	143 38 64	-	nC nC nC

1. Time related is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}
2. Energy related is defined as a constant equivalent capacitance giving the same stored energy as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}

Table 7. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max	Unit
$t_{d(v)}$ $t_{r(v)}$ $t_{f(i)}$ $t_{c(off)}$	Voltage delay time Voltage rise time Current fall time Crossing time	V_{DD} = 400 V, I_D = 38 A, R_G = 4.7 Ω, V_{GS} = 10 V (see *Figure 19* and *Figure 22*)	-	102 13.5 10 19	-	ns ns ns ns

Table 8. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD} I_{SDM} (1)	Source-drain current Source-drain current (pulsed)		-		58 232	A A
V_{SD} (2)	Forward on voltage	I_{SD} = 58 A, V_{GS} = 0	-		1.5	V
t_{rr} Q_{rr} I_{RRM}	Reverse recovery time Reverse recovery charge Reverse recovery current	I_{SD} = 58 A, di/dt = 100 A/µs V_{DD} = 100 V (see *Figure 19*)	-	480 11 46		ns µC A
t_{rr} Q_{rr} I_{RRM}	Reverse recovery time Reverse recovery charge Reverse recovery current	I_{SD} = 58 A, di/dt = 100 A/µs V_{DD} = 100 V, T_j = 150 °C (see *Figure 19*)	-	592 16 53		ns µC A

1. Pulse width limited by safe operating area.
2. Pulsed: pulse duration = 300 µs, duty cycle 1.5%

2.1 Electrical characteristics (curves)

Figure 2. Safe operating area for TO-3PF

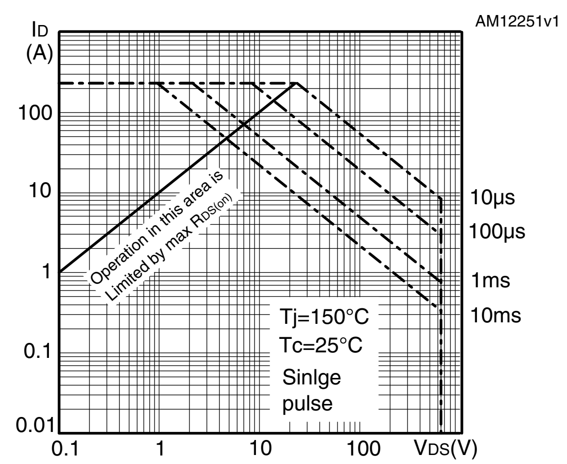


Figure 3. Thermal impedance for TO-3PF

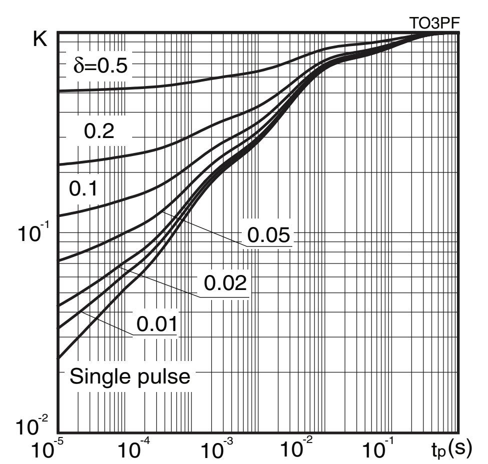


Figure 4. Safe operating area for TO-247

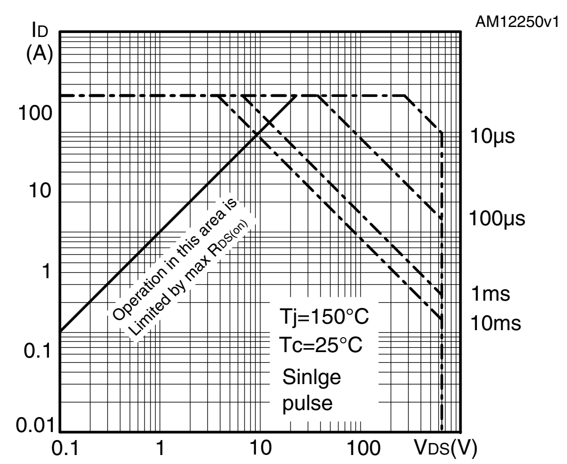


Figure 5. Thermal impedance for TO-247

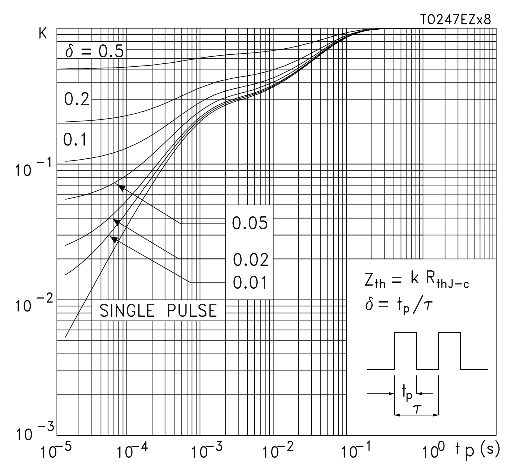


Figure 6. Output characteristics

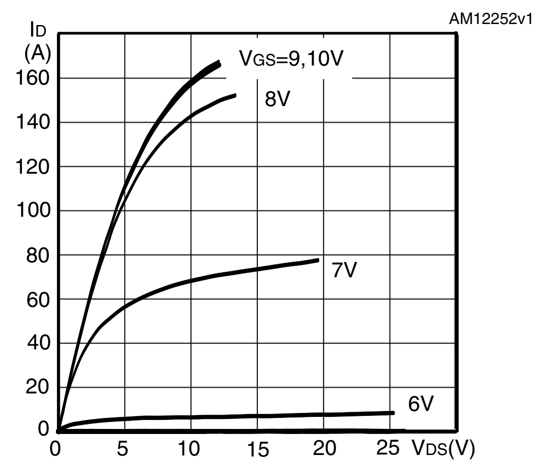


Figure 7. Transfer characteristics

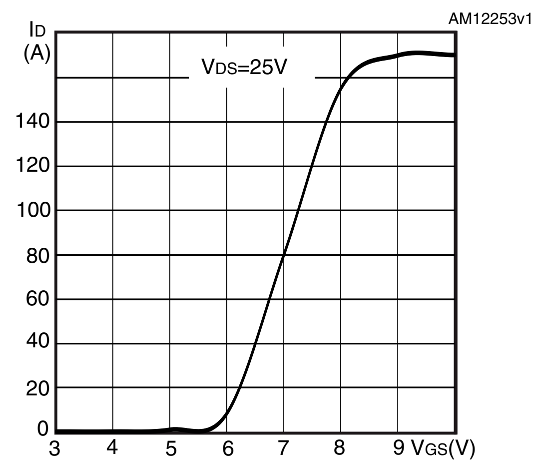


Figure 8. Gate charge vs gate-source voltage

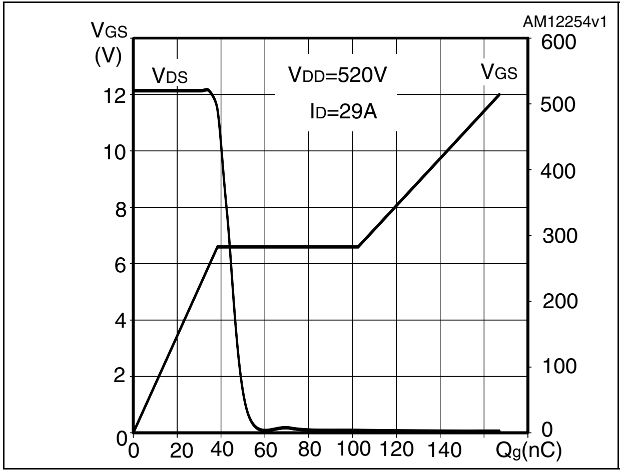


Figure 9. Static drain-source on-resistance

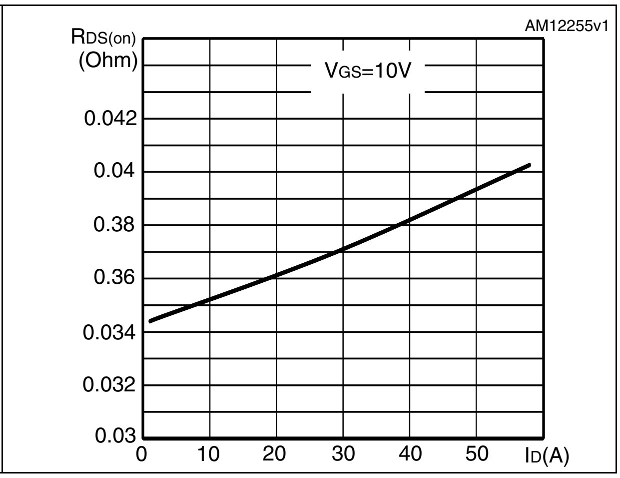


Figure 10. Capacitance variations

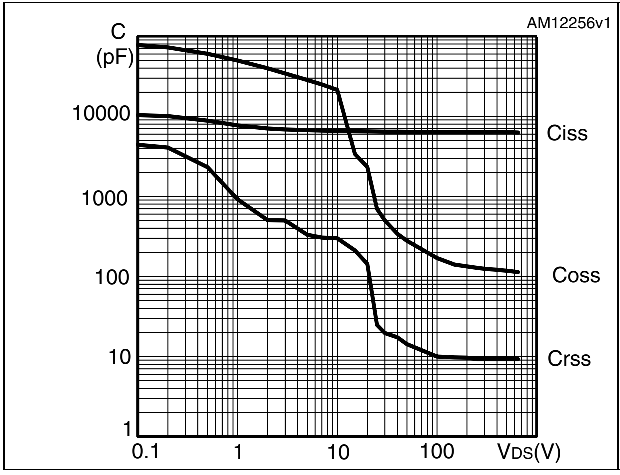


Figure 11. Output capacitance stored energy

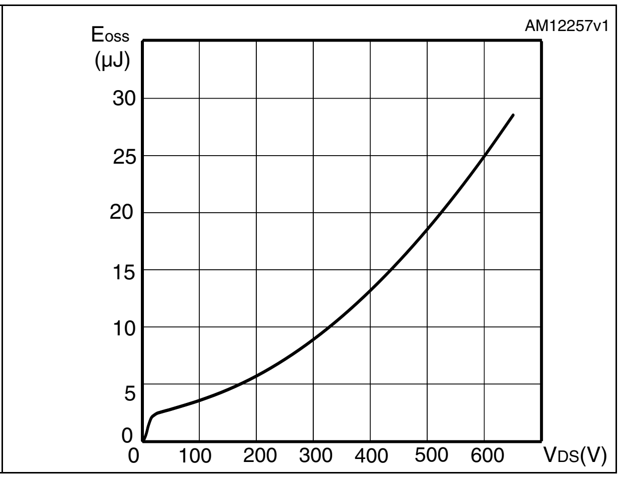


Figure 12. Normalized gate threshold voltage vs temperature

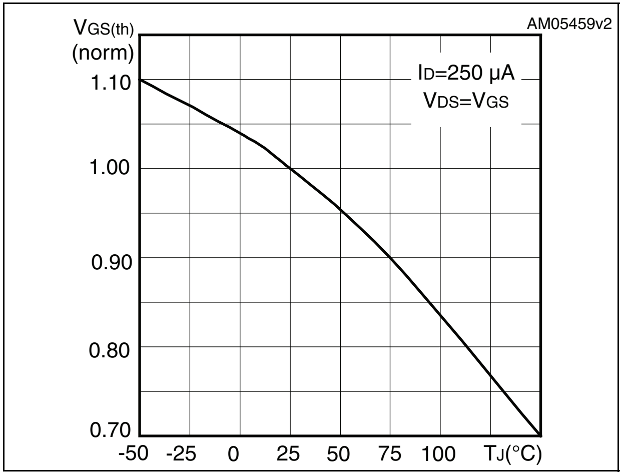


Figure 13. Normalized on-resistance vs temperature

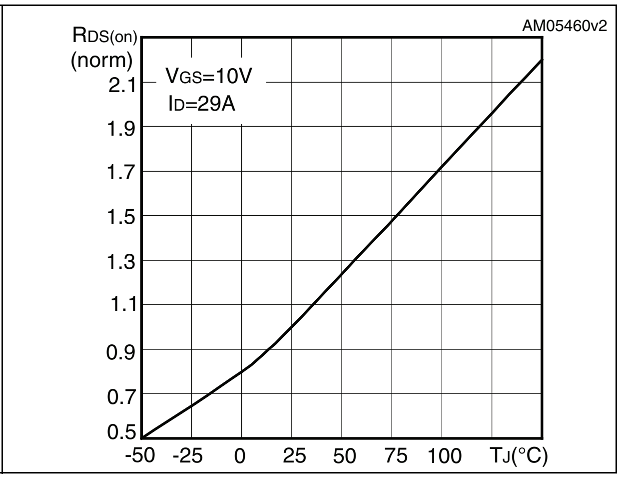


Figure 14. Source-drain diode forward characteristics

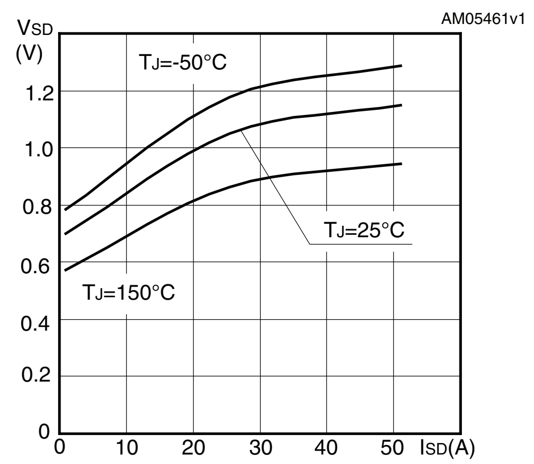


Figure 15. Normalized B_{VDSS} vs temperature

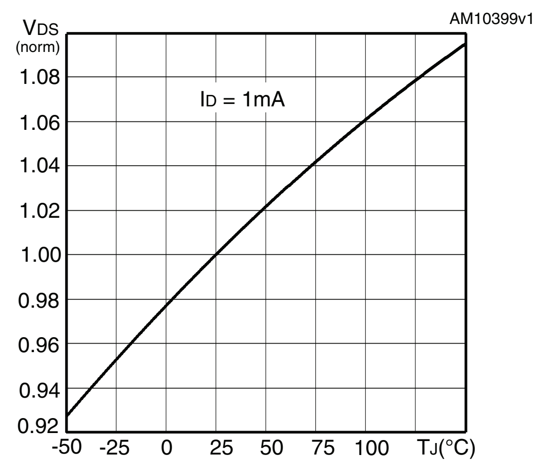
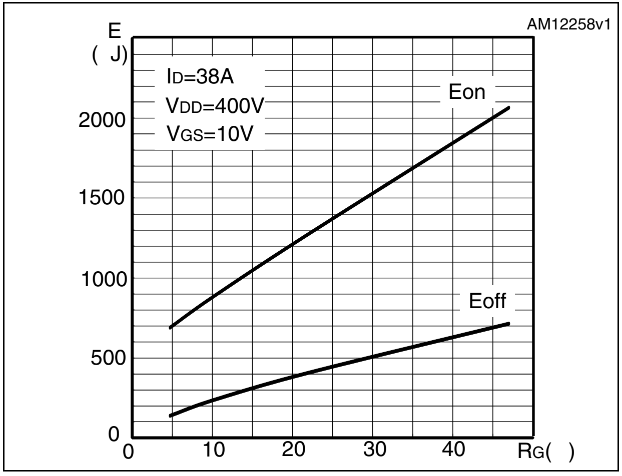


Figure 16. Switching losses vs gate resistance[1]



1. Eon including reverse recovery of a SiC diode

3 Test circuits

Figure 17. Switching times test circuit for resistive load

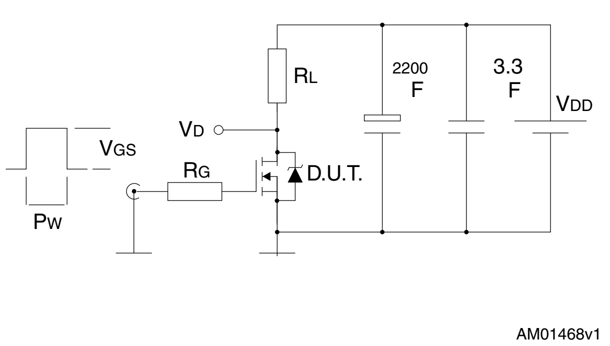


Figure 18. Gate charge test circuit

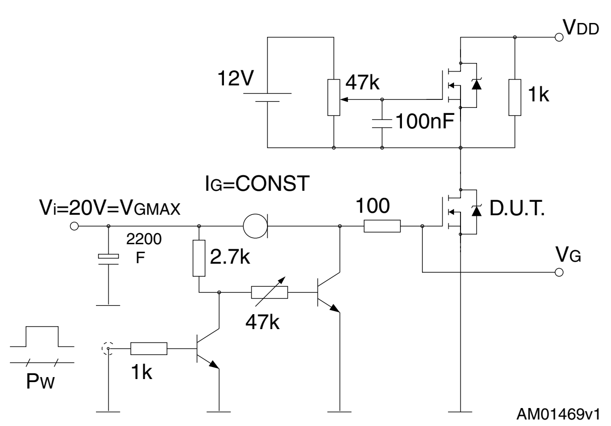


Figure 19. Test circuit for inductive load switching and diode recovery times

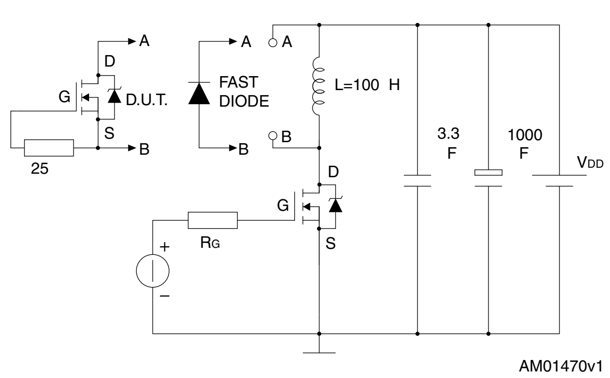


Figure 20. Unclamped inductive load test circuit

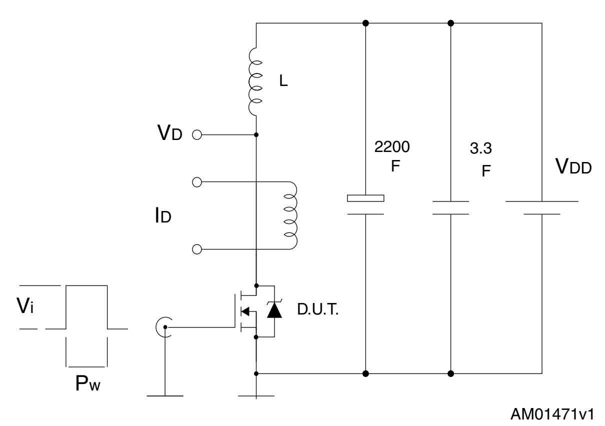


Figure 21. Unclamped inductive waveform

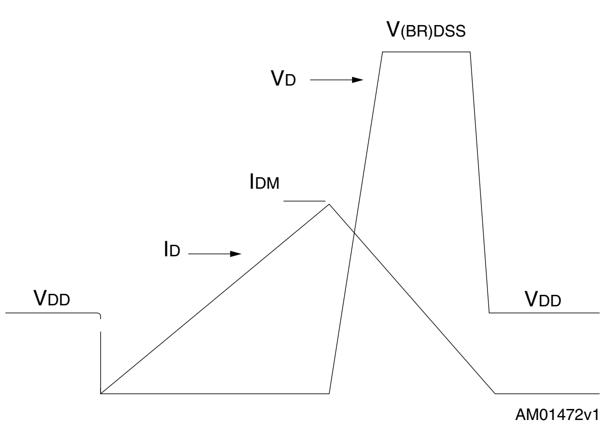
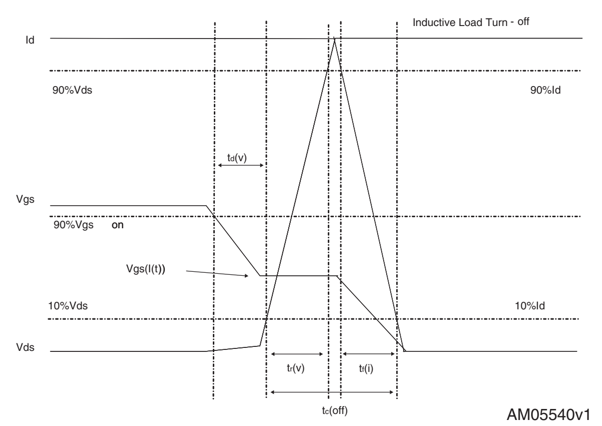


Figure 22. Switching time waveform



4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK® is an ST trademark.

Table 9. TO-3PF mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	5.30		5.70
C	2.80		3.20
D	3.10		3.50
D1	1.80		2.20
E	0.80		1.10
F	0.65		0.95
F2	1.80		2.20
G	10.30		11.50
G1		5.45	
H	15.30		15.70
L	9.80	10	10.20
L2	22.80		23.20
L3	26.30		26.70
L4	43.20		44.40
L5	4.30		4.70
L6	24.30		24.70
L7	14.60		15
N	1.80		2.20
R	3.80		4.20
Dia	3.40		3.80

Figure 23. TO-3PF drawing

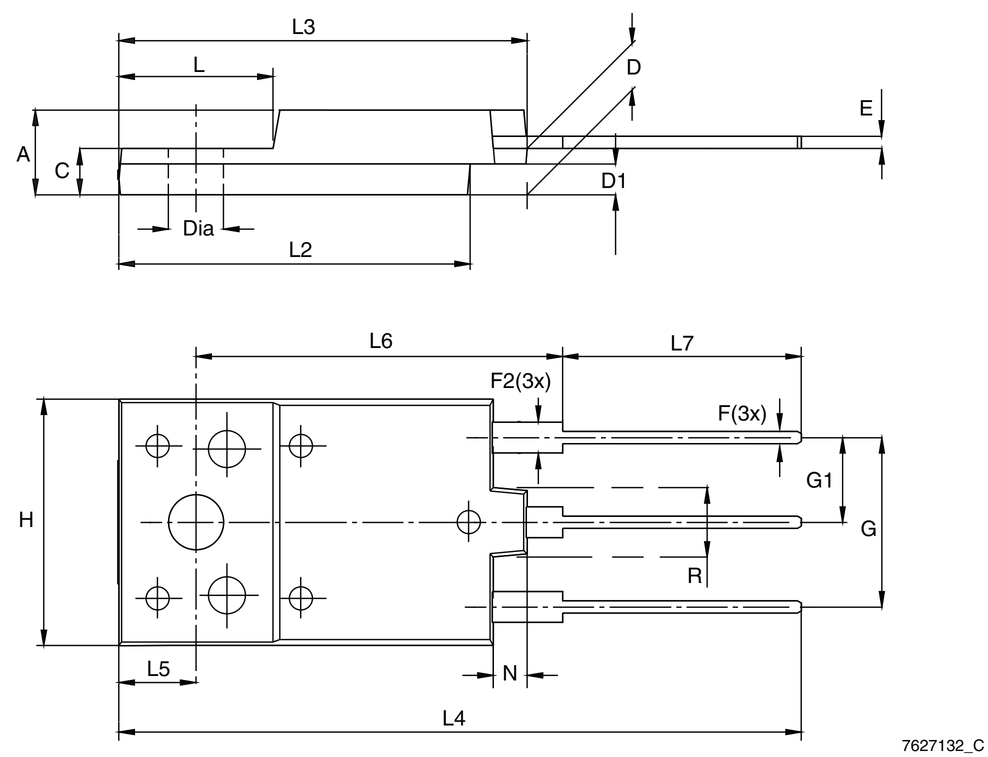
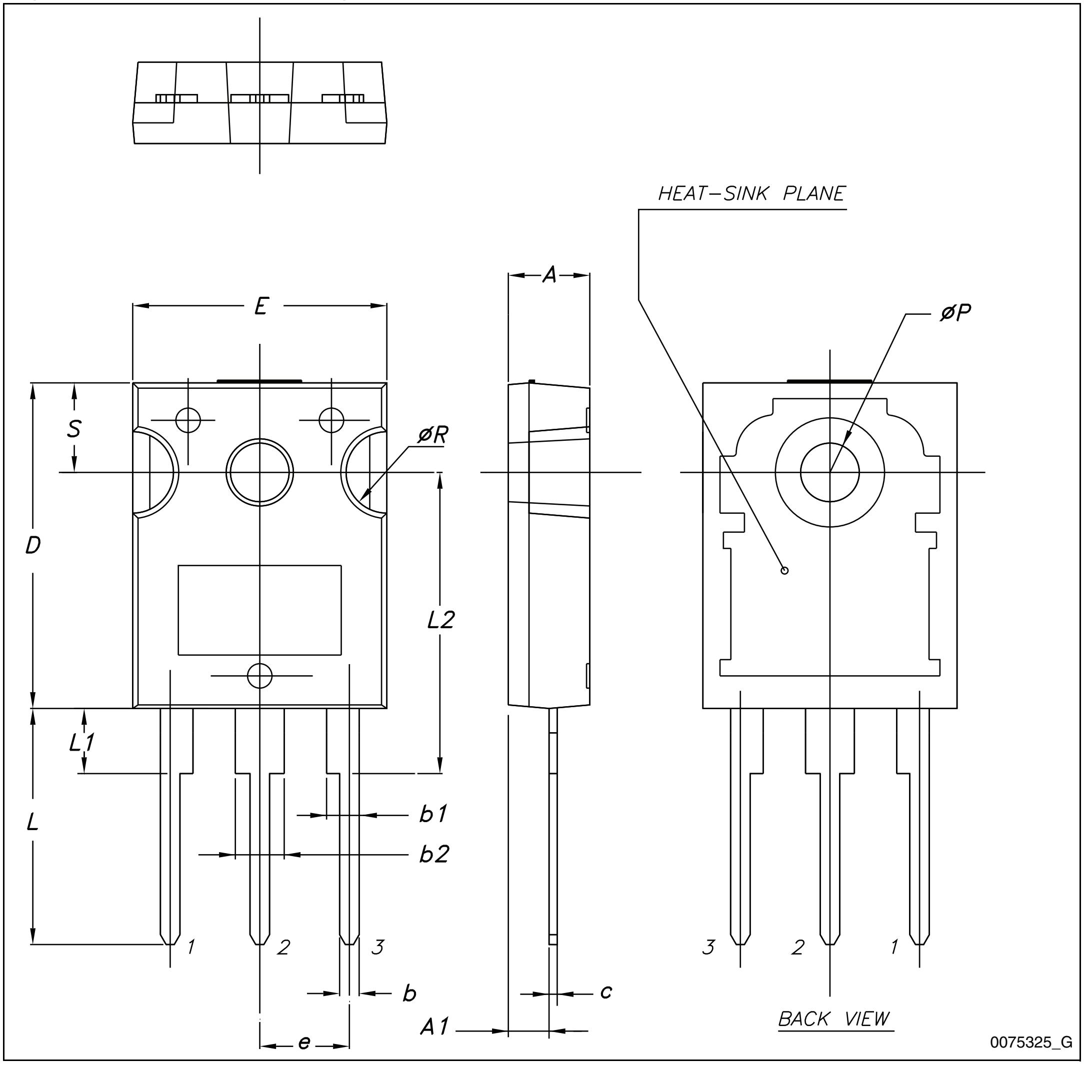


Table 10. TO-247 mechanical data

Dim.	mm.		
	Min.	**Typ.**	**Max.**
A	4.85		5.15
A1	2.20		2.60
b	1.0		1.40
b1	2.0		2.40
b2	3.0		3.40
c	0.40		0.80
D	19.85		20.15
E	15.45		15.75
e	5.30	5.45	5.60
L	14.20		14.80
L1	3.70		4.30
L2		18.50	
∅P	3.55		3.65
∅R	4.50		5.50
S	5.30	5.50	5.70

Figure 24. TO-247 drawing



5 Revision history

Table 11. Document revision history

Date	Revision	Changes
27-Feb-2012	1	First release.
28-Sep-2012	2	– Modified: note *3* of *Table 2*, values in *Table 4*, typ. values in *Table 6*, *7* and *8* – Curves inserted – Minor text changes

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