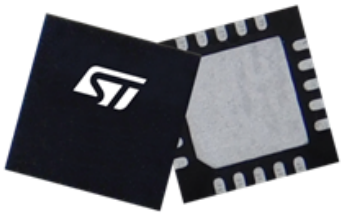
# STG1218

Datasheet

## Dual supply, quad SPDT switch, 1.8 V and 3.3 V logic input compatible



QFN20 (4x4 mm)

## Features

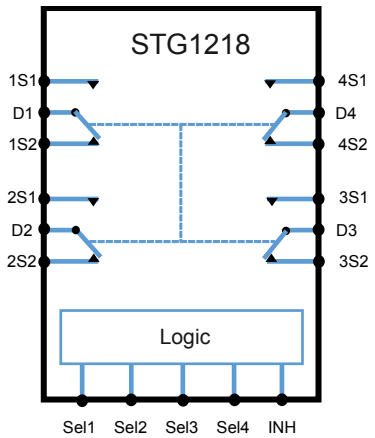
- Wide operating voltage range
  - Total voltage: 2.7 V to 15.5 V
  - Positive supply: 2.7 V to 5.5 V
  - Negative supply: down to -12 V
- Break before make feature
- Quad channel with one control pin for all switches
- Inhibit pin to set the swicthes in high impedance
- Benefits
  - GaN and LDMOS compatible
  - Compatible with 1.8 V and 3.3 V standard logic levels

## Applications

- 5G telecom infrastructure
- Remote radio unit LDMOS and GaN
- Gain selection for instrumentation

## Description

The STG1218 is a quad channel analog switch (SPDT), which is able to accommodate with positive and negative voltages. Each channel has an independent selection pin, and a common inhibit pin. Thanks to its large operating voltage range and low $R_{on}$, this switch can fit many applications such as RRU (both LDMOS and GaN solutions). It is also a good operational amplifier companion chip used with a standard 3.3 V single supply operation for gain selection. In addition, it has the versatility to be compatible with 3.3 V and 1.8 V logic standard thresholds.




SWITCHES SHOWN FOR A 0 INPUT LOGIC

| Product status link |
| --- |
| STG1218 |

# 1 Pin description, block diagram and truth table

## 1.1 Pin description

**Figure 1. Pin connections (top view)**

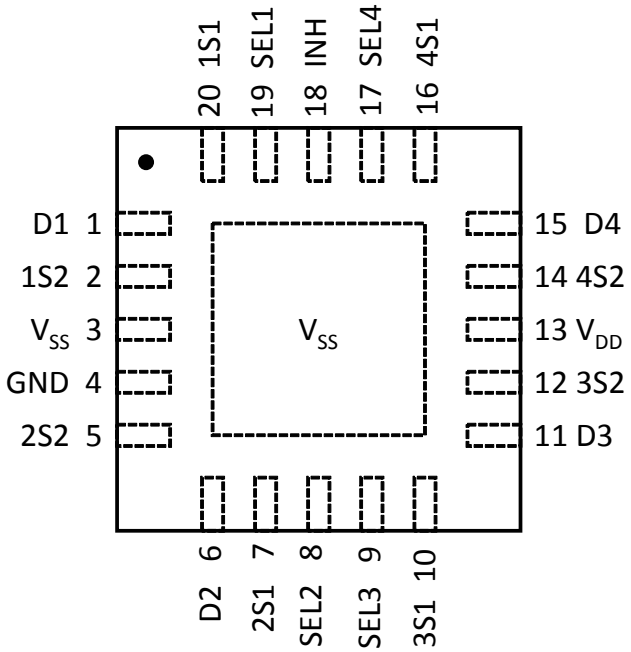
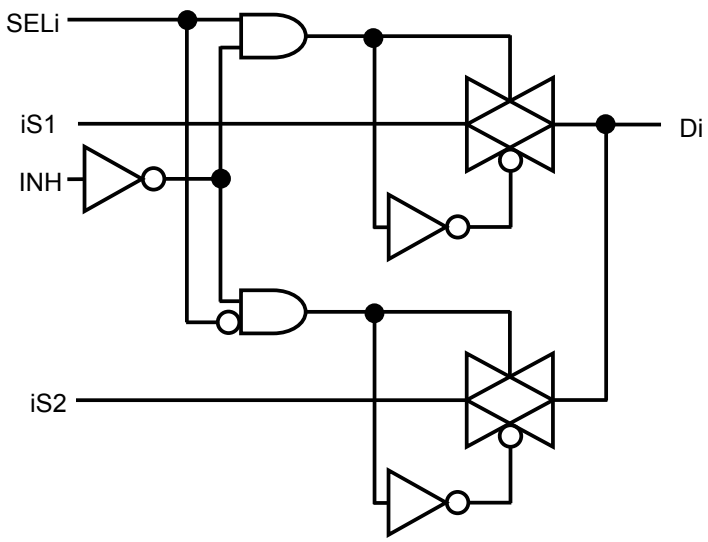



**Table 1. Pin description**

| Pin | Pin name | Description |
|---|---|---|
| 20, 2 | 1S1, 1S2 | Independent inputs / outputs |
| 7, 5 | 2S1, 2S2 | |
| 10, 12 | 3S1, 3S2 | |
| 16, 14 | 4S1, 4S2 | |
| 1, 6, 11, 15 | D1, D2, D3, D4 | Common inputs / outputs |
| 19, 8, 9, 17 | SEL1, SEL2, SEL3, SEL4 | Control pins. Operate only when INH is low.<br>If SELi is high, Di is connected to iS1.<br>If SELi is low, Di is connected to iS2 |
| 18 | INH | Inhibit pin. Set all switches OFF when set to high. Set the switches according to SELi pins when set to low |
| 4 | GND | Ground (0 V) |
| 13 | VDD | Positive supply voltage |
| 3 | VSS | Negative supply voltage |
| Exposed pad | | This pad is electrically connected to VSS |

## 1.2 Block diagram

Figure 2. **Block diagram**




## 1.3 Truth table

Table 2. **Truth table**

| INH | SELi | iS1 | iS2 |
|---|---|---|---|
| L | H | ON(1) | OFF(2) |
| L | L | OFF(2) | ON(1) |
| H | X (3) | OFF(2) | OFF(2) |

1. *Connected to Di*
2. *High impedance*
3. *Do not care*

# 2 Absolute maximum ratings

**Table 3. Absolute maximum ratings**

| Symbol | Parameters[1] | Value | Unit |
|---|---|---|---|
| $V_{DD}$ | Positive supply voltage | -0.3 to 6.0 | V |
| $V_{SS}$ | Negative supply voltage | -13 to 0.3 | V |
| $V_{DD}$ - $V_{SS}$ | Total supply voltage | -0.3 to 16 | V |
| $V_{INH}$ | DC inhibit pin[2] | -0.3 to $V_{DD}$ +0.3 | V |
| $V_{SEL}$ | DC control input voltage[2] | -0.3 to $V_{DD}$ +0.3 | V |
| $V_S$ | DC input voltage (pins iS1, iS2)[2] | $V_{SS}$ -0.3 to $V_{DD}$ +0.3 | V |
| $V_D$ | DC output voltage (pin Di)[2] | $V_{SS}$ -0.3 to $V_{DD}$ +0.3 | V |
| $I_{INH}$ | DC input diode current on INH pin[2] | ±10 | mA |
| $I_{SEL}$ | DC input diode current on SELi pins[2] | ±10 | mA |
| $I_{IK}$ | DC input diode current (pins iS1, iS2)[2] | ±10 | mA |
| $I_{OK}$ | DC output diode current (pin Di)[2] | ±10 | mA |
| $I_O$ | DC output current (pins iS1, iS2, Di), Top = 25 °C | ±150 | mA |
| $I_{OP}$ | Peak output current (pins iS1, iS2, Di)<br>1 ms pulse, 10% duty cycle, Top = 25 °C | ±450 | mA |
| $T_{stg}$ | Storage temperature | -65 to +150 | °C |
| $T_j$ | Maximum junction temperature | 150 | °C |
| $R_{th\text{-}ja}$ | Thermal resistance junction-to-ambient[3] | 45 | °C / W |
| $P_d$ | Continuous power dissipation[4]<br>$T_{op}$ = 70 °C | 1.78 | W |
| ESD | HBM: human body model[5] | 4 | kV |
| | CDM: charged device model[6] | 1.5 | kV |

1. *All voltage values are with respect to ground, unless otherwise specified.*
2. *Voltage and current limited whichever occurs first.*
3. *$R_{th\text{-}ja}$ is a typical value, obtained with PCB according to the standard JEDEC 2s2p without vias.*
4. *The maximum continuous power dissipation is: (150 °C - Top)/$R_{th\text{-}ja}$. In each switch, the power dissipation is $R_{ON}*I^2$, where I is the current through the switch. The overall power dissipation is the sum of the power dissipation in each switch. For example, if $T_{op}$ is 110 °C, considering the max. $R_{ON}$ at the power supply voltage used is 14 Ω, and that you want to source the maximum of current in 3 switches at the same time while the fourth is unused, then this maximum current is :*
   $\sqrt{\frac{Tjmax - Top}{3*Ron*Rthja}} = \sqrt{\frac{150-110}{3*14*45}} = 145mA$
   *In any case, the DC output current condition should be satisfied.*
5. *Human body model: HBM test according to the standard ESDA/JEDEC JS-001-2017.*
6. *Charged device model: CDM test according to the standard AEC-Q100-011.*

**Table 4. Operating conditions**

| Symbol | Parameter | Value |
|---|---|---|
| $V_{DD}$ | Positive supply voltage | 2.7 to 5.5 V |
| $V_{SS}$ | Negative supply voltage | -12 to 0 V |
| $V_{DD}$-$V_{SS}$ | Total supply voltage | 2.7 to 15.5 V |
| $V_S$ | Input voltage (iS1, iS2 pins) | $V_{SS}$ to $V_{DD}$ |
| $V_D$ | Output voltage ($D_i$ pin) | $V_{SS}$ to $V_{DD}$ |
| $V_{INH}$ | Inhibit input voltage | 0 V to $V_{DD}$ |
| $V_{SEL}$ | Control input voltage | 0 V to $V_{DD}$ |
| $T_{op}$ | Operating temperature | -40 to 125 °C |

# 3 Electrical characteristics

$V_{SEL}$ = 0 V or $V_{DD}$, VINH = 0 V, typical characteristics are given at $T_{op}$ = 25 °C and min./max. values cover full temperature range (unless otherwise specified).

**Table 5. DC electrical characteristics**

| Symbol | Parameters and conditions | | Specific conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|---|
| **Digital inputs** | | | | | | | |
| $V_{IH}$ | High level input voltage<br>SELi and INH pins | | 2.7 V < $V_{DD}$ < 5 V | 1.2 | | $V_{DD}$ | V |
| | | | 5 V < $V_{DD}$ < 5.5 V | 1.23 | | $V_{DD}$ | |
| $V_{IL}$ | Low level input voltage<br>SELi and INH pins | | 2.7 V < $V_{DD}$ < 5 V | 0 | | 0.45 | V |
| | | | 5 V < $V_{DD}$ < 5.5 V | 0 | | 0.4 | |
| $I_{IH}$, $I_{IL}$ | Control input leakage current<br>SELi and INH pins, 0 V or $V_{DD}$ | $T_{op}$ = 25 °C | $V_{DD}$ = 5 V, $V_{SS}$ = 0 V | | ±5 | | nA |
| | | | $V_{DD}$ = 3.3 V, $V_{SS}$ = -12 V | | ±5 | | |
| | | | $V_{DD}$ = 3.3 V, $V_{SS}$ = -8 V | | ±5 | | |
| | | $T_{min.}$ < $T_{op}$ < $T_{max.}$ | $V_{DD}$ = 5 V, $V_{SS}$ = 0 V | | | 100 | |
| | | | $V_{DD}$ = 3.3 V, $V_{SS}$ = -12 V | | | 100 | |
| | | | $V_{DD}$ = 3.3 V, $V_{SS}$ = -8 V | | | 100 | |
| **Power supply** | | | | | | | |
| $I_{VDD}$ | Positive quiescent supply current<br>All channels<br>$V_S$ = $V_{SS}$ or $V_{DD}$ | | $V_{DD}$ = 5 V, $V_{SS}$ = 0 V | | 5 | 30 | µA |
| | | | $V_{DD}$ = 3.3 V, $V_{SS}$ = -12 V | | 5 | 30 | |
| | | | $V_{DD}$ = 3.3 V, $V_{SS}$ = -8 V | | 5 | 30 | |
| $I_{VSS}$ | Negative quiescent supply current<br>All channels<br>$V_S$ = $V_{SS}$ or $V_{DD}$ | | $V_{DD}$ = 5 V, $V_{SS}$ = 0 V | | 0.01 | 20 | µA |
| | | | $V_{DD}$ = 3.3 V, $V_{SS}$ = -12 V | | 0.01 | 20 | |
| | | | $V_{DD}$ = 3.3 V, $V_{SS}$ = -8 V | | 0.01 | 20 | |
| **Switch** | | | | | | | |
| $R_{ONpeak}$ | Max. switch ON-resistance<br>$V_S$ = $V_{SS}$ to $V_{DD}$, I = 10 mA | | $V_{DD}$ = 5 V, $V_{SS}$ = -10.5 V | | 3.6 | 7.5 | Ω |
| | | | $V_{DD}$ = 5 V, $V_{SS}$ = 0 V | | 6.4 | 14 | |
| | | | $V_{DD}$ = 4.5 V, $V_{SS}$ = 0 V | | 7 | 14 | |
| | | | $V_{DD}$ = 3 V, $V_{SS}$ = -12 V | | 3.7 | 8 | |
| | | | $V_{DD}$ = 3 V, $V_{SS}$ = -10 V | | 3.9 | 8 | |
| | | | $V_{DD}$ = 3 V, $V_{SS}$ = -8 V | | 4.2 | 8 | |
| $R_{FLATON}$ | ON-resistance flatness<br>$V_S$ = $V_{SS}$ to $V_{DD}$, I = 10 mA | | $V_{DD}$ = 5 V, $V_{SS}$ = -10.5 V | | 1 | 4.2 | Ω |
| | | | $V_{DD}$ = 5 V, $V_{SS}$ = 0 V | | 1.2 | 5 | |
| | | | $V_{DD}$ = 4.5 V, $V_{SS}$ = 0 V | | 1.2 | 5.4 | |
| | | | $V_{DD}$ =3 V, $V_{SS}$ = -12 V | | 1 | 4.3 | |
| | | | $V_{DD}$ = 3 V, $V_{SS}$ = -10 V | | 1 | 4.7 | |
| | | | $V_{DD}$ = 3 V, $V_{SS}$ = -8 V | | 1 | 4.8 | |

| Symbol | Parameters and conditions | Specific conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $\Delta R_{ON}$ | ON-resistance mismatch<br>Max. delta between 8 $R_{on}$ values of the device (4 channels x 2 positions)<br>$V_S$ = $V_{SS}$ to $V_{DD}$, I = 10 mA | $V_{DD}$ = 5 V, $V_{SS}$ = -10.5 V | | 0.3 | 0.5 | Ω |
| | | $V_{DD}$ = 5 V, $V_{SS}$ = 0 V | | 0.3 | 0.5 | |
| | | $V_{DD}$ = 4.5 V, $V_{SS}$ = 0 V | | 0.3 | 0.5 | |
| | | $V_{DD}$ = 3 V, $V_{SS}$ = -12 V | | 0.3 | 0.5 | |
| | | $V_{DD}$ = 3 V, $V_{SS}$ = -10V | | 0.3 | 0.5 | |
| | | $V_{DD}$ = 3 V, $V_{SS}$ = -8 V | | 0.3 | 0.5 | |
| $\Delta R_{ON}/\Delta T$ | ON-resistance temperature coefficient<br>(worst case between $T_{min.}$ to 25 °C and 25 °C to $T_{max.}$ considered)<br>$V_S$ = $V_{SS}$ to $V_{DD}$, I = 10 mA | $V_{DD}$ = 5 V, $V_{SS}$ = -10.5 V | | 16 | | mΩ/°C |
| | | $V_{DD}$ = 5 V, $V_{SS}$ = 0 V | | 28 | | |
| | | $V_{DD}$ = 4.5 V, $V_{SS}$ = 0 V | | 30 | | |
| | | $V_{DD}$ = 3 V, $V_{SS}$ = -12 V | | 16 | | |
| | | $V_{DD}$ = 3 V, $V_{SS}$ = -10V | | 18 | | |
| | | $V_{DD}$ = 3 V, $V_{SS}$ = -8 V | | 19 | | |
| $I_{SOFF}$ | $S_n$ OFF leakage current<br>$V_D$ = $V_{SS}$ to $V_{DD}$, $V_S$ = $V_{SS}$ to $V_{DD}$<br>$V_{SEL}$ = 0 V for iS1, $V_{SEL}$ = $V_{DD}$ for iS2 | $V_{DD}$ = 5 V, $V_{SS}$ = 0 V | | 0.001 | 1.5 | µA |
| | | $V_{DD}$ = 3.3 V, $V_{SS}$ = -12 V | | 0.001 | 1.5 | |
| | | $V_{DD}$ = 3.3 V, $V_{SS}$ = -8 V | | 0.001 | 1.5 | |
| $I_{DOFF}$ | DOFF leakage current<br>$V_D$ = $V_{SS}$ to $V_{DD}$, $V_S$ = $V_{SS}$ to $V_{DD}$<br>$V_{SEL}$ = 0 V for iS1, $V_{SEL}$ = $V_{DD}$ for iS2 | $V_{DD}$ = 5 V, $V_{SS}$ = 0 V | | 0.001 | 2.5 | µA |
| | | $V_{DD}$ = 3.3 V, $V_{SS}$ = -12 V | | 0.001 | 2.5 | |
| | | $V_{DD}$ = 3.3 V, $V_{SS}$ = -8 V | | 0.001 | 2.5 | |
| $I_{DON}$ | DON leakage current<br>$V_D$ = $V_{SS}$ to $V_{DD}$, $V_S$ = $V_{SS}$ to $V_{DD}$,<br>$V_{SEL}$ = 0 V for iS2, $V_{SEL}$ = $V_{DD}$ for iS2 | $V_{DD}$ = 5 V, $V_{SS}$ = 0 V | | 0.001 | 1.5 | µA |
| | | $V_{DD}$ = 3.3 V, $V_{SS}$ = -12 V | | 0.001 | 1.5 | |
| | | $V_{DD}$ = 3.3 V, $V_{SS}$ = -8 V | | 0.001 | 1.5 | |

VINH = 0 V, typical characteristics are given at $T_{op}$ = 25 °C and min./max. values cover full temperature range (unless otherwise specified).

**Table 6. AC electrical characteristics**

| Symbol | Parameters and conditions | Specific conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $t_{PLH}$, $t_{PHL}$ | Propagation delay<br>$V_{SEL}$ = 0 V for iS2,<br>$V_{SEL}$ = $V_{DD}$ for iS1<br>$V_S$ square 0 V to 1.5 V<br>when $V_{ss}$ = 0 V,<br>$V_S$ square 0 V to -2.5 V when $V_{ss}$ < 0 V,<br>$R_L$ = 50 Ω, $C_L$ = 50 pF, 50% to 50% | $V_{DD}$ = 5 V, $V_{SS}$ = 0 V | | 0.8 | | ns |
| | | $V_{DD}$ = 3.3 V, $V_{SS}$ = -12 V | | 0.7 | | |
| | | $V_{DD}$ = 3.3 V, $V_{SS}$ = -8 V | | 0.7 | | |
| $t_{ONS1}$ (SEL) | Turn ON S1 time SEL pin<br>$V_{S1}$ = $V_{SS}$ or $V_{DD}$,<br>$V_{S2}$ floating<br>$V_{SEL}$ step 0 V to $V_{DD}$<br>$R_L$ = 300 Ω, $C_L$ = 20 pF, 50% to 90% of $V_{S1}$ | $V_{DD}$ = 5 V, $V_{SS}$ = 0 V | 105 | 162 | 320 | ns |
| | | $V_{DD}$ = 3.3 V, $V_{SS}$ = -12 V | 160 | 255 | 490 | |
| | | $V_{DD}$ = 3.3 V, $V_{SS}$ = -8 V | 160 | 255 | 490 | |
| $t_{ONS2}$ (SEL) | Turn ON S2 time SEL pin<br>$V_{S2}$ = $V_{SS}$ or $V_{DD}$,<br>$V_{S1}$ floating<br>$V_{SEL}$ step $V_{DD}$ to 0 V<br>$R_L$ = 300 Ω, $C_L$ = 20 pF 50% to 90% of $V_{S2}$ | $V_{DD}$ = 5 V, $V_{SS}$ = 0 V | 370 | 555 | 855 | ns |
| | | $V_{DD}$ = 3.3 V, $V_{SS}$ = -12 V | 390 | 556 | 815 | |
| | | $V_{DD}$ = 3.3 V, $V_{SS}$ = -8 V | 390 | 555 | 810 | |
| $t_{OFFS1}$ (SEL) | Turn OFF S1 time SEL pin<br>$V_{S1}$= $V_{SS}$ or $V_{DD}$,<br>$V_{S2}$ floating<br>$V_{SEL}$ step $V_{DD}$ to 0 V<br>$R_L$ = 300 Ω, $C_L$ = 20 pF 50% to 90% of $V_{S1}$ | $V_{DD}$ = 5 V, $V_{SS}$ = 0 V | 310 | 501 | 850 | ns |
| | | $V_{DD}$ = 3.3 V, $V_{SS}$ = -12 V | 285 | 455 | 700 | |
| | | $V_{DD}$ = 3.3 V, $V_{SS}$ = -8 V | 285 | 455 | 700 | |
| $t_{OFFS2}$ (SEL) | Turn OFF S2 time SEL pin<br>$V_{S2}$= $V_{SS}$ or $V_{DD}$,<br>$V_{S1}$ floating<br>$V_{SEL}$ step 0 V to $V_{DD}$,<br>$R_L$ = 300 Ω, $C_L$ = 20 pF 50% to 90% of $V_{S2}$ | $V_{DD}$ = 5 V, $V_{SS}$ = 0 V | 70 | 100 | 195 | ns |
| | | $V_{DD}$ = 3.3 V, $V_{SS}$ = -12 V | 100 | 155 | 290 | |
| | | $V_{DD}$ = 3.3 V, $V_{SS}$ = -8 V | 100 | 152 | 290 | |
| $t_{ONS1}$ (SEL) Skew | Turn ON time SEL pin skew max. ($t_{ONiS1}$) -min.($t_{ONiS1}$) | $V_{DD}$ = 5 V, $V_{SS}$ = 0 V | | 2 | | ns |
| | | $V_{DD}$ = 3.3 V, $V_{SS}$ = -12 V | | 3 | | |
| | | $V_{DD}$ = 3.3 V, $V_{SS}$ = -8 V | | 3 | | |

| Symbol | Parameters and conditions | Specific conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $t_{ONS2}$ (SEL) Skew | Turn ON time SEL pin skew max.($t_{ONiS2}$) -min.($t_{ONiS2}$) | $V_{DD}$ = 5 V, $V_{SS}$ = 0 V | | 87 | | ns |
| | | $V_{DD}$ = 3.3 V, $V_{SS}$ = -12 V | | 59 | | |
| | | $V_{DD}$ = 3.3 V, $V_{SS}$ = -8 V | | 59 | | |
| $t_{OFFS1}$ (SEL) Skew | Turn OFF time SEL pin skew max.($t_{OFFiS1}$) -min.($t_{OFFiS1}$) | $V_{DD}$ = 5 V, $V_{SS}$ = 0 V | | 89 | | ns |
| | | $V_{DD}$ = 3.3 V, $V_{SS}$ = -12 V | | 63 | | |
| | | $V_{DD}$ = 3.3 V, $V_{SS}$ = -8 V | | 63 | | |
| $t_{OFFS2}$ (SEL) Skew | Turn OFF time SEL pin skew max.($t_{OFFiS2}$)-min.($t_{OFFiS2}$) | $V_{DD}$ = 5 V, $V_{SS}$ = 0 V | | 1 | | |
| | | $V_{DD}$ = 3.3 V, $V_{SS}$ = -12 V | | 1 | | |
| | | $V_{DD}$ = 3.3 V, $V_{SS}$ = -8 V | | 1 | | |
| $t_{ONS1}$ (INH) | Turn ON time INH pin<br>$V_S$ = $V_{SS}$ or $V_{DD}$<br>$V_{SEL}$ = $V_{DD}$<br>$V_{INH}$ step $V_{DD}$ to 0 V,<br>$R_L$ = 300 Ω, $C_L$ = 20 pF,<br>50% to 90% of $V_S$ | $V_{DD}$ = 5 V, $V_{SS}$ = 0 V | 270 | 710 | 915 | ns |
| | | $V_{DD}$ = 3.3 V, $V_{SS}$ = -12 V | 180 | 665 | 750 | |
| | | $V_{DD}$ = 3.3 V, $V_{SS}$ = -8 V | 270 | 660 | 930 | |
| $t_{ONS2}$ (INH) | Turn ON time INH pin<br>$V_S$ = $V_{SS}$ or $V_{DD}$<br>$V_{SEL}$ = 0 V<br>$V_{INH}$ step $V_{DD}$ to 0 V,<br>$R_L$ = 300 Ω, $C_L$ = 20 pF,<br>50% to 90% of $V_S$ | $V_{DD}$ = 5 V, $V_{SS}$ = 0 V | 270 | 563 | 915 | |
| | | $V_{DD}$ = 3.3 V, $V_{SS}$ = -12 V | 180 | 415 | 620 | |
| | | $V_{DD}$ = 3.3 V, $V_{SS}$ = -8 V | 245 | 415 | 915 | |
| $t_{OFF}$ (INH) | Turn OFF time INH pin<br>$V_S$ = $V_{SS}$ or $V_{DD}$<br>$V_{SEL}$ = 0 V for iS2,<br>$V_{SEL}$ = $V_{DD}$ for IS1,<br>$V_{INH}$ step $V_{DD}$ to 0 V,<br>$R_L$ = 300 Ω, $C_L$ = 20 pF,<br>50% to 90% of $V_S$ | $V_{DD}$ = 5 V, $V_{SS}$ = 0 V | 25 | 37 | 65 | ns |
| | | $V_{DD}$ = 3.3 V, $V_{SS}$ = -12 V | 25 | 34 | 65 | |
| | | $V_{DD}$ = 3.3 V, $V_{SS}$ = -8 V | 25 | 33 | 65 | |
| $t_D$ | Break before make time delay,<br>$V_{SEL}$ step 0 V to $V_{DD}$<br>20 pF//300 Ω,<br>90% to 90% | $V_{DD}$ = 5 V, $V_{SS}$ = 0 V,<br>$V_S$ = 1.5 V | 35 | 62 | 115 | ns |
| | | $V_{DD}$ = 3.3 V, $V_{SS}$ = -12 V,<br>$V_S$ = 2.5 V | 60 | 108 | 200 | |
| | | $V_{DD}$ = 3.3 V, $V_{SS}$ = -8 V,<br>$V_S$ = 2.5 V | 60 | 109 | 200 | |
| Q | Charge injection<br>$C_L$ =1 nF, $R_L$ = 1 MΩ,<br>f = 500 kHz, iS1 = 0 V, iS2 floating<br>$V_{SEL}$ step 0 V to $V_{DD}$ square waveform, or<br>iS1 floating, iS2 = 0 V | $V_{DD}$ = 5 V, $V_{SS}$ = 0 V | | 48 | | pC |
| | | $V_{DD}$ = 3.3 V, $V_{SS}$ = -12 V | | 220 | | |
| | | $V_{DD}$ = 3.3 V, $V_{SS}$ = -8 V | | 140 | | |

| Symbol | Parameters and conditions | Specific conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| Q | $V_{SEL}$ step $V_{DD}$ to 0 V square waveform | | | | | pC |
| $C_{SOFF}$ | OFF channel capacitance<br>$V_{SEL}$ = 0 V for iS1 capacitance<br>$V_{SEL}$ = $V_{DD}$ for iS2 capacitance | $V_{DD}$ = 5 V, $V_{SS}$ = 0 V | | 25 | | pF |
| | | $V_{DD}$ = 3.3 V, $V_{SS}$ = -12 V | | 16 | | |
| | | $V_{DD}$ = 3.3 V, $V_{SS}$ = -8 V | | 18 | | |
| $C_{SON}$, $C_{DON}$ | ON channel capacitance<br>$V_{SEL}$ = 0 V for iS2 capacitance<br>$V_{SEL}$ = $V_{DD}$ for iS1 capacitance<br>$V_{SEL}$ = 0 V or $V_{DD}$ for D capacitance | $V_{DD}$ = 5 V, $V_{SS}$ = 0 V | | 66 | | pF |
| | | $V_{DD}$ = 3.3 V, $V_{SS}$ = -12 V | | 62 | | |
| | | $V_{DD}$ = 3.3 V, $V_{SS}$ = -8 V | | 57 | | |
| OIRR | OFF isolation<br>20log($V_D$/$V_S$)<br>$V_{SEL}$ = 0 V and 50 Ω on iS1 for iS1 test,<br>$V_{SEL}$ = $V_{DD}$ and 50 Ω on iS2 for iS2 test,<br>$R_L$ = 50 Ω, $C_L$ = 5 pF,<br>$V_S$ = 1 $V_{rms}$, f = 1 MHz<br>For those cases with $V_{ss}$ = 0 V a DC bias is added to AC signal and set to $V_{DD}$/2 | $V_{DD}$ = 5 V, $V_{SS}$ = 0 V | | -66 | | dB |
| | | $V_{DD}$ = 3.3 V, $V_{SS}$ = -12 V | | -66 | | |
| | | $V_{DD}$ = 3.3 V, $V_{SS}$ = -8 V | | -66 | | |
| $X_{talk}$ | Crosstalk<br>20log($V_{Si}$/$V_{Sj}$)<br>$V_{SEL}$ = 0 V and 50 Ω on iS1 for iS2 test,<br>$V_{SEL}$ = $V_{DD}$ and 50 Ω on iS2 for iS1 test,<br>$R_L$ = 50 Ω, $C_L$ = 5 pF,<br>$V_S$ = 1 $V_{rms}$, f = 1 MHz<br>For those cases with $V_{ss}$ = 0 V a DC bias is added to AC signal and set to $V_{DD}$/2 | $V_{DD}$ = 5 V, $V_{SS}$ = 0 V | | -66 | | dB |
| | | $V_{DD}$ = 3.3 V, $V_{SS}$ = -12 V | | -66 | | |
| | | $V_{DD}$ = 3.3 V, $V_{SS}$ = -8 V | | -66 | | |
| $B_W$ | -3 dB bandwidth<br>$V_{SEL}$ = 0 V for iS2 test,<br>$V_{SEL}$ = $V_{DD}$ for iS1 test,<br>$R_L$ = 50 Ω, $C_L$ = 5 pF,<br>$V_S$ = 0 dBm<br>For those cases with $V_{ss}$ = 0 V a DC bias is added to AC signal and set to $V_{DD}$/2 | $V_{DD}$ = 5 V, $V_{SS}$ = 0 V | 150 | 200 | | MHz |
| | | $V_{DD}$ = 3.3 V, $V_{SS}$ = -12 V | 150 | 200 | | |
| | | $V_{DD}$ = 3.3 V, $V_{SS}$ = -8 V | 150 | 200 | | |

# 4 Electrical characteristics curves

**Figure 3. ON-resistance vs. S or D voltage for different power supply voltage**

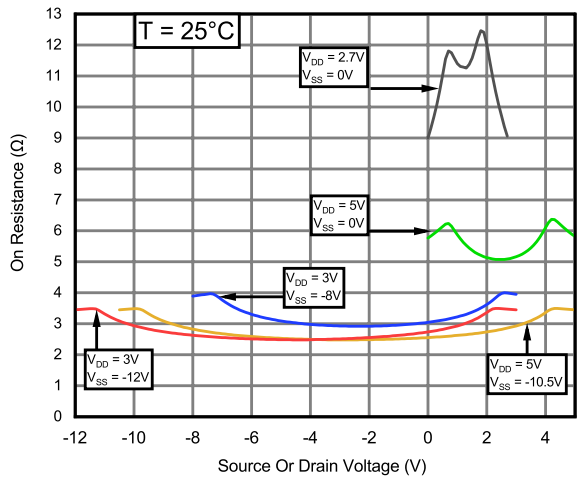



**Figure 4. ON-resistance vs. power supply voltage**

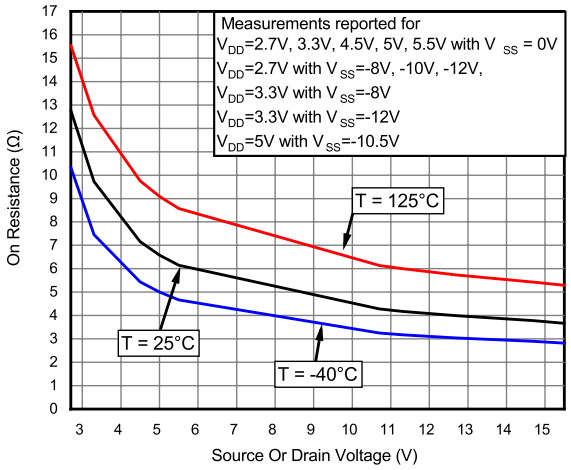



**Figure 5. ON-resistance vs. S or D voltage for $V_{DD}$ / $V_{SS}$ = 4.5 V/0 V**

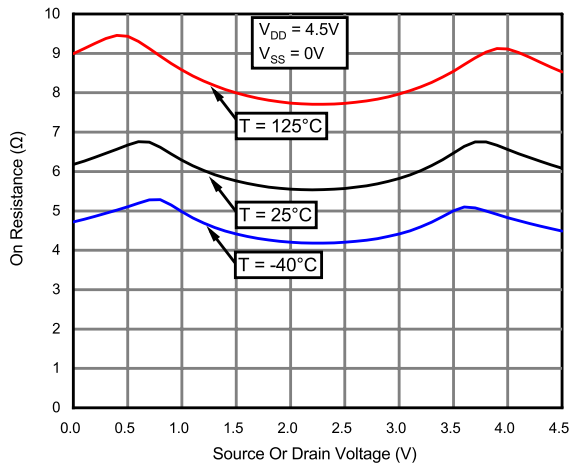



**Figure 6. ON-resistance vs. S or D voltage for $V_{DD}$ / $V_{SS}$ = 5 V/0 V**

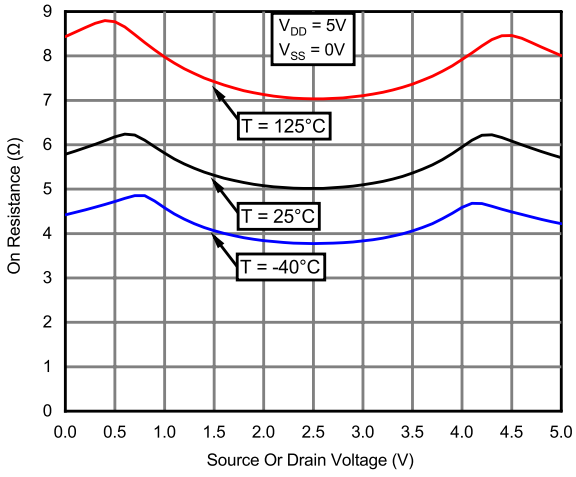


**Figure 7. ON-resistance vs. S or D voltage for $V_{DD}$/ $V_{SS}$ = 3 V/-8 V**

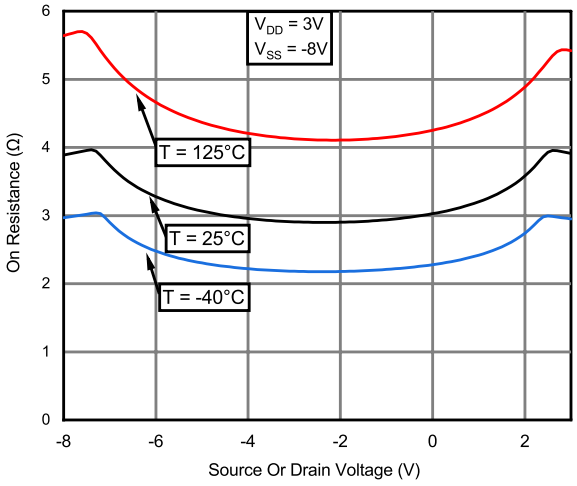



**Figure 8. ON-resistance vs. S or D voltage for $V_{DD}$/ $V_{SS}$ = 3 V/-12 V**

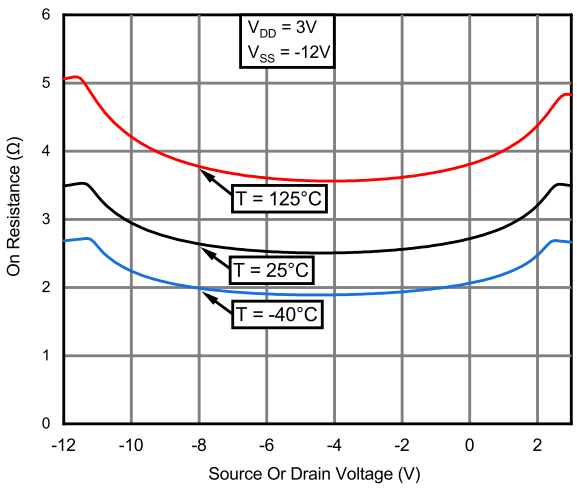



**Figure 9. ON-resistance vs. S or D voltage for $V_{DD}$/ $V_{SS}$ = 5 V/-10.5 V**

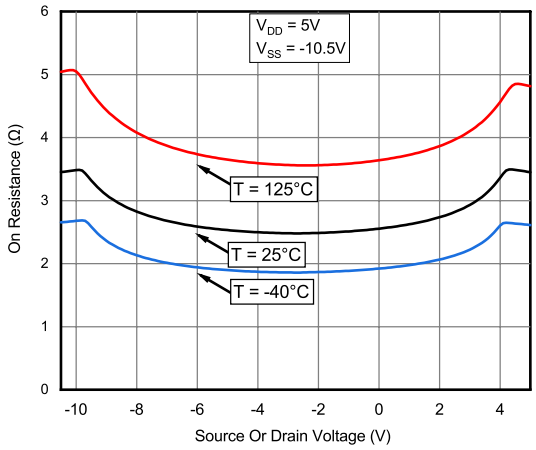



**Figure 10. $I_{DD}$ vs. logic voltage at 25 °C, $V_{Select}$ swept for two switches, the two others left grounded**

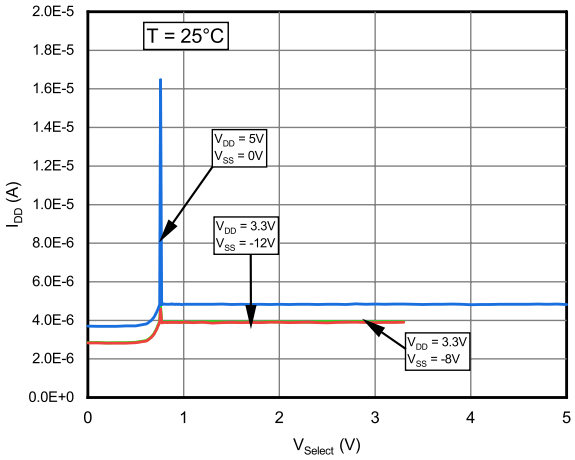


**Figure 11. $I_{SS}$ vs. logic voltage at 25 °C, $V_{Select}$ swept for two switches, the two others left grounded**

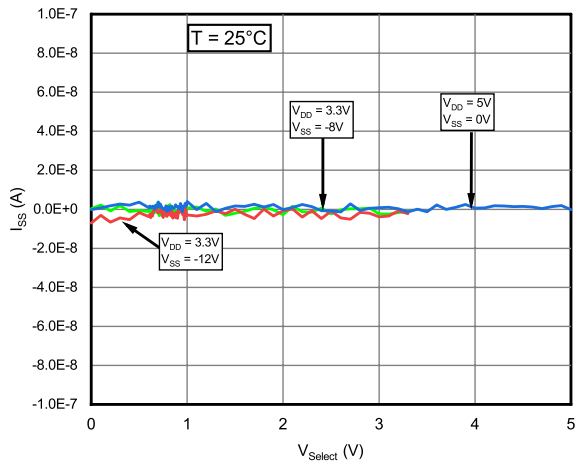



**Figure 12. $I_{DD}$ vs. logic voltage at -40 °C, $V_{Select}$ swept for two switches, the two others left grounded**

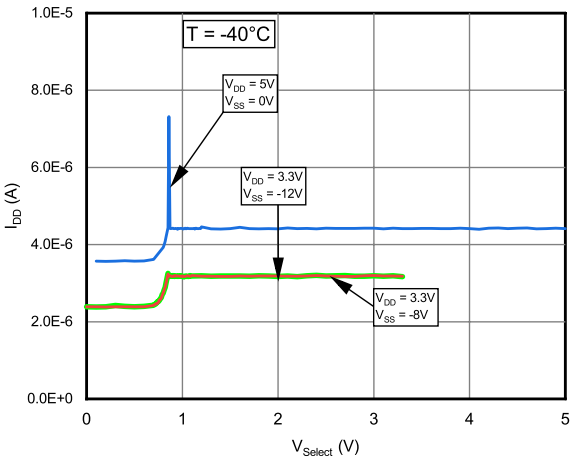



**Figure 13. $I_{SS}$ vs. logic voltage at -40 °C, $V_{Select}$ swept for two switches, the two others left grounded**

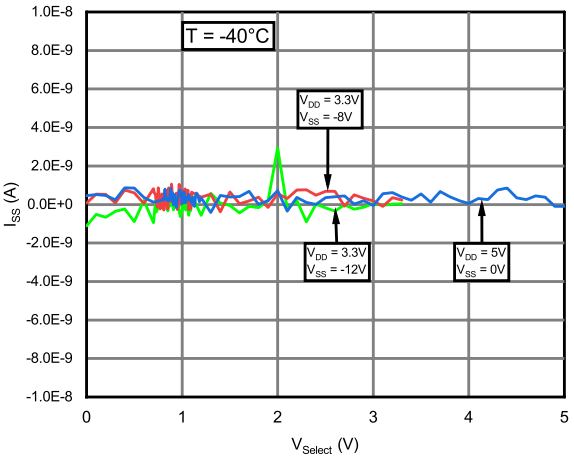



**Figure 14. $I_{DD}$ vs. logic voltage at 125 °C, $V_{Select}$ swept for two switches, the two others left grounded**

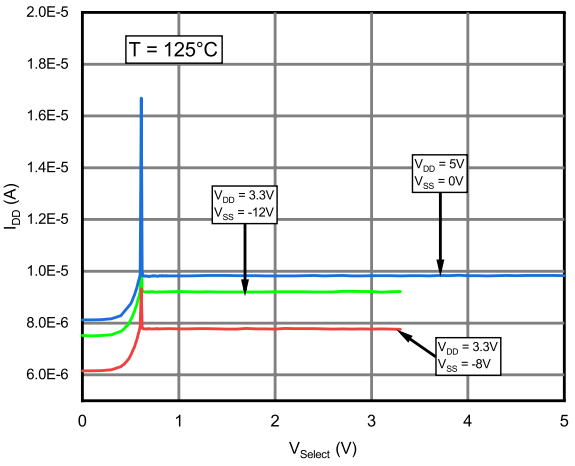


**Figure 15. $I_{SS}$ vs. logic voltage at 125 °C, $V_{Select}$ swept for two switches, the two others left grounded**

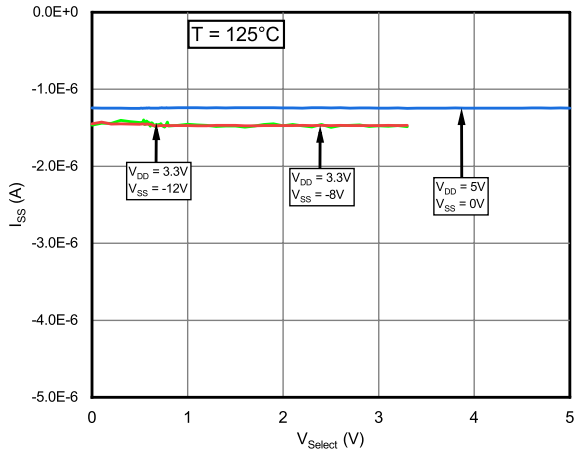



**Figure 16. Leakage currents at 25 °C**

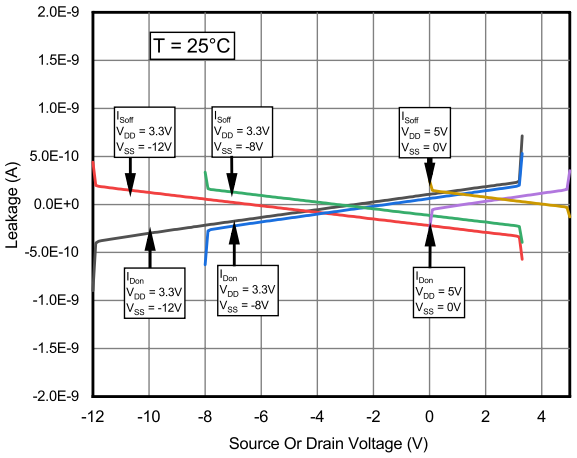



**Figure 17. Leakage currents at -40 °C**

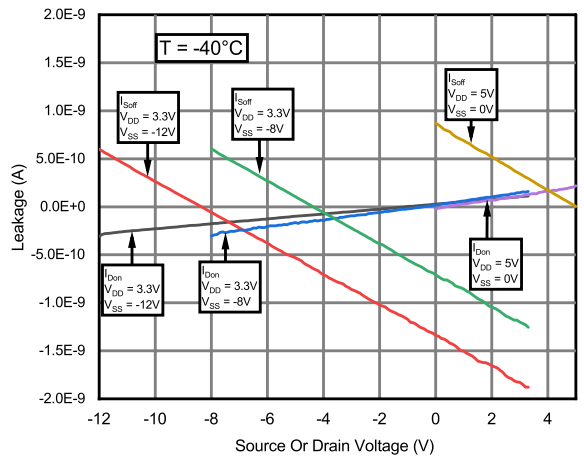



**Figure 18. Leakage currents at 125 °C**

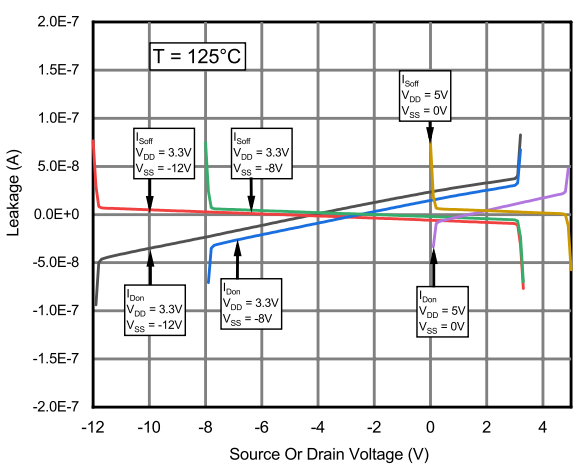


**Figure 19. $T_{ONS1}$(SEL) vs. temperature**

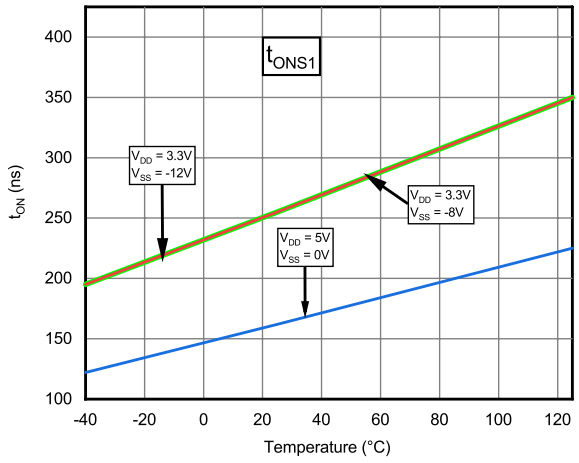



**Figure 20. $T_{ONS2}$(SEL) vs. temperature**

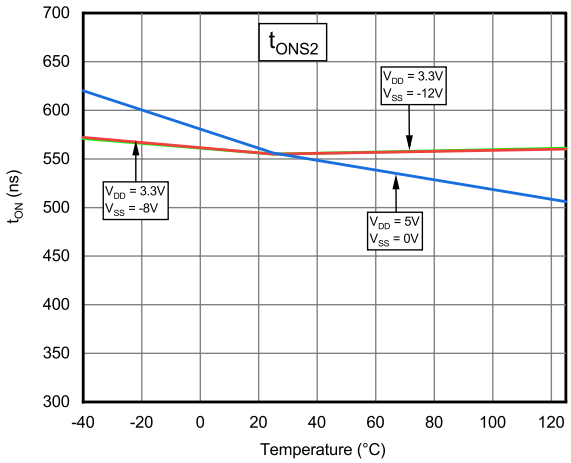



**Figure 21. $T_{OFFS1}$(SEL) vs. temperature**

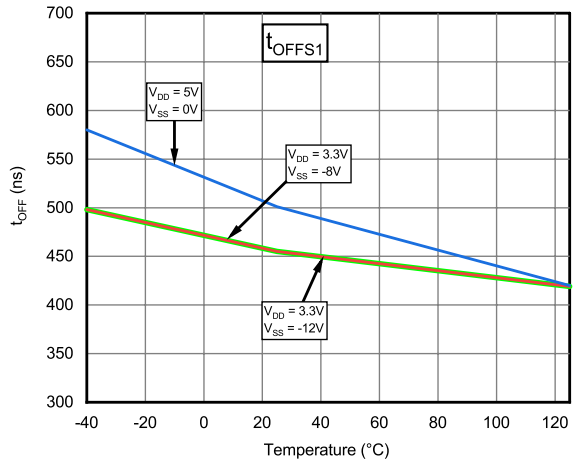



**Figure 22. $T_{OFFS2}$(SEL) vs. temperature**

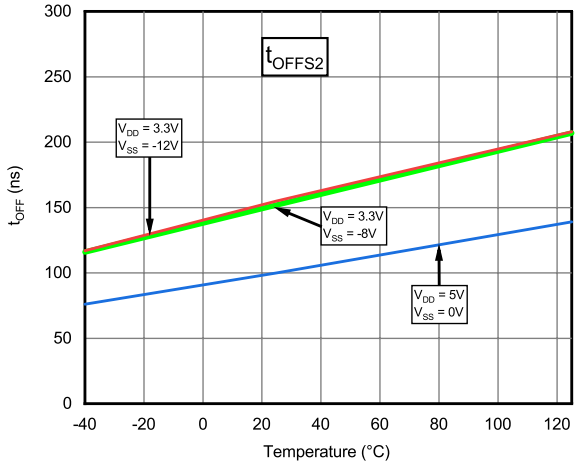



**Figure 23. Bandwidth**

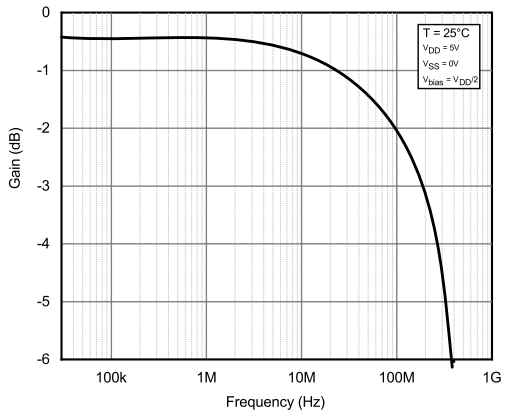



**Figure 24. OFF isolation**

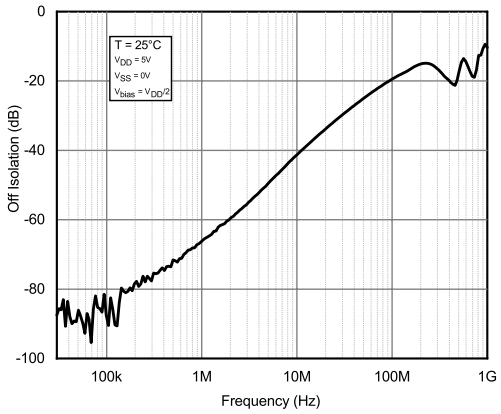
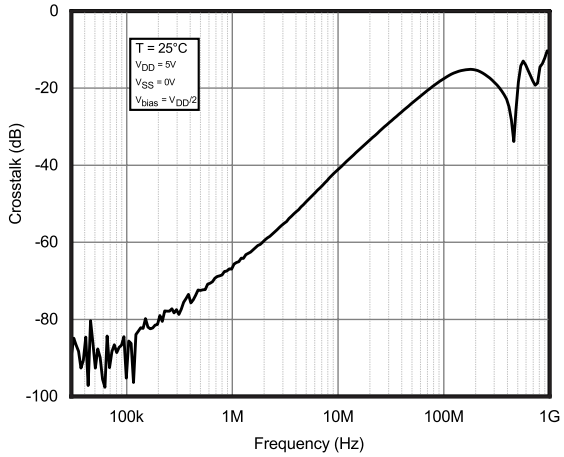


Figure 25. **Crosstalk**



# 5 Test circuits

Figure 26. **Input threshold voltage test circuit**

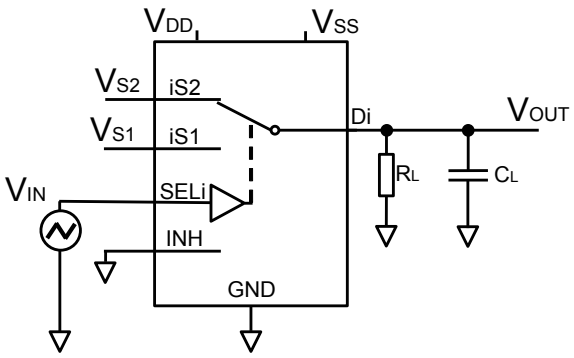



Figure 27. **Input threshold**

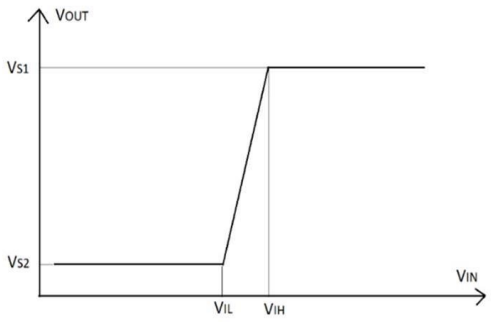



Figure 28. **Control input leakage current test circuit**

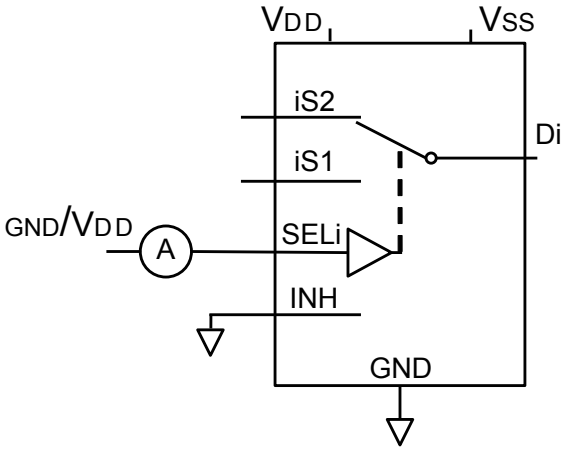



Figure 29. **ON-resistance, flatness and mismatch test circuit**

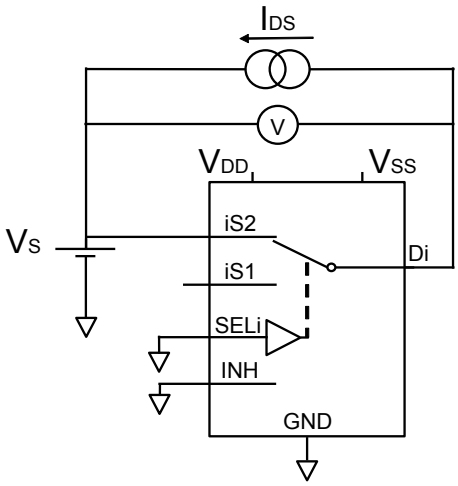



Figure 30. **OFF and ON leakage currents test circuit**

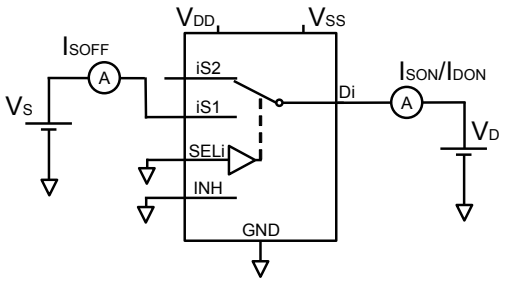



Figure 31. **OFF leakage current test circuit**

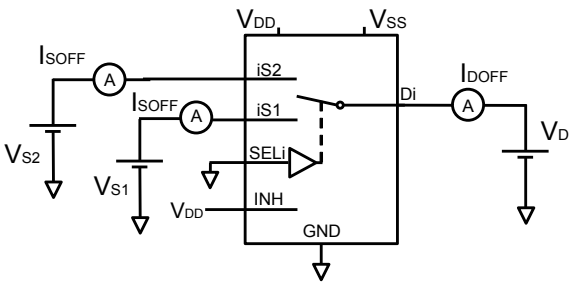


**Figure 32. Propagation delay test circuit**

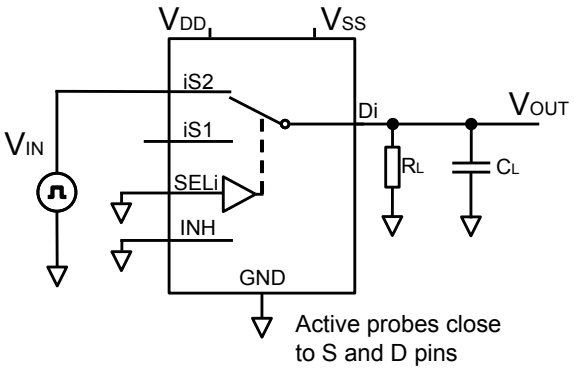



**Figure 33. Propagation delay timing**

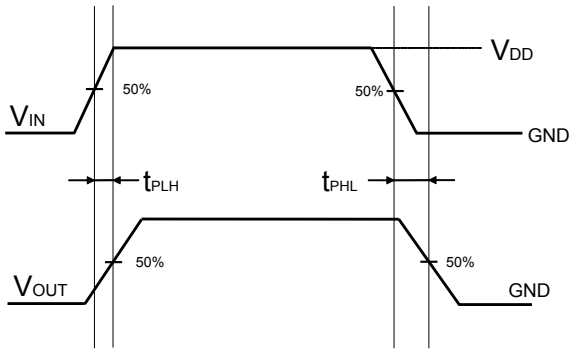



**Figure 34. Turn-on time, turn-off time and skew on SEL pin and charge injection test circuit**

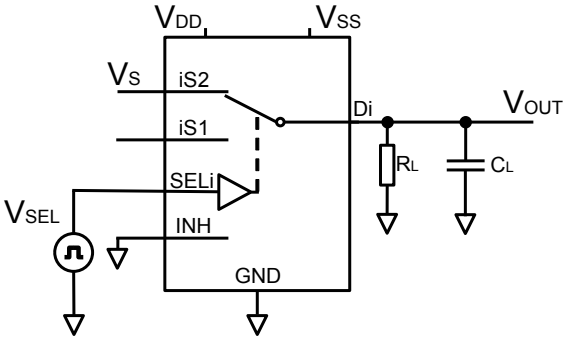



**Figure 35. Turn-on time and turn-off time on SEL pin timing**

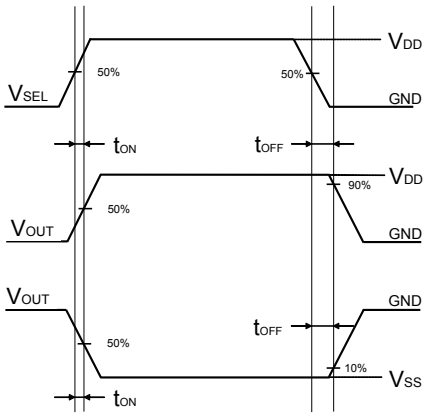



**Figure 36. Charge injection timing**

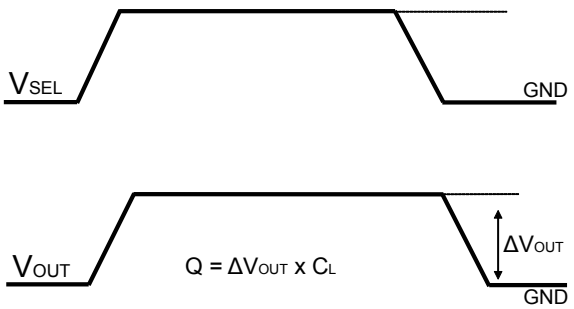



**Figure 37. Turn-on time, turn-off time on INH pin test circuit**

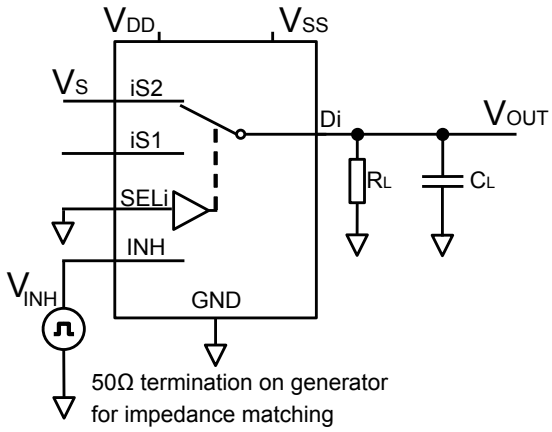


**Figure 38. Turn-on time, turn-off time on INH pin timing**

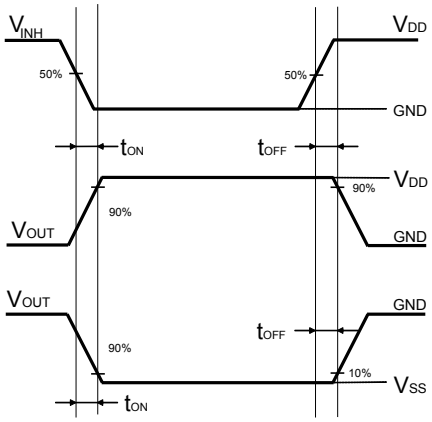
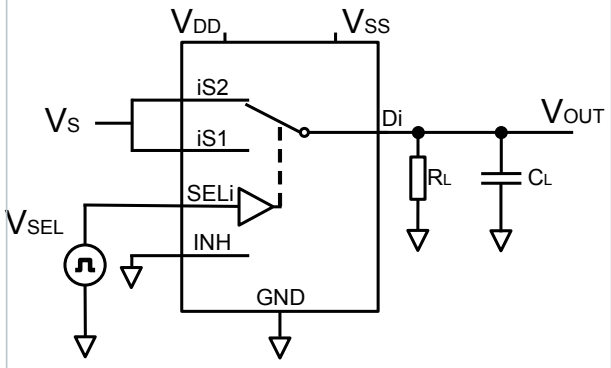



**Figure 39. Break before make test circuit**




50Ω termination on generator for impedance matching

**Figure 40. Break before make timing**

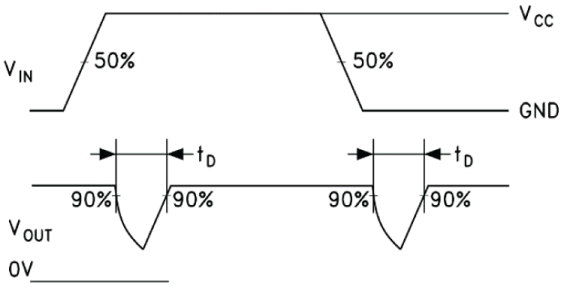
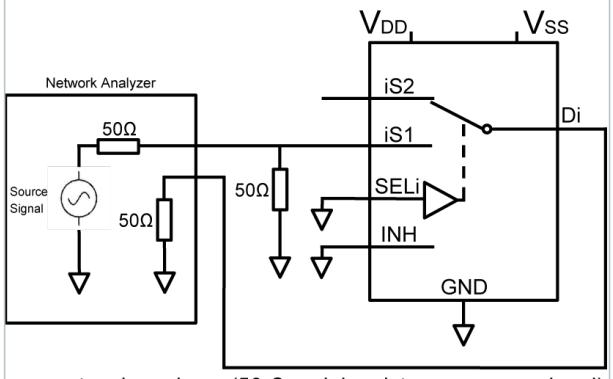
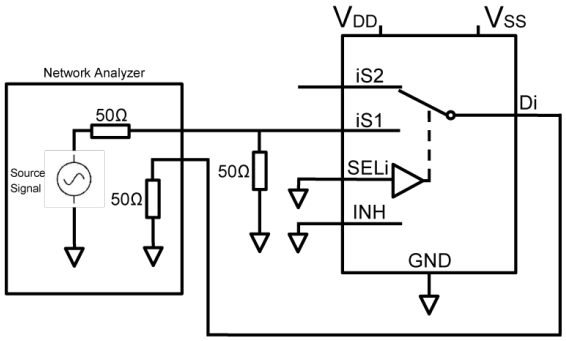



**Figure 41. OFF isolation test circuit**



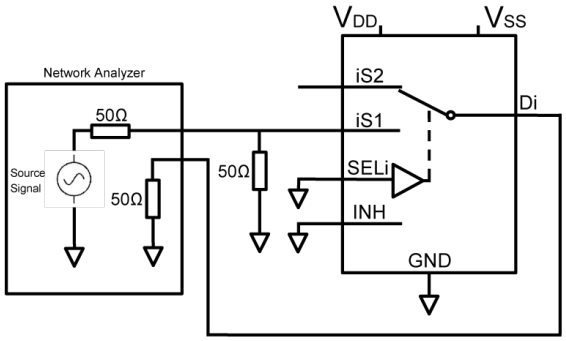

use network analyzer (50 Ω serial resistor on source signal)

**Figure 42. Crosstalk test circuit**




use network analyzer (50 Ω serial resistor on source signal )

**Figure 43. Bandwidth test circuit**




use network analyzer (50 Ω serial resistor on source signal )

Figure 44. $C_{SON}$ test circuit

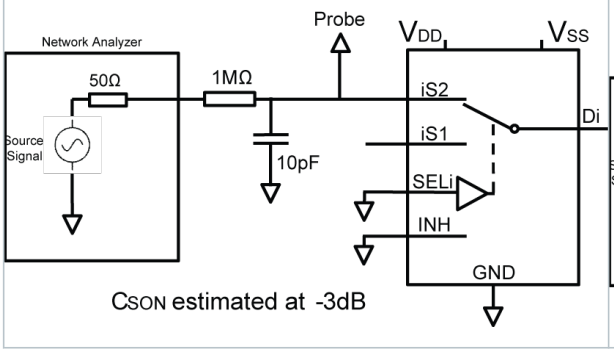



Figure 45. $C_{SOFF}$ test circuit

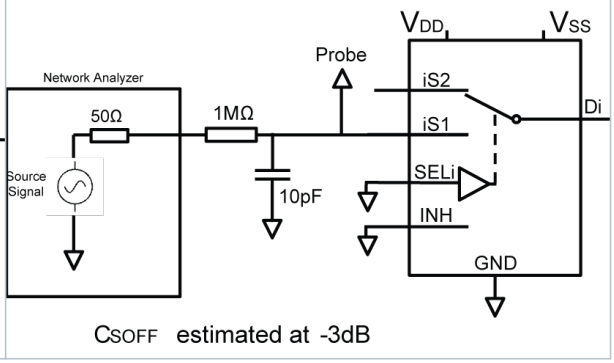
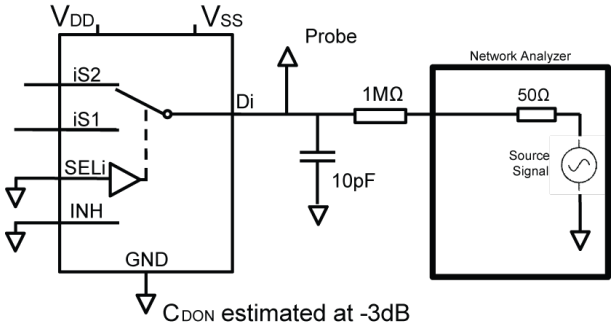



Figure 46. $C_{DON}$ test circuit



# 6 Application information

The device should be properly decoupled with 100 nF capacitors connected electrically and physically close to each power supply pin ($V_{DD}$ and $V_{SS}$); the other terminal of the capacitor being connected to the ground plane. In order to obtain the best performance of the device, a proper layout should be done in order to minimize the impact of parasitic inductance to avoid significant LdI/dt overshoot voltages. Trace length should be minimized. If the application is switching DC signals, adding decoupling capacitors on the S or D pins connected to these sources is also a good practice. Unused analog pins (Di, iS1, iS2) can either be left floating or connected to ground (or any other fixed voltage compatible with the operating table). Digital pins (SELi and INH) must be connected to either 0 V or $V_{DD}$. It is recommended to solder the exposed pad to a copper plane on PCB at $V_{SS}$ potential to obtain a better thermal impedance (but it can also be left open). When used for gain selection of an inverting gain amplification stage, it is recommended to place the switch directly on the inverting pin of the op amp (and not on the other side of Rg resistor). Indeed, as the input common mode voltage is fixed, the voltage on the analog switch is constant on all the channels, regardless of the analog signal being amplified. Therefore, even if the gain is reduced because of the Ron (-Rf/(Ron+Rg)), it is not modulated by its flatness which is not null.

# 7 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

## 7.1 QFN20 (4x4 mm) package information

**Figure 47. QFN20 (4x4 mm) package outline**

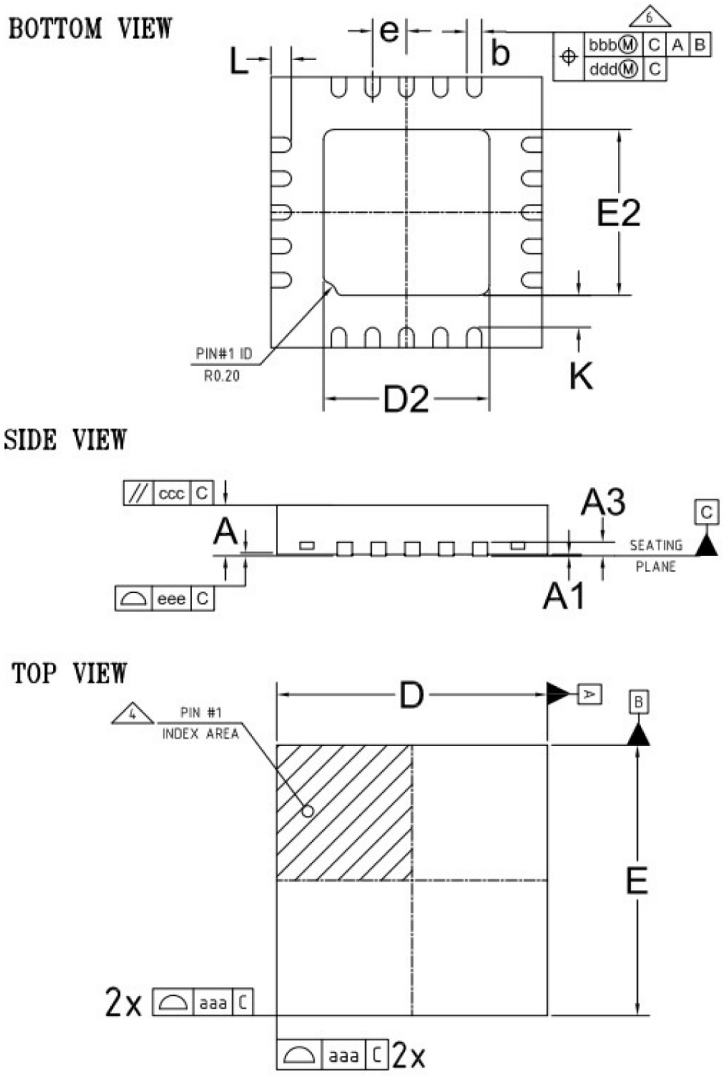
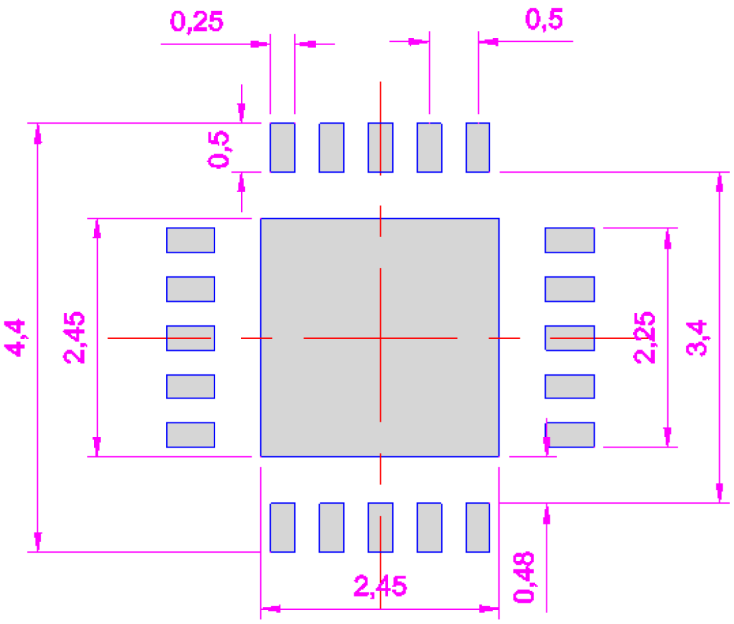


Table 7. **QFN20 (4x4 mm) mechanical data**

| Symbol | Milimeters | | |
|---|---|---|---|
| | Min. | Typ. | Max. |
| A | 0.70 | 0.75 | 0.80 |
| A1 | 0.00 | 0.02 | 0.05 |
| A3 | | 0.20 | |
| b | 0.18 | 0.25 | 0.30 |
| D | | 4.00 | |
| E | | 4.00 | |
| e | | 0.50 | |
| D2 | 2.30 | 2.45 | 2.55 |
| E2 | 2.30 | 2.45 | 2.55 |
| K | 0.20 | | |
| L | 0.20 | 0.30 | 0.40 |
| aaa | | 0.05 | |
| bbb | | 0.10 | |
| ccc | | 0.10 | |
| ddd | | 0.05 | |
| eee | | 0.08 | |

Figure 48. **QFN20 (4x4 mm) recommended footprint**



# 8 Ordering information

Table 8. **Order code**

| Order code | Temp. range | Package | Marking |
|---|---|---|---|
| STG1218IQT | -40 °C to 125 °C | QFN20 (4x4 mm) | W100 |

# Revision history

Table 9. **Document revision history**

| Date | Version | Changes |
|---|---|---|
| 29-Jun-2021 | 1 | Initial release. |
| 07-Jul-2021 | 2 | Updated Section 3 Electrical characteristics and Section 4 Electrical characteristics curves. |
| 02-Dec-2021 | 3 | Updated Section 4 Electrical characteristics curves. |

# Contents

# List of tables

# List of figures