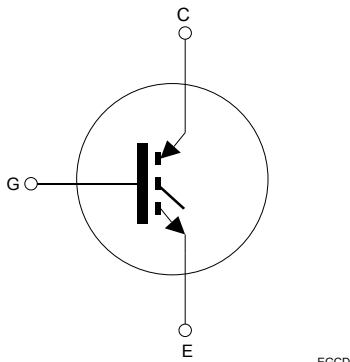


Trench gate field-stop 1200 V, 15 A low-loss M series IGBT die in D7 packing



Features

- 10 μ s of short-circuit withstanding time
- Low $V_{CE(sat)} = 1.85$ V (typ.) @ $I_C = 15$ A
- Positive $V_{CE(sat)}$ temperature coefficient
- Tight parameter distribution
- Maximum junction temperature: $T_J = 175$ °C

Applications

- Industrial motor control
- Industrial drives
- Solar inverters
- Uninterruptable power supplies (UPS)
- PFC converters

Description

This device is an IGBT developed using an advanced proprietary trench gate field-stop structure. The device is part of the M series IGBTs, which represent an optimal balance between inverter system performance and efficiency where the low-loss and the short-circuit functionality is essential. Furthermore, the positive $V_{CE(sat)}$ temperature coefficient and the tight parameter distribution result in safer paralleling operation.



Product status link

[STG15M120F3D7](#)

Product summary

Order code	STG15M120F3D7
V_{CE}	1200 V
I_{CN}	15 A
Die size	4.4 x 4.4 mm
Packing	D7

1 Mechanical parameters

Table 1. Mechanical parameters

Symbol	Value	Unit
Die size including scribe line	4.4 x 4.4	mm
Wafer size	200	mm
Maximum possible dice per wafer	1353	dice
Die thickness	110	µm
Front side passivation	Silicone nitride	
Emitter pad size including gate pad	2.57 x 3.37	mm
Gate pad size	0.82 x 1.20	mm
Front side metallization	composition	AlCu
	thickness	4.5 µm
Back side metallization	composition	Al/Ti/NiV/Ag
	thickness	0.65 µm
Die bond	Electrically conductive glue or soft solder	
Recommended wire bonding	≤500	µm

2 Electrical ratings

$T_J = 25\text{ °C}$ unless otherwise specified.

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{CES}	Collector-emitter voltage ($V_{GE} = 0\text{ V}$)	1200	V
V_{GE}	Gate-emitter voltage	± 20	V
$I_{CN}^{(1)}$	Continuous collector current at $T = 100\text{ °C}$	15	A
$I_{CP}^{(1)(2)}$	Pulsed collector current	45	A
$t_{SC}^{(3)}$	Short circuit withstand time ($V_{CC} = 600\text{ V}$, $V_{GE} = 15\text{ V}$, $V_{CE}(\text{peak}) \leq 1200\text{ V}$, $T_{J\text{start}} \leq 150\text{ °C}$)	10	μs
T_J	Operating junction temperature range	-55 to 175	$^{\circ}\text{C}$

1. Nominal collector current for die packaged in ST discrete solution. Current level depends on the assembly thermal properties and is limited by maximum junction temperature.
2. Pulse width is limited by maximum junction temperature.
3. Evaluated by design/characterization, not tested in production.

3 Electrical characteristics

$T_J = 25\text{ °C}$ unless otherwise specified.

Table 3. Static characteristics (tested on wafer unless otherwise specified)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)CES}$	Collector-emitter breakdown voltage	$I_C = 2\text{ mA}$, $V_{GE} = 0\text{ V}$	1200			V
$V_{CE(sat)}$	Collector-emitter saturation voltage	$V_{GE} = 15\text{ V}$, $I_C = 10\text{ A}$		1.5	2.0	V
		$V_{GE} = 15\text{ V}$, $I_C = 15\text{ A}$			2.4	
$V_{GE(th)}$	Gate threshold voltage	$V_{CE} = V_{GE}$, $I_C = 500\text{ }\mu\text{A}$	5	6	7	V
I_{CES}	Collector cut-off current	$V_{GE} = 0\text{ V}$, $V_{CE} = 1200\text{ V}$			25	μA
I_{GES}	Gate-emitter leakage current	$V_{CE} = 0\text{ V}$, $V_{GE} = \pm 20\text{ V}$			± 250	nA

Table 4. Electrical characteristics (evaluated by design/characterization, not tested in production)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{CE(sat)}$	Collector-emitter saturation voltage	$V_{GE} = 15\text{ V}$, $I_C = 15\text{ A}$	-	1.85	2.3	V
		$V_{GE} = 15\text{ V}$, $I_C = 15\text{ A}$, $T_J = 175\text{ °C}$	-	2.2		V
C_{ies}	Input capacitance		-	985		pF
C_{oes}	Output capacitance	$V_{CE} = 25\text{ V}$, $f = 1\text{ MHz}$, $V_{GE} = 0\text{ V}$	-	118		pF
C_{res}	Reverse transfer capacitance		-	38		pF
Q_g	Total gate charge	$V_{CC} = 960\text{ V}$, $I_C = 15\text{ A}$, $V_{GE} = 0\text{ to }15\text{ V}$	-	53		nC

Table 5. Switching characteristics on inductive load (evaluated by design/characterization, not tested in production)

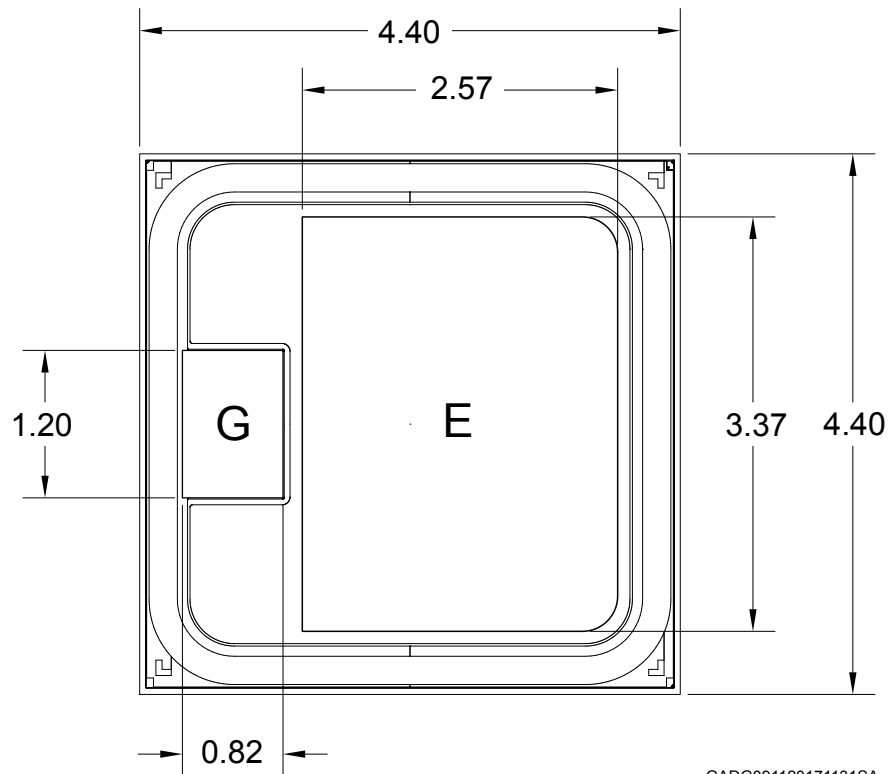
Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{CC} = 600\text{ V}$, $I_C = 15\text{ A}$, $V_{GE} = 15\text{ V}$, $R_G = 22\text{ }\Omega$	-	26	-	ns
t_r	Current rise time		-	12	-	ns
$t_{d(off)}$	Turn-off-delay time		-	122	-	ns
t_f	Current fall time		-	163	-	ns
$E_{off}^{(1)}$	Turn-off switching energy		-	850	-	μJ
$t_{d(on)}$	Turn-on delay time	$V_{CC} = 600\text{ V}$, $I_C = 15\text{ A}$, $V_{GE} = 15\text{ V}$, $R_G = 22\text{ }\Omega$, $T_J = 175\text{ °C}$	-	25	-	ns
t_r	Current rise time		-	14	-	ns
$t_{d(off)}$	Turn-off-delay time		-	136	-	ns
t_f	Current fall time		-	270	-	ns
$E_{off}^{(1)}$	Turn-off switching energy		-	1130	-	μJ

1. Including the tail of the collector current.

Note: The aforementioned values are not tested at chip level and are strongly dependent on the package/module design and the mounting technology. Refer to STGWA15M120DF3 datasheet for further information.

4 Die layout

Figure 1. Die drawing (dimensions are in mm)

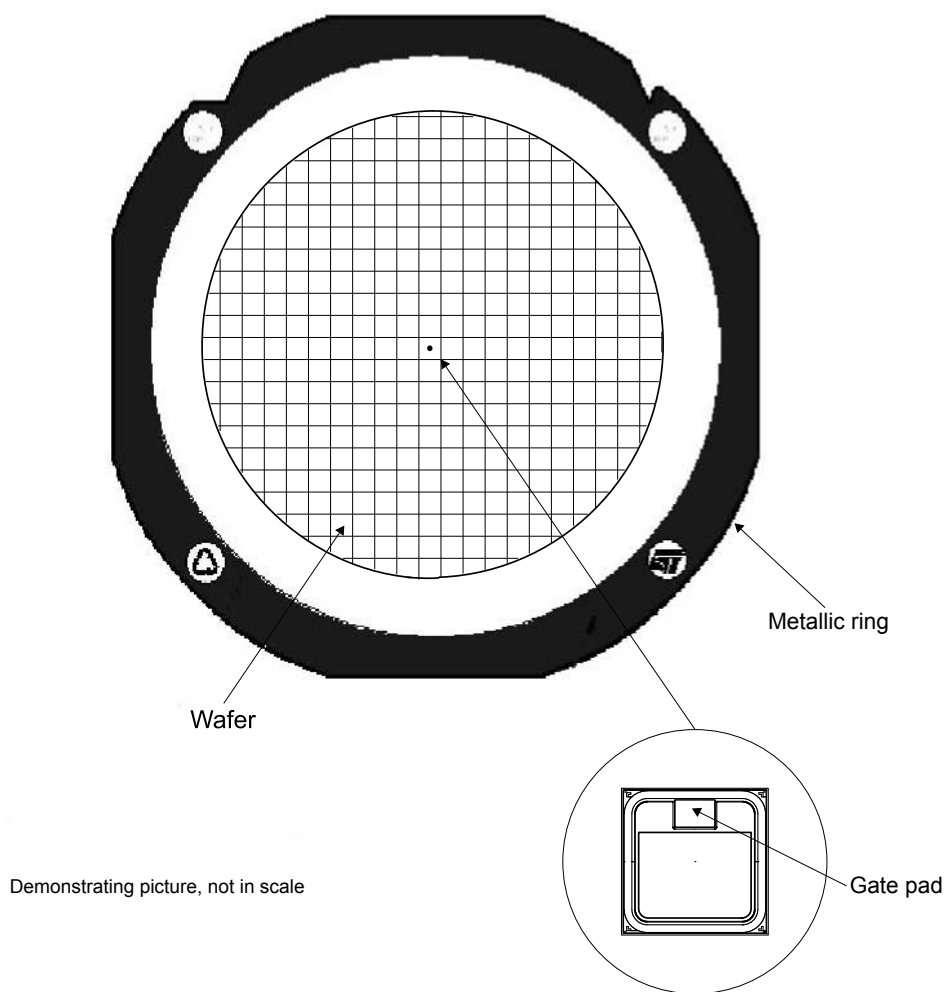


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Table 6. Die delivery

Packing	Description	Details
D7	Wafer tested, inked or inkless, cut on sticky foil on 10.8" (276 mm) ring (see Figure 2. D7 drawing and die orientation).	Wafer is held by ring and placed in a proper box, containing a maximum of 25 wafers, sealed under vacuum inside a plastic envelope. The latter is protected by two foam shells and then sealed in a carton box.

Figure 2. D7 drawing and die orientation



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5 Additional information

5.1 Additional testing and screening

For customers requiring product supplied as known good die (KGD) or requiring specific die level testing (that is for dynamic and switching characterization), please contact the local ST sales office.

If KGD is requested, the shipping delivery is D8.

5.2 Shipping

Several shipping options are offered. Consult the local ST sales office for availability:

- Die on film-sticky foil - suffix on sales type D7
- Carrier tape - suffix on sales type D8

5.3 Handling

- Products must be handled only at ESD safe workstations. Standard ESD precautions and safe work environments are as defined in MIL-HDBK-263.
- Products must be handled only in a class 1000 or better-designated clean room environment.
- Singular die is not to be handled with tweezers. A vacuum wand with a nonmetallic ESD protected tip should be used.

5.4 Wafer/die storage

Once the packaging is opened, the wafer must be stored in a dry, inert atmosphere, such as nitrogen.

Optimum temperature for storage is $18\text{ °C} \pm 2\text{ °C}$ with as few variations as possible to avoid parasitic polymerization of the adhesive. Sawn wafers must be processed within 12 weeks after receipt by the customer.

After the customer opens the package, the customer is responsible for the products.

Revision history

Table 7. Document revision history

Date	Revision	Changes
26-Jan-2015	1	Initial release
22-Nov-2017	2	<p>Modified title, internal schematic, features, applications and description.</p> <p>Modified <i>Table 2: "Mechanical parameters"</i>, <i>Table 3: "Absolute maximum ratings ($T_J = 25\text{ }^\circ\text{C}$ unless otherwise specified)"</i>, <i>Table 4: "Static characteristics (tested on wafer unless otherwise specified)"</i>, <i>Table 5: "Electrical characteristics (not tested at chip level, verified by design/characterization)"</i>, <i>Table 6: "Switching characteristics on inductive load (not tested at chip level, verified by design/characterization)"</i>.</p> <p>Modified <i>Figure 1: "Die drawing (dimensions are in mm)"</i> and <i>Figure 2: "D7 drawing and die orientation"</i>.</p> <p>Minor text changes.</p>
16-Aug-2022	3	<p>Updated title on cover page.</p> <p>Moved <i>2.1 Absolute maximum ratings</i> content as Section 2 Electrical ratings.</p> <p>Moved <i>2.2 Electrical characteristics</i> content as Section 3 Electrical characteristics.</p> <p>Updated <i>Table 3. Static characteristics (tested on wafer unless otherwise specified)</i>.</p> <p>Updated <i>Table 6. Die delivery</i>.</p> <p>Minor text changes.</p>

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