SamHop Microelectronics Corp.

# STG2454

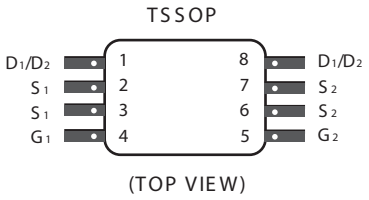
Ver 1.1

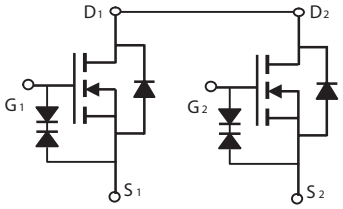
## Dual N-Channel Enhancement Mode Field Effect Transistor

| PRODUCT SUMMARY | | |
|---|---|---|
| $V_{DSS}$ | $I_D$ | $R_{DS(ON)}$ (mΩ) Max |
| 24V | 7A | 17 @ VGS=4.0V |
| | | 29 @ VGS=2.5V |

### FEATURES

- Super high dense cell design for low $R_{DS(ON)}$.
- Rugged and reliable.
- Suface Mount Package.
- ESD Protected.




### ABSOLUTE MAXIMUM RATINGS ($T_A$=25°C unless otherwise noted)

| Symbol | Parameter | | Limit | Units |
|---|---|---|---|---|
| $V_{DS}$ | Drain-Source Voltage | | 24 | V |
| $V_{GS}$ | Gate-Source Voltage | | ±12 | V |
| $I_D$ | Drain Current-Continuous [a] | $T_A$=25°C | 7 | A |
| | | $T_A$=70°C | 5.6 | A |
| $I_{DM}$ | -Pulsed [b] | | 28.5 | A |
| $P_D$ | Maximum Power Dissipation [a] | $T_A$=25°C | 1.5 | W |
| | | $T_A$=70°C | 1 | W |
| $T_J$, $T_{STG}$ | Operating Junction and Storage Temperature Range | | -55 to 150 | °C |

### THERMAL CHARACTERISTICS

| | | | |
|---|---|---|---|
| $R_{\theta JA}$ | Thermal Resistance, Junction-to-Ambient [a] | 85 | °C/W |

## ELECTRICAL CHARACTERISTICS ($T_A$=25°C unless otherwise noted)

| Symbol | Parameter | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| **OFF CHARACTERISTICS** | | | | | | |
| $BV_{DSS}$ | Drain-Source Breakdown Voltage | $V_{GS}$=0V , $I_D$=250uA | 24 | | | V |
| $I_{DSS}$ | Zero Gate Voltage Drain Current | $V_{DS}$=19V , $V_{GS}$=0V | | | 1 | uA |
| $I_{GSS}$ | Gate-Body Leakage Current | $V_{GS}$= ±12V , $V_{DS}$=0V | | | ±10 | uA |
| **ON CHARACTERISTICS** | | | | | | |
| $V_{GS(th)}$ | Gate Threshold Voltage | $V_{DS}$=$V_{GS}$ , $I_D$=250uA | 0.5 | 0.8 | 1.5 | V |
| $R_{DS(ON)}$ | Drain-Source On-State Resistance | $V_{GS}$=4.0V , $I_D$=7A | 10 | 14 | 17 | m ohm |
| | | $V_{GS}$=2.5V , $I_D$=6A | 13 | 20 | 29 | m ohm |
| $g_{FS}$ | Forward Transconductance | $V_{DS}$=5V , $I_D$=7A | | 35 | | S |
| **DYNAMIC CHARACTERISTICS** [c] | | | | | | |
| $C_{ISS}$ | Input Capacitance | $V_{DS}$=10V,$V_{GS}$=0V f=1.0MHz | | 730 | | pF |
| $C_{OSS}$ | Output Capacitance | | | 200 | | pF |
| $C_{RSS}$ | Reverse Transfer Capacitance | | | 180 | | pF |
| **SWITCHING CHARACTERISTICS** [c] | | | | | | |
| $t_{D(ON)}$ | Turn-On Delay Time | $V_{DD}$=10V $I_D$=1A $V_{GS}$=4.0V $R_{GEN}$=6 ohm | | 23 | | ns |
| $t_r$ | Rise Time | | | 83 | | ns |
| $t_{D(OFF)}$ | Turn-Off Delay Time | | | 108 | | ns |
| $t_f$ | Fall Time | | | 58 | | ns |
| $Q_g$ | Total Gate Charge | $V_{DS}$=10V,$I_D$=7A, $V_{GS}$=4.0V | | 12.5 | | nC |
| $Q_{gs}$ | Gate-Source Charge | | | 2 | | nC |
| $Q_{gd}$ | Gate-Drain Charge | | | 5 | | nC |
| **DRAIN-SOURCE DIODE CHARACTERISTICS AND MAXIMUM RATINGS** | | | | | | |
| $V_{SD}$ | Diode Forward Voltage [b] | $V_{GS}$=0V,$I_S$=1.5A | | 0.78 | 1.2 | V |

Notes

a.Surface Mounted on FR4 Board,t ≤ 10sec.
b.Pulse Test:Pulse Width ≤ 300us, Duty Cycle ≤ 2%.
c.Guaranteed by design, not subject to production testing.

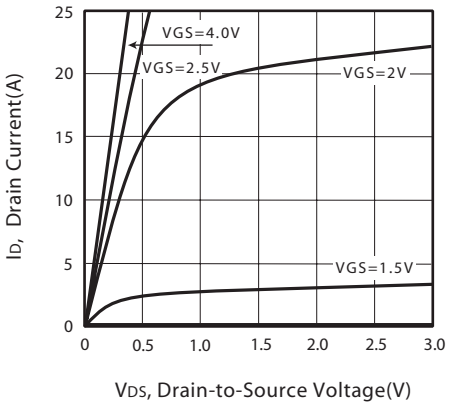



Figure 1. Output Characteristics

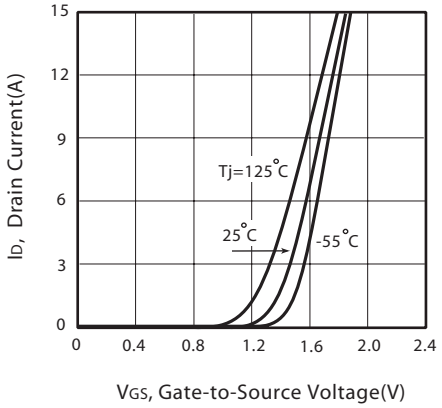



Figure 2. Transfer Characteristics

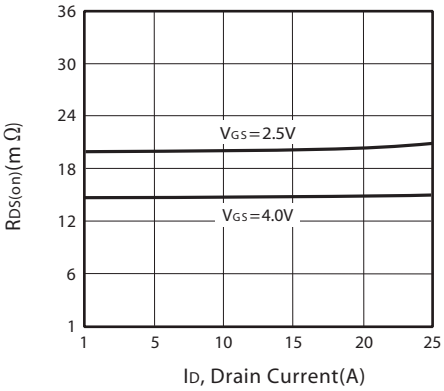



Figure 3. On-Resistance vs. Drain Current and Gate Voltage

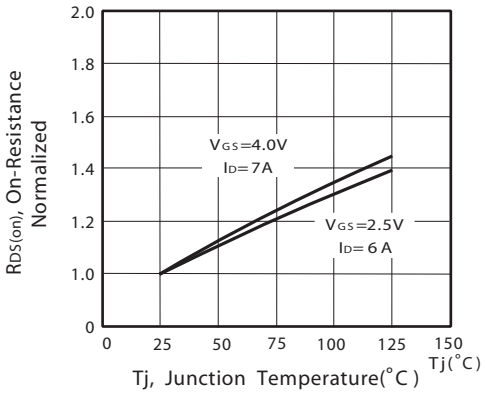



Figure 4. On-Resistance Variation with Drain Current and Temperature

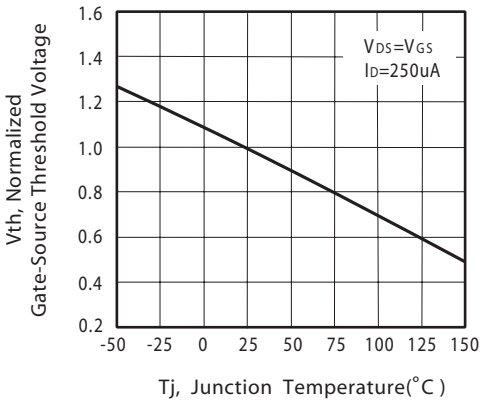



Figure 5. Gate Threshold Variation with Temperature

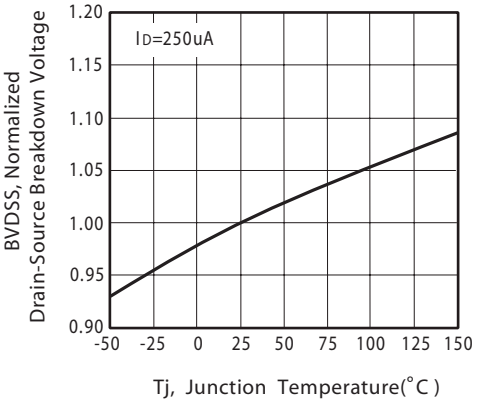



Figure 6. Breakdown Voltage Variation with Temperature

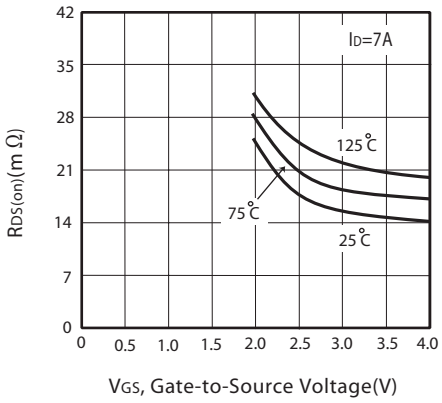



Figure 7. On-Resistance vs. Gate-Source Voltage

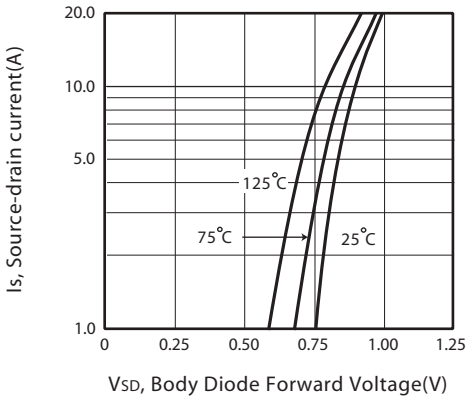



Figure 8. Body Diode Forward Voltage Variation with Source Current

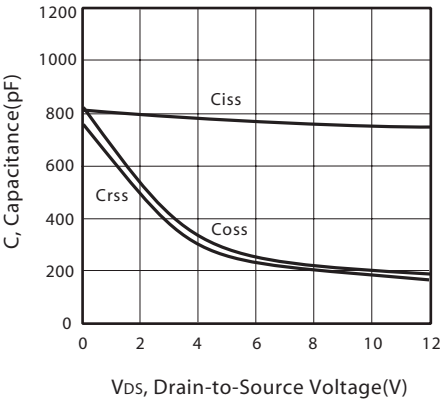



Figure 9. Capacitance

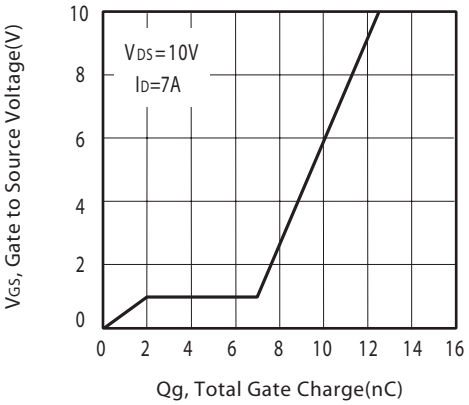



Figure 10. Gate Charge

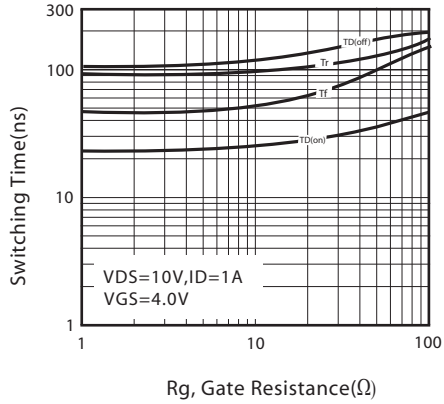



Figure 11. switching characteristics

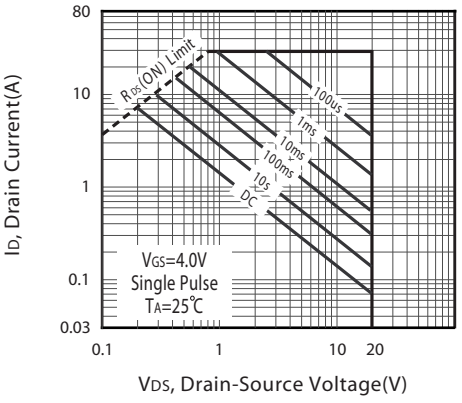
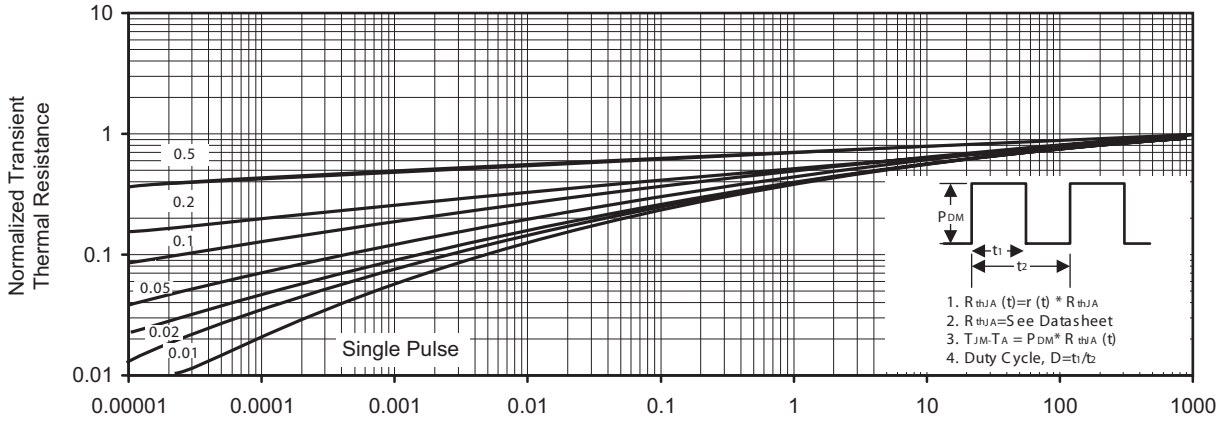


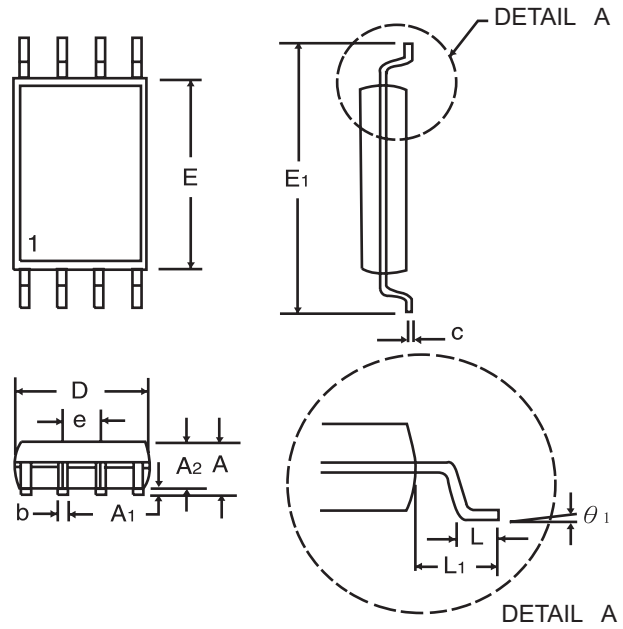

Figure 12. Maximum Safe Operating Area




Normalized Thermal Transient Impedance Curve

## PACKAGE OUTLINE DIMENSIONS

TSSOP-8

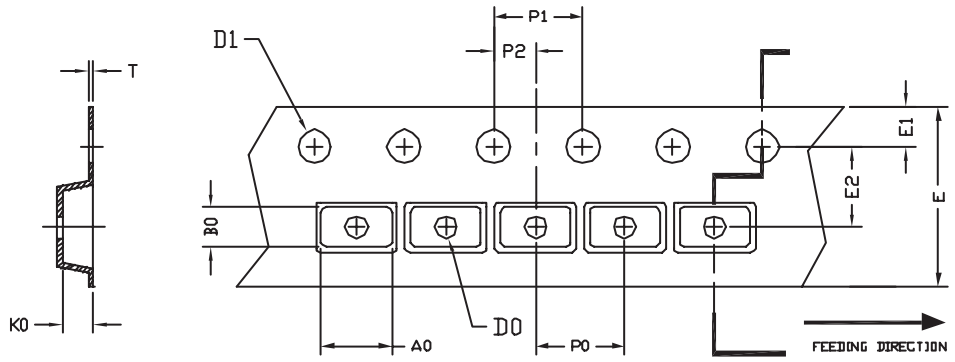



| SYMBOLS | MILLIMETERS | | INCHES | |
|---|---|---|---|---|
| | MIN | MAX | MIN | MAX |
| A | 0.85 | 1.20 | 0.033 | 0.047 |
| A1 | 0.05 | 0.15 | 0.002 | 0.006 |
| A2 | 0.80 | 1.05 | 0.031 | 0.041 |
| b | 0.19 | 0.30 | 0.007 | 0.012 |
| c | 0.127 | | 0.005 | |
| D | 2.90 | 3.10 ② | 0.114 | 0.122 ② |
| E | 4.30 | 4.50 ③ | 0.169 | 0.177 ③ |
| E1 | 6.20 | 6.60 | 0.244 | 0.260 |
| e | 0.65BSC | | 0.025BSC | |
| L | 0.50 | 0.70 | 0.020 | 0.028 |
| L1 | 1.00 | | 0.039 | |
| $\theta_1$ | 0° | 8° | 0° | 8° |

Notes:
1. This drawing is for general information only.Refer to JEDEC Drawing MO-153,Variation AA,for proper dimensions,tolerances,datums,etc.
2. Dimension D does not include mold Flash,protrusions or gate burrs.Mold Flash,protrusions and gate burrs shall not exceed 0.15 mm (0.006 in) per side.
3. Dimension E does not include inter-lead Flash or protrusions.Inter-lead Flash and protrusions shall not exceed 0.25mm (0.010 in) per side.
4. Dimension b does not include Dambar protrusion.Allowable Dambar protrusion shall be 0.08 mm total in excess of the b dimension at maximum material condition.Dambar cannot be located on the lower radius of the foot. Minimum space between protrusion and adjacent lead is 0.07 mm.
5. Dimension D and E to be determined at Datum Plane H.

# TSSOP-8 Tape and Reel Data

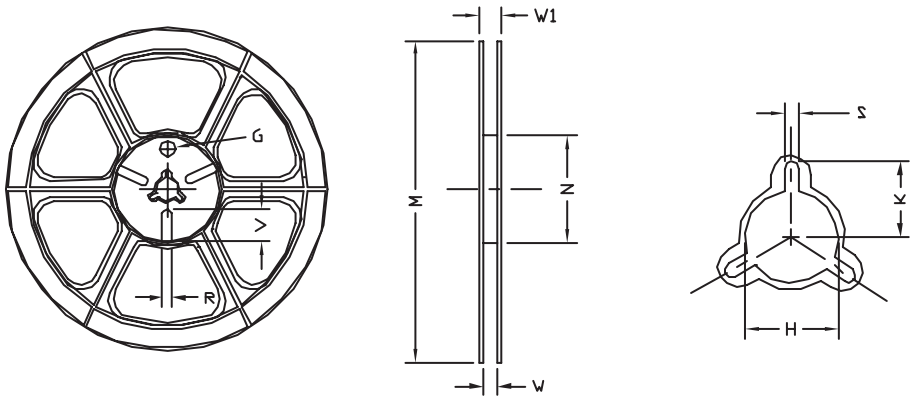
## TSSOP-8 Carrier Tape




UNIT : mm

| PACKAGE | A0 | B0 | K0 | D0 | D1 | E | E1 | E2 | P0 | P1 | P2 | T |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| TSSOP 8 | 6.08 | 4.40 | 1.60 | $\phi$ 1.50 + 0.1 - 0.0 | $\phi$ 1.50 + 0.1 - 0.0 | 12.00 ± 0.3 | 1.75 | 5.50 ± 0.05 | 8.00 | 4.00 | 2.00 ±0.05 | 0.30 ±0.05 |

## TSSOP-8 Reel




UNIT : mm

| TAPE SIZE | REEL SIZE | M | N | W | W1 | H | K | S | G | R | V |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 12 mm | $\phi$ 330 | 330 | 100 | 12.5 | 16.0 | $\phi$ 13.0 + 0.5 - 0.2 | 10.6 | 2.0 ±0.5 | --- | --- | --- |