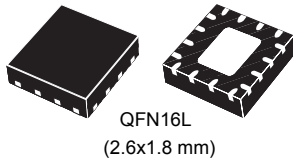


Low voltage high bandwidth quad SPDT switch



Maturity status link

[STG5592](#)

Device summary

Order code	STG5592QTR
Package	QFN16L (2.6 x 1.8 mm)
Packing	Tape and reel

Features

- Wide operating voltage range:
 - $V_{CC} \text{ (opr)} = 1.65 \text{ V to } 5.5 \text{ V}$ single supply
- Low on-resistance:
 - $R_{\text{on(peak)}} = 2.75 \Omega$ ($T_A = 25 \text{ }^\circ\text{C}$) at $V_{CC} = 5 \text{ V}$
- 1.8 V logic compatible
- Fail-safe logic
- Low power dissipation:
 - $I_{CC} = 0.1 \mu\text{A}$ at $T_A = 25 \text{ }^\circ\text{C}$
 - $I_{CC} = 25 \mu\text{A}$ at $T_A = 125 \text{ }^\circ\text{C}$
- Typical bandwidth (-3 dB) at 500 MHz on all channels
- -40 °C to +125 °C operating temperature
- USB (2.0) high speed (480 Mbps) signal switching compliant

Description

The circuit is a high-speed CMOS low voltage quad analog SPDT (single pole dual throw) switch or 2:1 multiplexer/demultiplexer switch developed with silicon gate CMOS technology. It is designed to operate from 1.65 V to 5.5 V, making this device ideal for portable applications.

The nSEL inputs are provided to control the switch. The switch S1 is ON (connected to common port Dn) when the nSEL input is held high, and OFF (a high impedance state exists between the two ports) when SEL is held low. The switch S2 is ON (connected to common port D) when the nSEL input is held low, and OFF (a high impedance state exists between the two ports) when nSEL is held high. Additional key features include: fast switching speed, break-before-make delay time, and ultra-low power consumption. All inputs and outputs are equipped with protection circuits against static discharge, giving them ESD immunity.

1 Pin configuration

Figure 1. Pin connection (top through view)

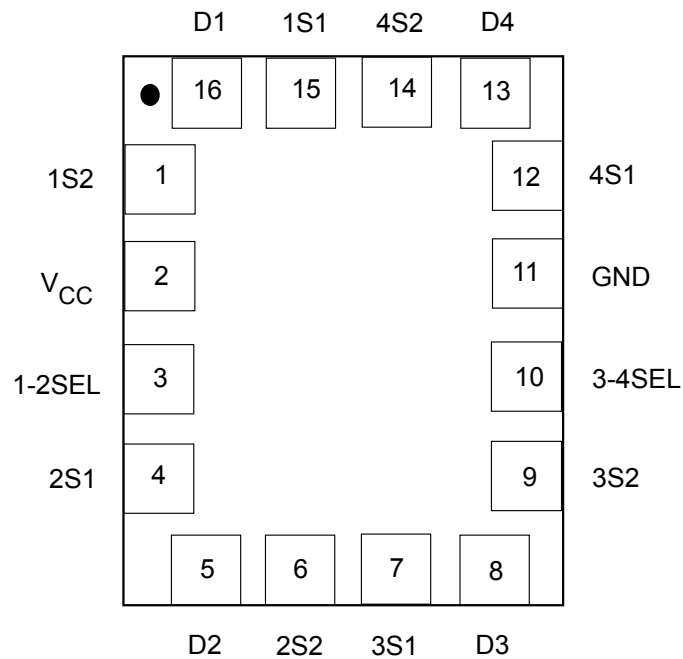


Table 1. Pin description

Pin	Symbol	Name and function
15, 1	1S1, 1S2	Independent channels
4, 6	2S1, 2S2	
7, 9	3S1, 3S2	
12, 14	4S1, 4S2	
16, 5, 8, 13	D1, D2, D3, D4	Common channels
3, 10	1-2SEL, 3-4SEL	Control
2	V _{CC}	Positive supply voltage
11	GND	Ground (0 V)

Note: The exposed pad must be soldered to a floating plane. Do not connect to power or ground.

2 Logic diagram

Figure 2. Input equivalent circuit

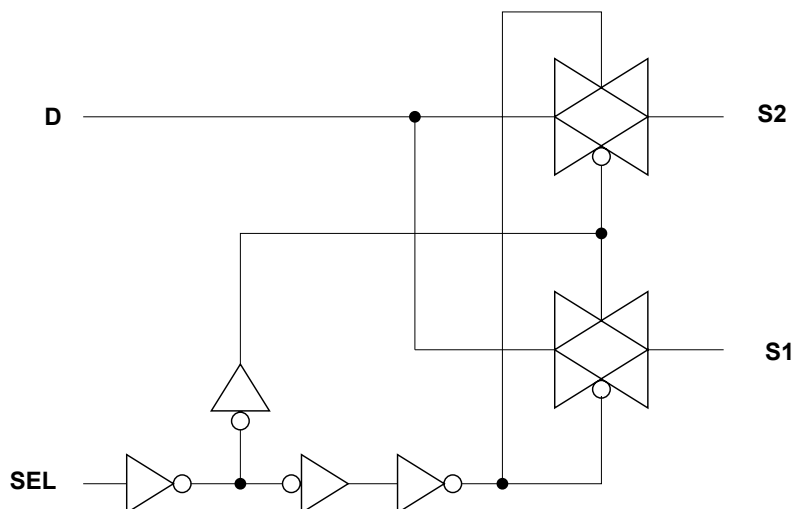


Table 2. Truth table

SEL	SWITCH S1	SWITCH S2
H	ON	OFF ⁽¹⁾
L	OFF ⁽¹⁾	ON

1. High impedance.

3 Maximum ratings

Stressing the device above the ratings listed in the absolute maximum ratings table may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 3. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{CC}	Supply voltage	-0.5 to +7	V
V_I	DC input voltage	-0.5 to $V_{CC} + 0.5$	V
V_{IC}	DC control input voltage	-0.5 to +7	V
V_O	DC output voltage	-0.5 to $V_{CC} + 0.5$	V
I_{IKC}	DC input diode current on control pin ($V_{SEL} < 0$ V)	-50	mA
I_{IK}	DC input diode current (S pins)	±50	mA
I_{OK}	DC output diode current (D pins)	±20	mA
I_O	DC output current	±128	mA
I_{OP}	DC output current peak (pulse at 1 ms, 10% duty cycle)	±300	mA
I_{CC} or I_{GND}	DC V_{CC} or ground current	±100	mA
P_D	Power dissipation at $T_A = 70$ °C ⁽¹⁾	1120	mW
T_{stg}	Storage temperature	-65 to +150	°C
T_L	Lead temperature (10 s)	300	°C
ESD	HBM: human body model ⁽²⁾	2000	V
	CDM: charged device model ⁽³⁾	1000	

1. Derate above 70 °C by 18.5 mW/C.
2. HBM test according to the standard ESDA/JEDEC JS-001-2017.
3. CDM test according to the standard ESDA/JEDEC JS-002-2022.

Table 4. Recommended operating conditions

Symbol	Parameter	Value	Unit
V_{CC}	Supply voltage	1.65 to 5.5	V
V_I	Input voltage	0 to V_{CC}	V
V_{IC}	Control input voltage	0 to 5.5	V
V_O	Output voltage	0 to V_{CC}	V
T_{op}	Operating temperature	-40 to +125	°C
dt/dv	Input rise and fall time control input	$V_{CC} = 1.65$ V to 2.7 V	0 to 20
		$V_{CC} = 3.0$ V to 5.5 V	0 to 10

4 Electrical characteristics

Table 5. DC electrical characteristics for STG5592

Symbol	Parameter	Test conditions		Value					Unit
		V _{CC} (V)		T _A = 25 °C			-40 to +125 °C ⁽¹⁾		
				Min.	Typ.	Max.	Min.	Max.	
V _{IH}	High level input voltage	1.65 to 1.95		0.8	0.73		0.9		V
		2.3 to 2.5		0.9	0.79		1		
		2.7 to 3.0		1	0.87		1.05		
		3.3 to 3.6		1.05	0.95		1.1		
		4.3		1.15	1.02		1.2		
		5		1.25	1.07		1.3		
		5.5		1.3	1.11		1.35		
V _{IL}	Low level input voltage	1.65 to 1.95			0.55	0.5		0.4	V
		2.3 to 2.5			0.67	0.6		0.5	
		2.7 to 3.0			0.71	0.65		0.55	
		3.3 to 3.6			0.76	0.7		0.6	
		4.3			0.87	0.8		0.75	
		5			0.93	0.9		0.8	
		5.5			0.98	0.95		0.85	
R _{PEAK}	Switch-on peak resistance	1.8	V _S = 0 V to V _{CC} , I _S = 8 mA		9	13		16	Ω
		2.7			4.5	6		8	
		3			4	5		7.5	
		3.7			3.5	4.5		6.5	
		4.3			3	4		6.0	
		5			2.75	3.5		5.5	
		5.5			2.5	3.5		5	
R _{ON}	Switch-on resistance	3	V _S = 3 V, I _S = 8 mA		3.2	4			Ω
		3	V _S = 0.8 V, I _S = 8 mA		3.6	4.5			
ΔR _{ON} (per channel)	ON-resistance match ⁽²⁾	1.8 V to 5.5 V	V _S @ R _{ON} max., I _S = 8 mA		0.13			0.2	Ω
ΔR _{ON} (per switch)	ON-resistance match ⁽³⁾	1.8 V to 5.5 V	V _S @ R _{ON} max., I _S = 8 mA		0.21			0.3	Ω
R _{FLAT}	ON-resistance flatness ⁽⁴⁾	1.8	V _S = 0 V to V _{CC} , I _S = 8 mA		4	7		10	Ω
		2.7			1	2		3	
		3			0.5	2		2.5	
		3.7			0.5	1.5		2	
		4.3			0.5	1.5		2	
		5			0.5	1.5		2	
		5.5			0.5	1.5		2	

Symbol	Parameter	Test conditions		Value					Unit
		V _{CC} (V)		T _A = 25 °C			-40 to +125 °C ⁽¹⁾		
				Min.	Typ.	Max.	Min.	Max.	
I _{OFF}	OFF-state leakage current (SN)	5.5	V _S = 0.3 V and V _D = 5.2 V or V _S = 5.2 V and V = 0.3 V			±20		±50	nA
I _{ON}	ON-state leakage current (D)	5.5	V _S = 0.3 V and V _D = 5.2 V or V _S = 5.2 V and V _D = 0.3 V			±20		±50	nA
I _{SEL}	SEL input leakage current	0 to 5.5	V _{SEL} = 0 V to 5.5 V T _{max} = 125 °C			±0.1		±15	μA
			V _{SEL} = 0 V to 5.5 V T _{max} = 85 °C					±2	μA
I _{CC}	Quiescent supply current	1.65 to 5.5	V _{SEL} = V _{CC} or GND T _{max} = 125 °C			±0.1		±25	μA
			V _{SEL} = V _{CC} or GND T _{max} = 85 °C			±0.1		±3	μA
I _{CCLV} ⁽⁵⁾	Quiescent supply current low voltage driving	4.3	V _{1-2SEL} or V _{3-4SEL} = 1.65 V		±20	±25		±50	μA
			V _{1-2SEL} or V _{3-4SEL} = 1.80 V		±17	±22		±45	
			V _{1-2SEL} or V _{3-4SEL} = 2.60 V		±6	±11		±40	
I _{CCLV} ⁽⁵⁾	Quiescent supply current low voltage driving	5.5	V _{1-2SEL} or V _{3-4SEL} = 1.65 V		±46	±55		±70	μA
			V _{1-2SEL} or V _{3-4SEL} = 1.80 V		±42	±50		±65	
			V _{1-2SEL} or V _{3-4SEL} = 2.60 V		±25	±30		±50	

1. Unless otherwise specified.

2. ΔR_{ON} (per channel) = max. |mS1-mS2|, where m = 1..4.

3. ΔR_{ON} (per switch) = max. |mSN-nSN|, where m = 1..4 and n = 1..4, N = 1..2.

4. Flatness is defined as the difference between the maximum and minimum value of on-resistance as measured over the specified analog signal ranges.

5. One of the two selection pins is connected to GND.

Table 6. Analog switch characteristics for STG5592 ($C_L = 5 \text{ pF}$, $R_L = 50 \text{ }\Omega$)

Symbol	Parameter	Test conditions		Value					Unit
		V_{CC} (V)		$T_A = 25 \text{ }^\circ\text{C}$			$-40 \text{ to } +125 \text{ }^\circ\text{C}$		
				Min.	Typ.	Max.	Min.	Max.	
t_{PLH} , t_{PHL}	Propagation delay	1.65 to 1.95			0.3				ns
		2.3 to 2.7			0.3				
		3.0 to 3.3			0.25				
		3.6 to 4.3			0.25				
		5 to 5.5			0.25				
t_{ON}	Turn-on time	1.65 to 1.95	$V_S = 0.8 \text{ V}$		20	35		40	ns
		2.3 to 2.7	$V_S = 1.5 \text{ V}$		11	20		25	
		3.0 to 3.3			8	15		20	
		3.6 to 4.3			7	11		15	
		5 to 5.5			5	10		13	
t_{OFF}	Turn-off time	1.65 to 1.95	$V_S = 0.8 \text{ V}$		8	20		22	ns
		2.3 to 2.7	$V_S = 1.5 \text{ V}$		6	15		17	
		3.0 to 3.3			6	10		12	
		3.6 to 4.3			6	10		12	
		5 to 5.5			6	10		12	
t_D	Break-before-make time delay	1.65 to 1.95	$C_L = 35 \text{ pF}$, $R_L = 50 \text{ }\Omega$, $V_S = 1.5 \text{ V}$		5	11		2	ns
		2.3 to 2.7			3	6		1	
		3.0 to 3.3			2	4		1	
		3.6 to 4.3			1	2		0.5	
		5 to 5.5			1	1.5		0.5	
Q	Charge injection	1.65	$C_L = 100 \text{ pF}$		2.7				pC
		2.3			4.3				
		3			5.6				
		4.3			7.7				
		5.5			9.7				
OIRR	Off isolation ⁽¹⁾	1.65 to 5.5	$V_S = 1 \text{ V}_{DC}$, $f = 1 \text{ MHz}$, signal = 0 dBm		-74			dB	
			$V_S = 1 \text{ V}_{DC}$, $f = 10 \text{ MHz}$, signal = 0 dBm		-54				
X_{talk}	Crosstalk	1.65 to 5.5	$V_S = 1 \text{ V}_{DC}$, $f = 1 \text{ MHz}$, signal = 0 dBm		-75			dB	
			$V_S = 1 \text{ V}_{DC}$, $f = 10 \text{ MHz}$, signal = 0 dBm		-55				
B_W	-3 dB bandwidth	1.65 to 5.5 Typ 4.3 V	$R_L = 50 \text{ }\Omega$, signal = 0 dBm	350	450	600	335	MHz	
D_G	Differential gain	3.0 to 5.5	$R_L = 150 \text{ }\Omega$		0.64			%	
D_P	Differential phase	3.0 to 5.5	$R_L = 150 \text{ }\Omega$		0.1			deg	

Symbol	Parameter	Test conditions		Value					Unit
		V _{CC} (V)		T _A = 25 °C			-40 to +125 °C		
				Min.	Typ.	Max.	Min.	Max.	
C _{IN}	Control pin input capacitance	3.3	V _S = 40 mV _{PP}		3				pF
C _{ON}	Sn port capacitance when the switch is enabled	3.3			12				pF
C _{OFF}	Sn port capacitance when the switch is disabled	3.3			5				pF

1. Off isolation = 20 Log₁₀ (V_D/V_S), V_D = output. V_S = input to off switch.

Table 7. USB related AC electrical characteristics for STG5592

Symbol	Parameter	Test conditions		Value					Unit
		V _{CC} (V)		T _A = +25 °C			-40 to +125 °C		
				Min.	Typ.	Max.	Min.	Max.	
t _{SK(0)}	Channel-to-channel skew	3.0 to 3.6	C _L = 10 pF		26				ps
t _{SK(P)}	Skew of opposite transition of the same output	3.0 to 3.6	C _L = 10 pF		60				ps
T _J	Total jitter	3.0 to 3.6	R _L = 50 Ω, C _L = 10 pF, t _R = t _F = 750 ps at 480 Mbps		130				ps

5 Electrical characteristics curves of STG5592

Figure 3. ON resistance vs. S or D voltage for various power supply voltages

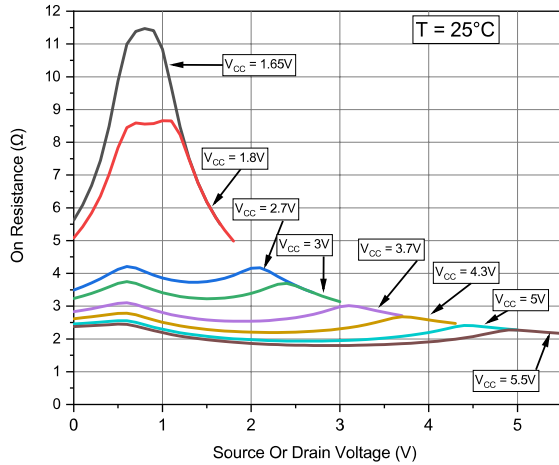


Figure 4. ON resistance peak vs. power supply voltage

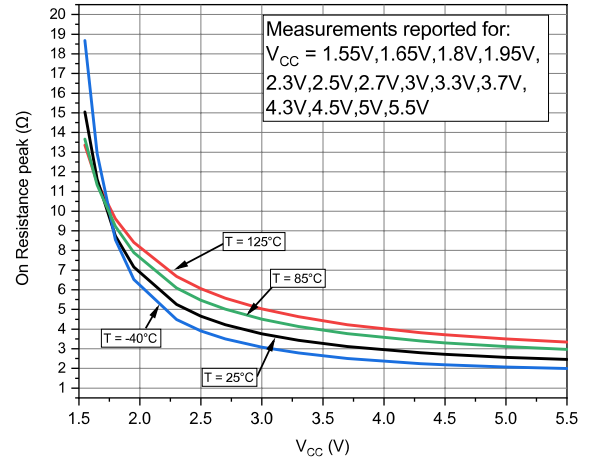


Figure 5. ON resistance vs. S or D for $V_{CC} = 1.8\text{V}$

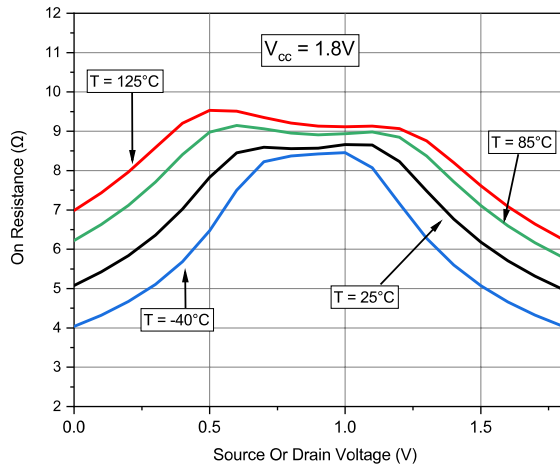


Figure 6. ON resistance vs. S or D for $V_{CC} = 2.7\text{V}$

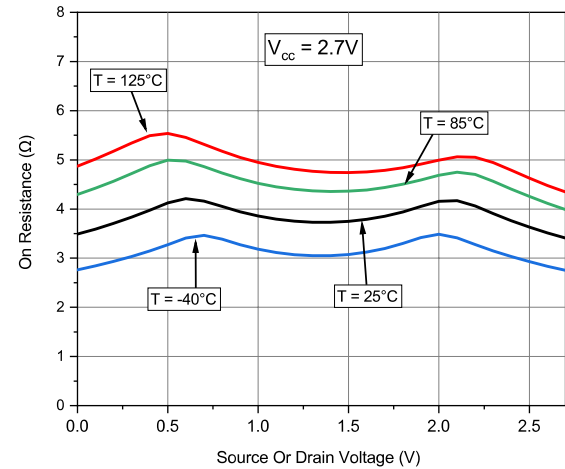


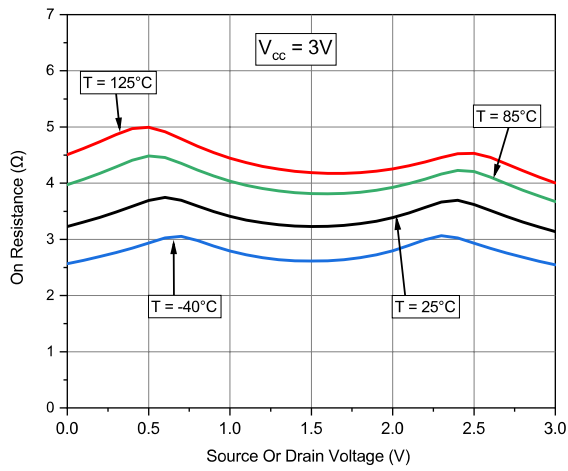
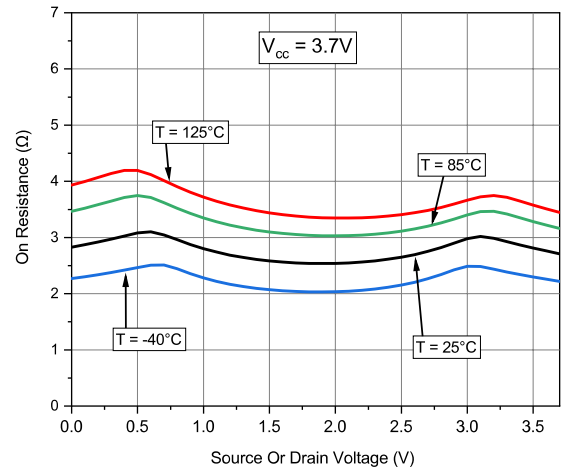
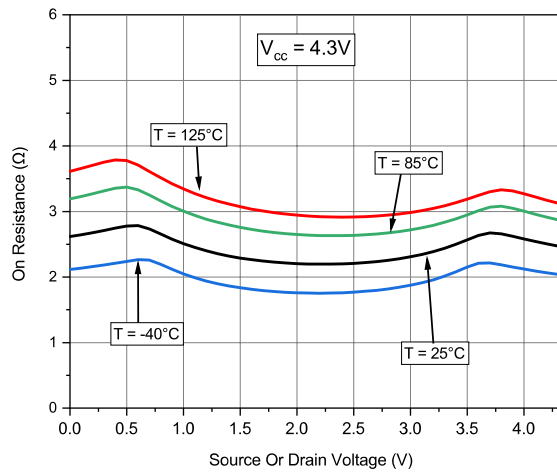
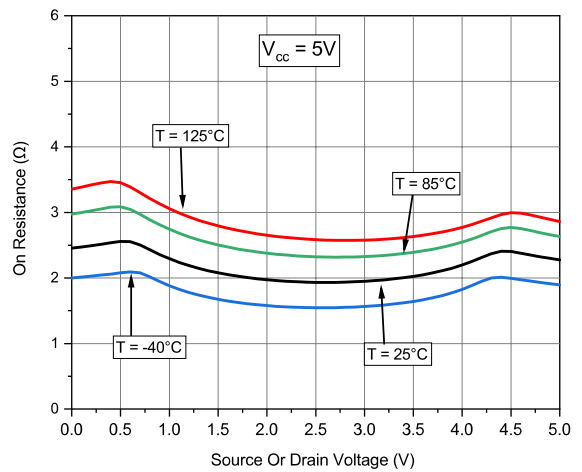
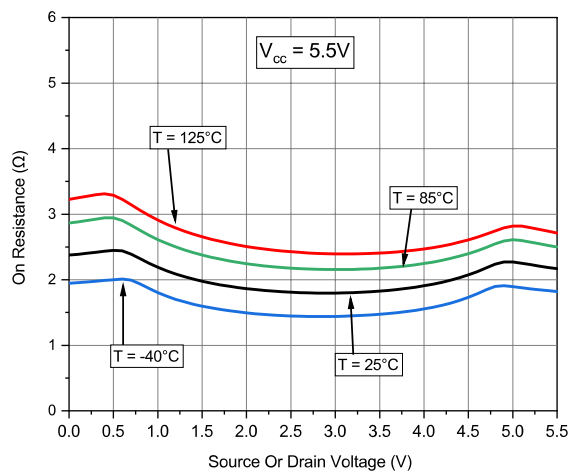
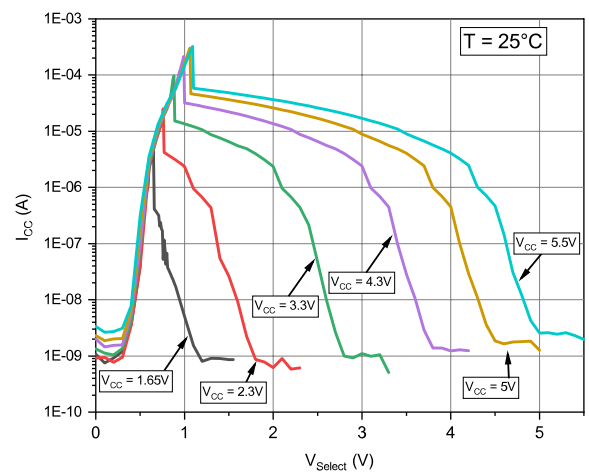
Figure 7. ON resistance vs. S or D for $V_{CC} = 3V$

Figure 8. ON resistance vs. S or D for $V_{CC} = 3.7V$

Figure 9. ON resistance vs. S or D for $V_{CC} = 4.3V$

Figure 10. ON resistance vs. S or D for $V_{CC} = 5V$

Figure 11. ON resistance vs. S or D for $V_{CC} = 5.5V$

Figure 12. I_{CC} vs. logic voltage at 25°C


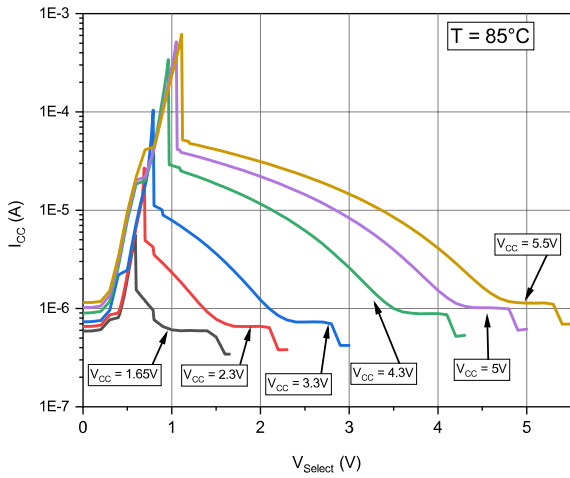
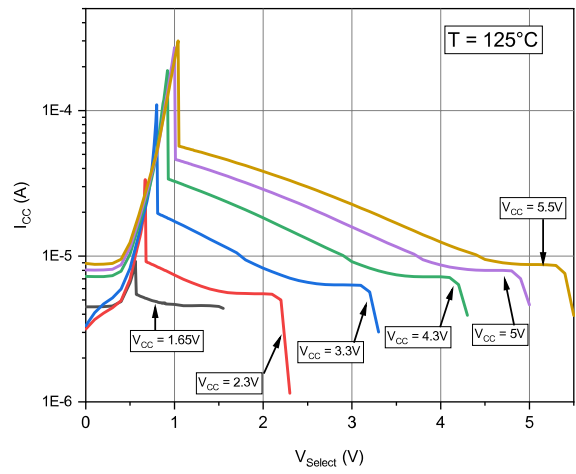
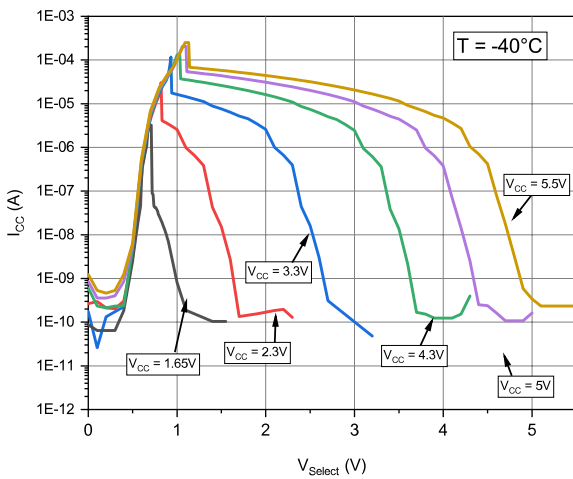
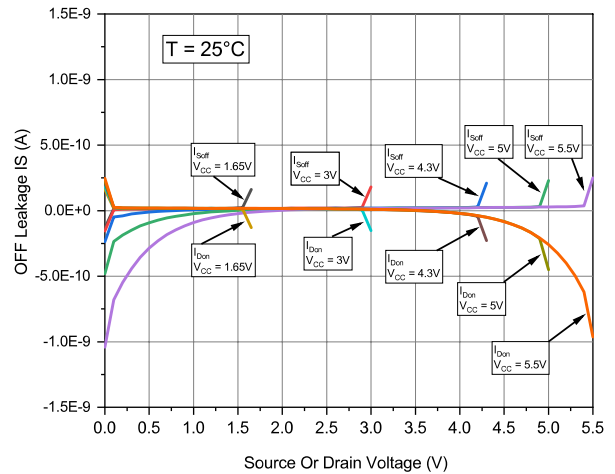
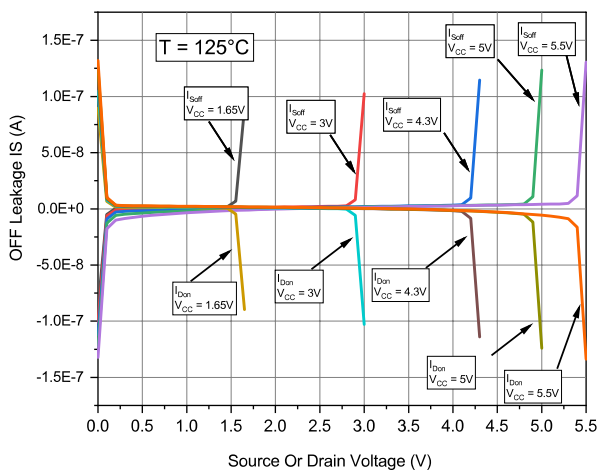
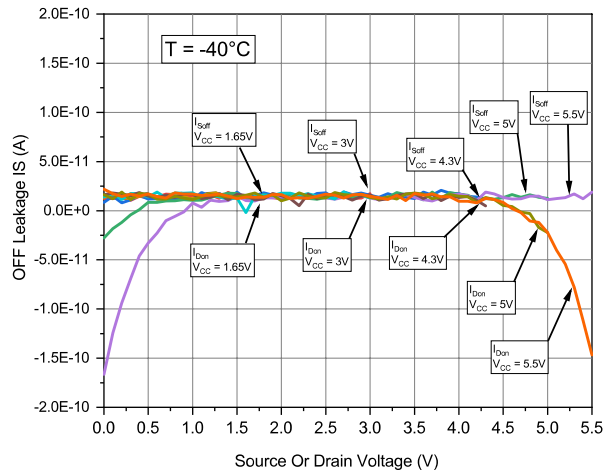
Figure 13. I_{CC} vs. logic voltage at 85 °C

Figure 14. I_{CC} vs. logic voltage at 125 °C

Figure 15. I_{CC} vs. logic voltage at -40 °C

Figure 16. Leakage current at 25 °C

Figure 17. Leakage current at 125 °C

Figure 18. Leakage current at -40 °C


Figure 19. $t_{ONS1}(SEL)$ vs. temperature

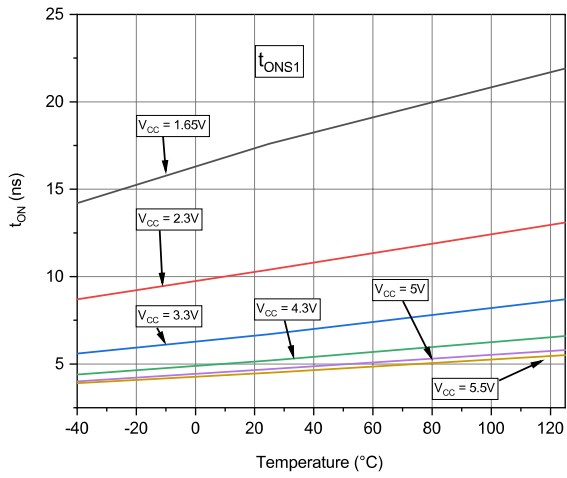


Figure 20. $t_{ONS2}(SEL)$ vs. temperature

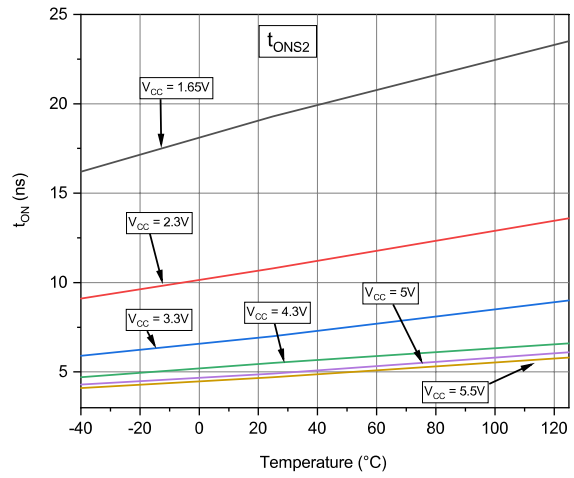


Figure 21. $t_{OFFS1}(SEL)$ vs. temperature

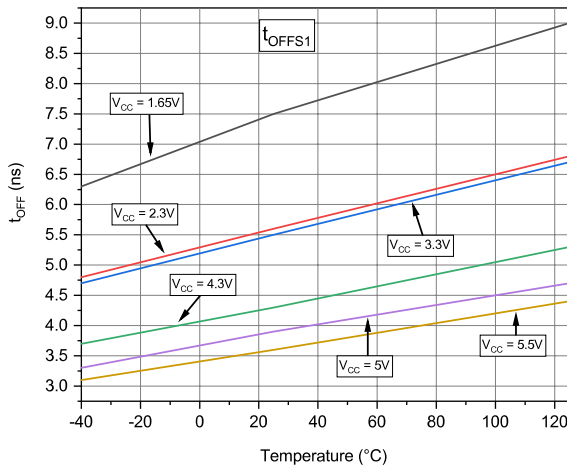


Figure 22. $t_{OFFS2}(SEL)$ vs. temperature

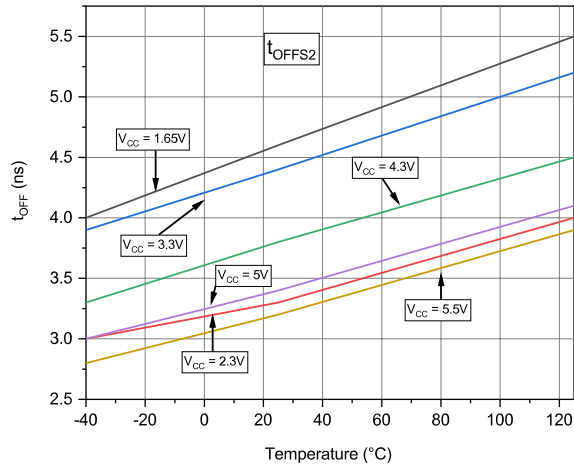


Figure 23. Bandwidth

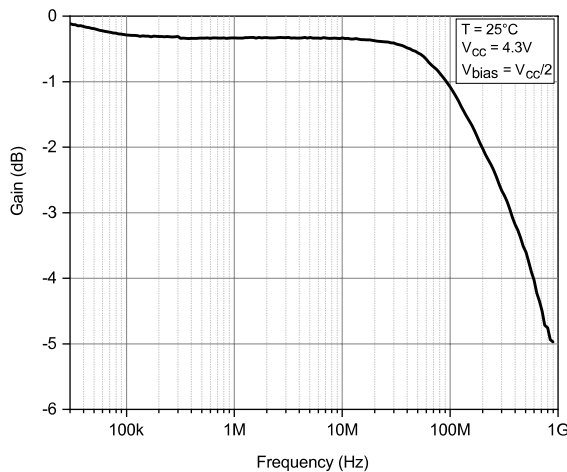


Figure 24. Off isolation

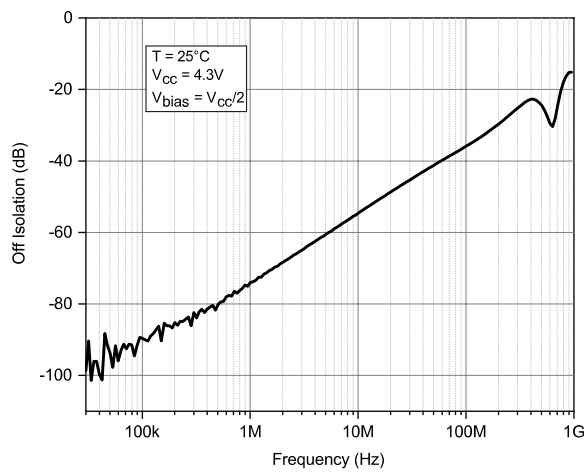
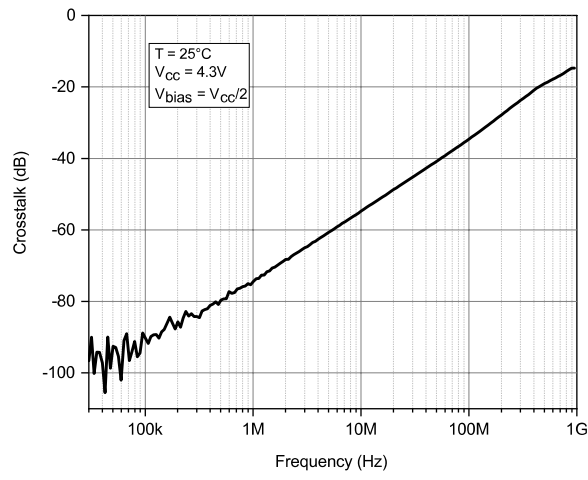


Figure 25. Crosstalk



6 Test circuits

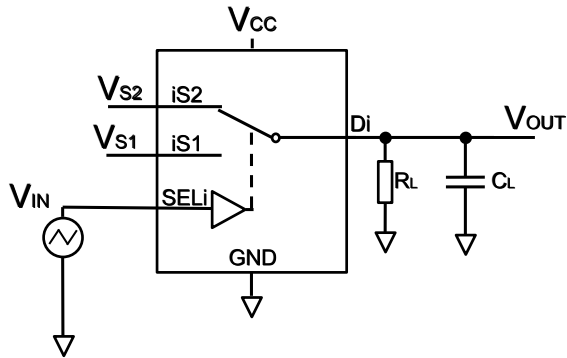
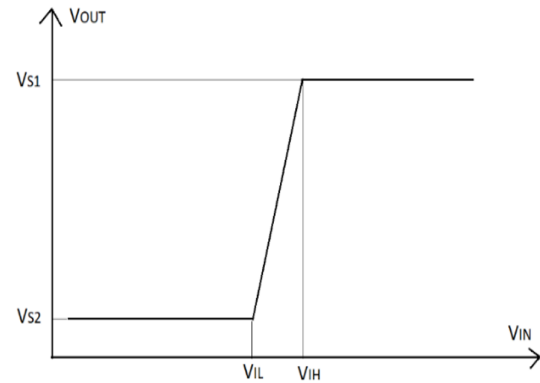
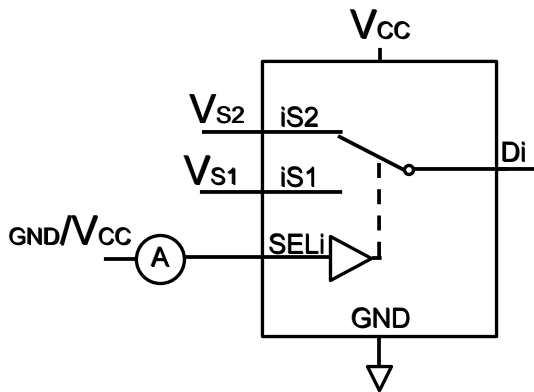
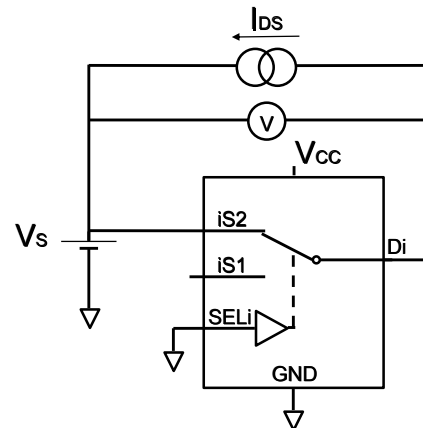
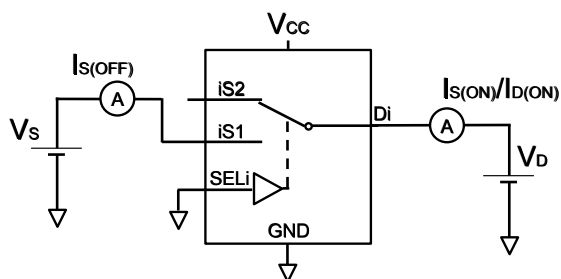
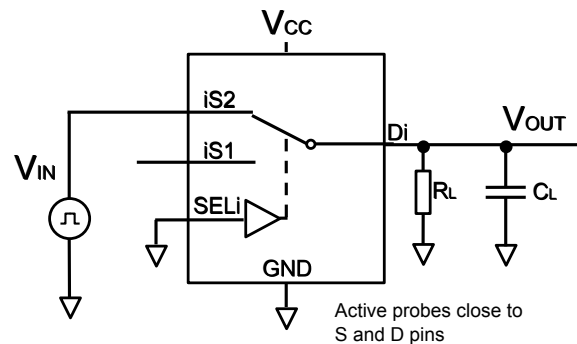
Figure 26. SEL input threshold voltage test circuit

Figure 27. SEL input threshold

Figure 28. SEL input leakage current test circuit

Figure 29. ON resistance, flatness, and mismatch test circuit

Figure 30. OFF & ON leakage current test circuit

Figure 31. Propagation delay test circuit


Figure 32. Propagation delay timing

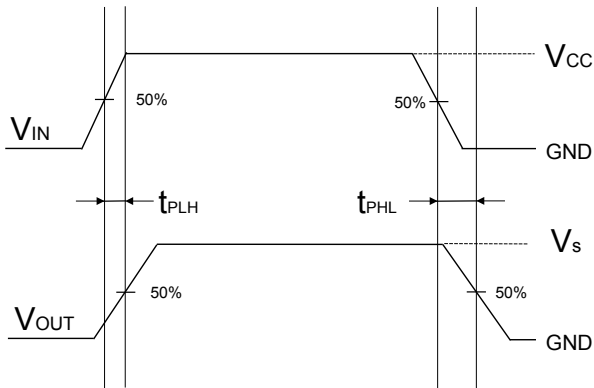


Figure 33. Turn ON time, turn OFF time, and skew on SEL pin

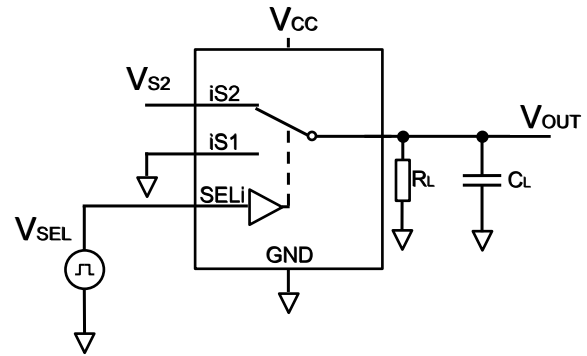


Figure 34. Turn ON time and turn OFF time on SEL pin timing

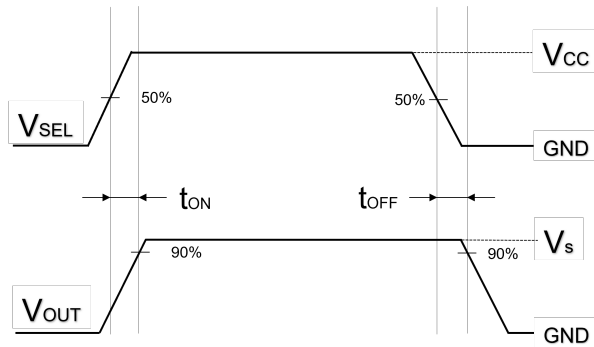


Figure 35. Charge injection test circuit

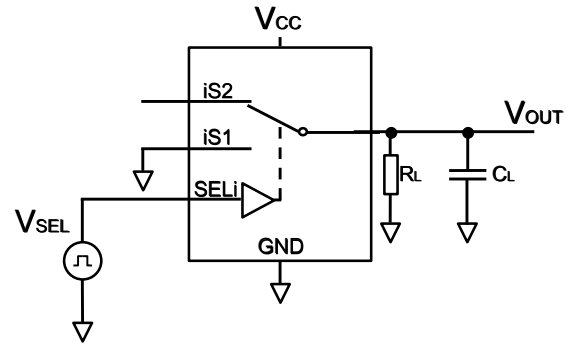


Figure 36. Charge injection timing

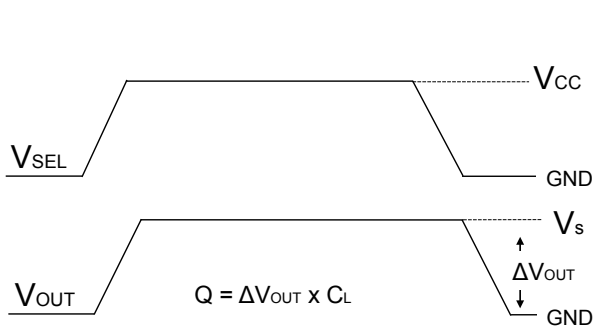
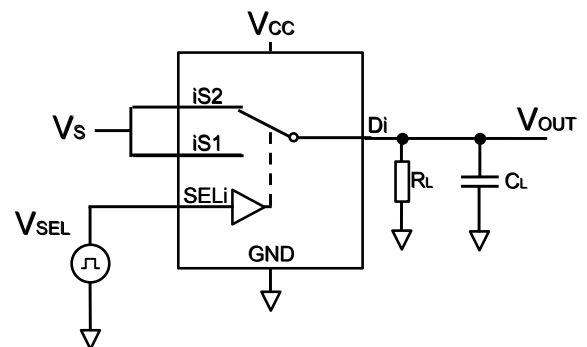


Figure 37. Break-before-make test circuit



50 Ω termination on generator for impedance matching

Figure 38. Break-before-make timing

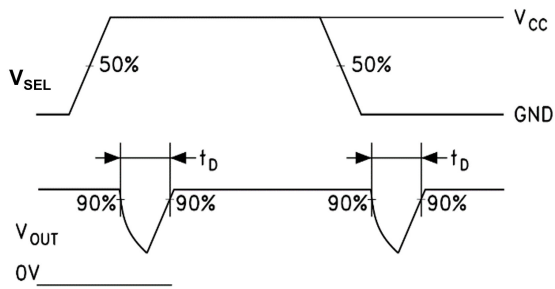


Figure 39. Off isolation test circuit

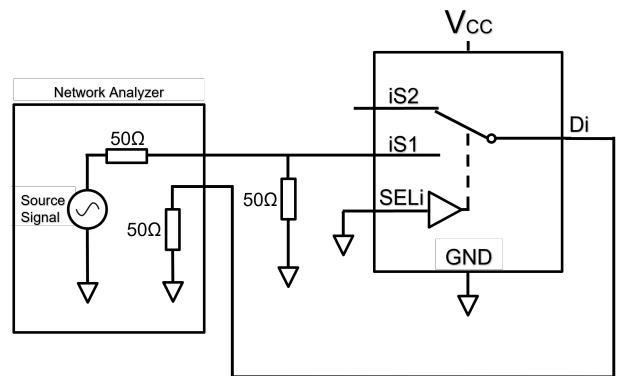


Figure 40. Bandwidth test circuit

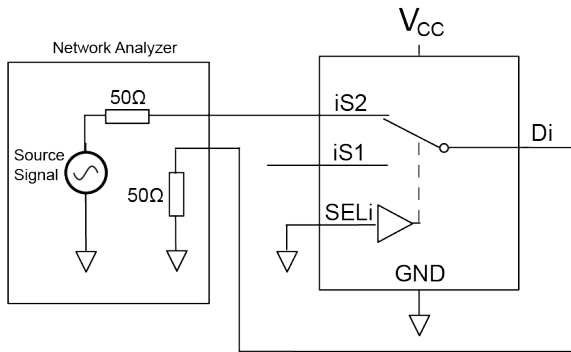


Figure 41. Crosstalk test circuit

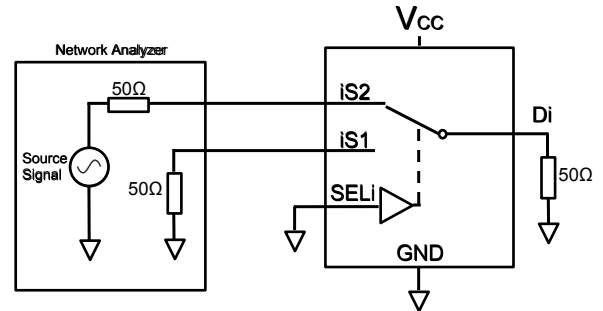


Figure 42. C_{SON} test circuit

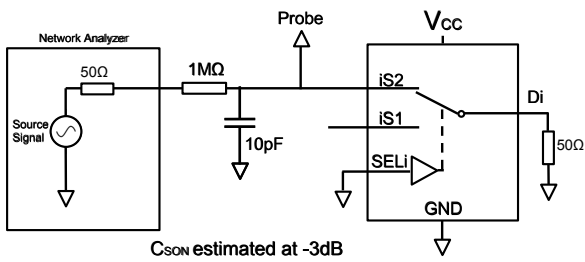
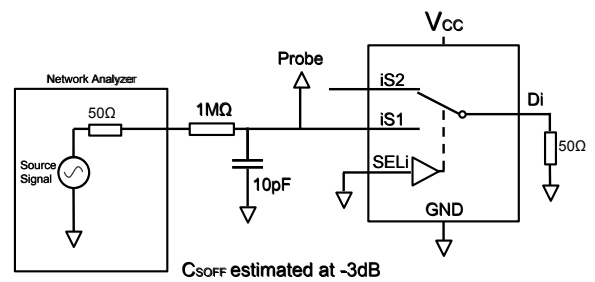


Figure 43. C_{SOFF} test circuit

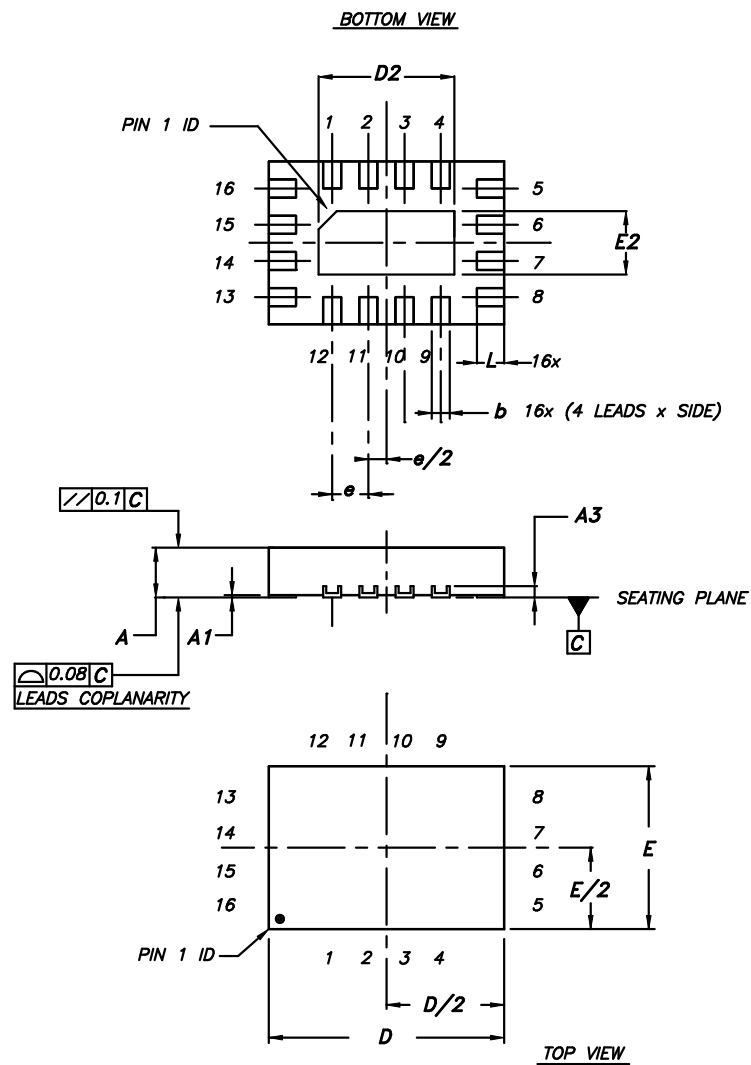


7 Package information

In order to meet environmental requirements, ST offers these devices in different grades of **ECOPACK** packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

7.1 QFN16L (2.6x1.8 mm) package information

Figure 44. QFN16L (2.6x1.8 mm) package outline



7.2 QFN16L (2.6x1.8 mm) packing information

Figure 46. QFN16L (2.6x1.8 mm) carrier tape

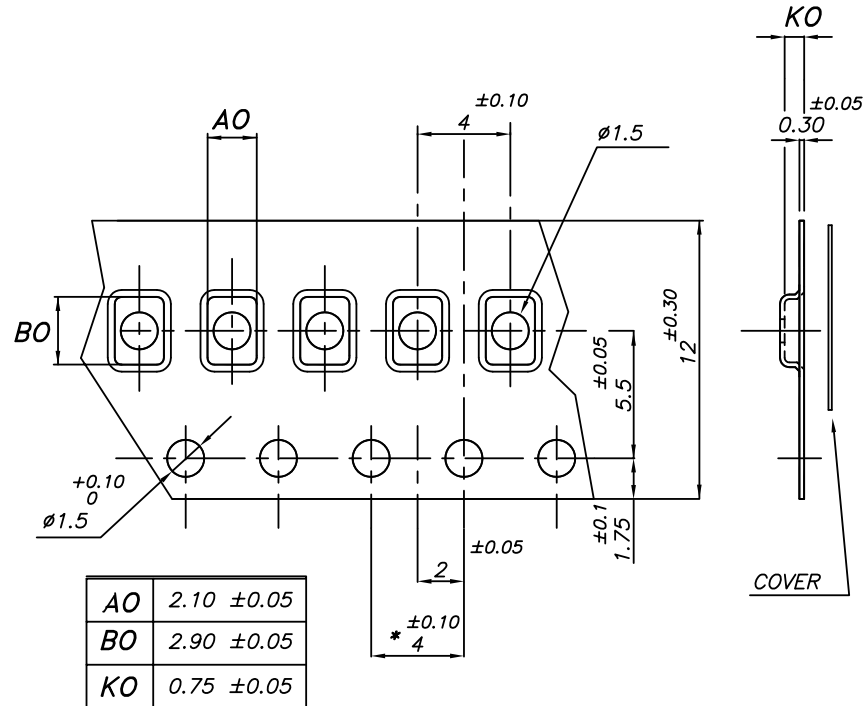
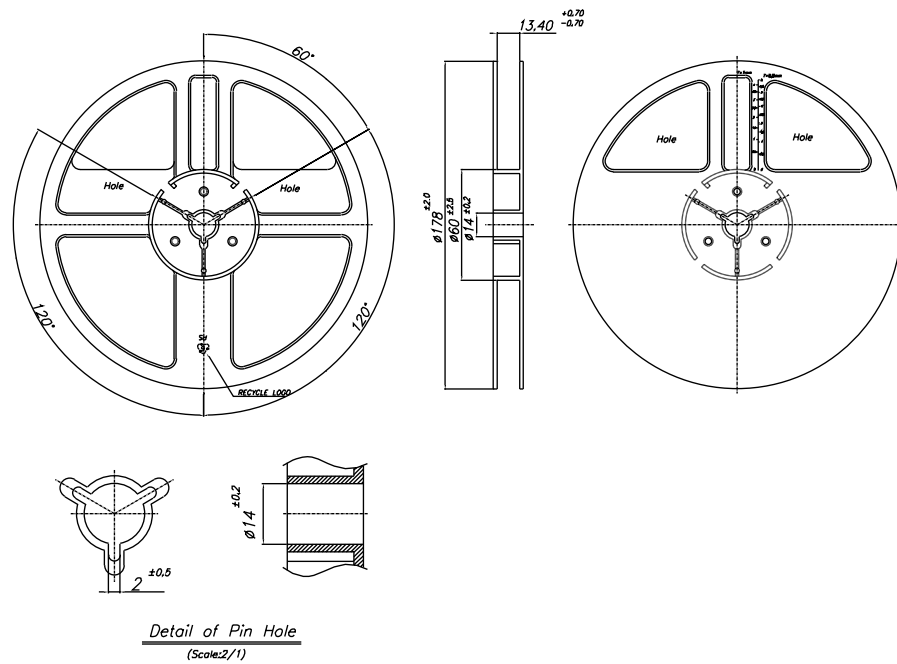


Figure 47. QFN16L (2.6x1.8 mm) reel

- 10 SPROCKET HOLE PITCH CUMULATIVE TOLERANCE ±0.20



8 Ordering information

Table 9. Order code

Order code	Temperature range	Package	Marking
STG5592	-40 °C to 125 °C	QFN16L	592

Revision history

Table 10. Document revision history

Date	Revision	Changes
06-Feb-2024	1	Initial release.

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