

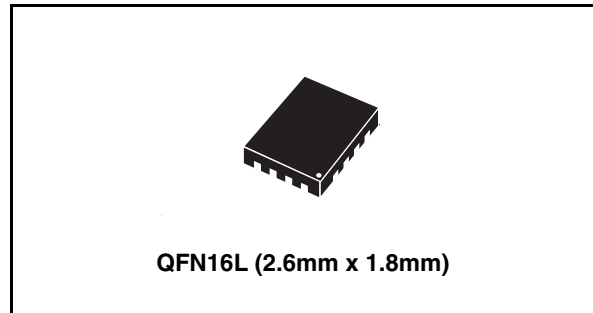


## STG5683

Low voltage dual SPDT switch  
with negative rail capability

### Features

- Distortion-free negative signal throughput down to  $V_{CC} = -5.5V$
- Wide operating voltage range:  
 $V_{CC} (Opr) = 1.65V$  to  $4.5V$  single supply
- Ultra low power dissipation:  
 $I_{CC} = 0.2\mu A$  (Max.) at  $t_A = 85^\circ C$
- Low "ON" resistance  $V_{IN} = 0V$ :  
 $R_{ON} = 0.5\Omega$  (max.  $t_A = 25^\circ C$ ) at  $V_{CC} = 4.3V$
- 4.3V tolerant and 1.8V compatible threshold on digital control input at  $V_{CC} = 1.65$  to  $3.0V$
- Latch-up performance exceeds 300mA (JESD 17)
- ESD performance exceeds JESD22
- 2000-V human-body model (A114-A)



### Description

The STG5683 is a high-speed CMOS low voltage dual analog S.P.D.T. (Single Pole Dual Throw) SWITCH or 2:1 Multiplexer /Demultiplexer Switch fabricated in silicon gate C<sup>2</sup>MOS technology. It is designed to operate from 1.65V to 4.5V, making this device ideal for portable applications.

Additional key features are fast switching speed, Break Before Make Delay Time and Ultra Low Power Consumption. All inputs and outputs are equipped with protection circuits against static discharge, giving them ESD immunity and transient excess voltage.

**Figure 1. Device summary**

Order code	Package	Packaging
STG5683QTR	QFN16L (2.6mm x 1.8mm)	Tape and reel

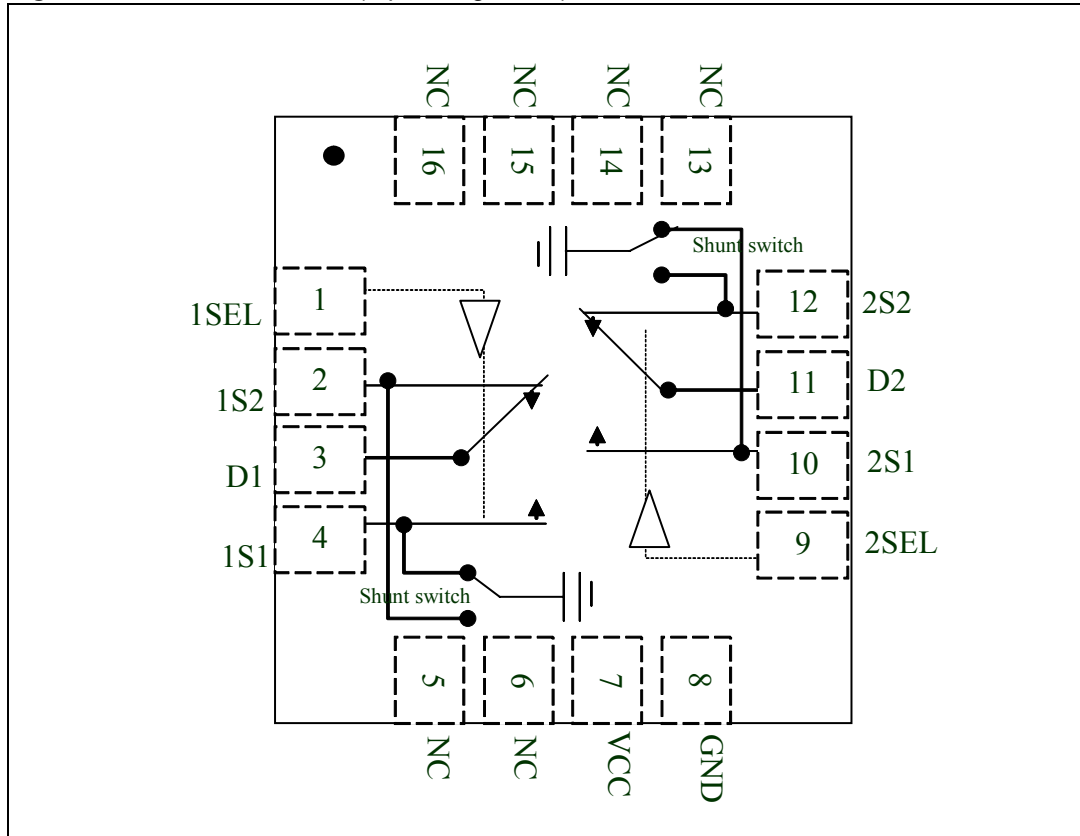
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# 1 Pin settings

## 1.1 Pin connection

Figure 2. Pin connection (top through view)



## 1.2 Pin description

Table 1. Pin description

Pin N°	Symbol	Name and function
4, 2, 10, 12	1S1, 1S2, 2S1, 2S2	Independent channels
3, 11	D1, D2	Common channel
1, 9	1SEL, 2SEL	Control
7	V <sub>CC</sub>	Positive supply voltage
8	GND	Ground (0V)
5,6,13,14,15,16	NC	No connect



### 3 Maximum rating

Stressing the device above the rating listed in the “Absolute Maximum Ratings” table may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the STMicroelectronics SURE Program and other relevant quality documents.

**Table 3. Absolute maximum ratings**

Symbol	Parameter	Value	Unit
$V_{CC}$	Supply voltage	-0.5 to 5.5	V
$V_I$	DC input voltage	- ( $V_{CC} - 6.0V$ ) to $V_{CC} + 0.5$	V
$V_{IC}$	DC control input voltage	-0.5 to 5.5	V
$V_O$	DC output voltage	- ( $V_{CC} - 6.0V$ ) to $V_{CC} + 0.5$	V
$I_{IKC}$	DC input diode current on control pin ( $V_{SEL} < 0V$ )	-50	mA
$I_{IK}$	DC input diode current ( $V_{SEL} < 0V$ )	$\pm 50$	mA
$I_{OK}$	DC output diode current	$\pm 20$	mA
$I_O$	DC output current	$\pm 150$	mA
$I_{OP}$	DC output current peak (pulse at 1ms, 10% duty cycle)	$\pm 400$	mA
$I_{CC}$ or $I_{GND}$	DC $V_{CC}$ or ground current	$\pm 100$	mA
$P_D$	Power dissipation at $T_A = 70^\circ C$ <sup>(1)</sup>	1120	mW
$T_{stg}$	Storage temperature	-65 to 150	$^\circ C$
$T_L$	Lead temperature (10 sec)	300	$^\circ C$

1. Derate above 70°C by 18.5mW/C

### 3.1 Recommended operating conditions

**Table 4. Recommended operating conditions**

Symbol	Parameter		Value	Unit
$V_{CC}$	Supply voltage <sup>(1)</sup>		1.65 to 4.5	V
$V_I$	Input voltage		$V_{CC} - 5.5$ to $V_{CC}$	V
$V_{IC}$	Control input voltage		0 to 4.5	V
$V_O$	Output voltage		$V_{CC} - 5.5$ to $V_{CC}$	V
$T_{op}$	Operating temperature		-40 to 85	°C
dt/dv	Input rise and fall time control input	$V_{CC} = 1.65V$ to $2.7V$	0 to 20	ns/V
		$V_{CC} = 3.0$ to $4.3V$	0 to 10	

1. Truth Table guaranteed: 1.2V to 4.3V

## 4 Electrical characteristics

Table 5. DC specifications

Symbol	Parameter	Test conditions		Value					Unit
		V <sub>CC</sub> (V)		T <sub>A</sub> = 25°C			-40 to 85°C		
				Min	Typ	Max	Min	Max	
V <sub>IH</sub>	High level input voltage	1.65 -1.95		0.65V <sub>CC</sub>			0.65V <sub>CC</sub>		V
		2.3-2.5		1.0			1.4		
		2.7-3.0		1.1			1.5		
		3.3-4.3		1.3			1.6		
V <sub>IL</sub>	Low level input voltage	1.65-1.95				0.5		0.5	V
		2.3-2.5				0.5		0.4	
		2.7-3.0				0.6		0.5	
		3.3-4.3				0.7		0.6	
R <sub>ON</sub>	Switch ON resistance	1.8	V <sub>S</sub> = V <sub>CC</sub> -5.5V to V <sub>CC</sub> ; I <sub>S</sub> = 100mA		3.20	4.0			Ω
		2.7			0.77	0.90			
		3.0			0.64	0.80			
		3.6			0.51	0.65			
		4.3			0.45	0.55			
ΔR <sub>ON</sub>	ON resistance match between channels <sup>(1)</sup>	1.8	V <sub>S</sub> @ R <sub>ON</sub> Max I <sub>S</sub> = 100mA		50				mΩ
		2.7			20				
		3.0			15				
		3.6			15				
		4.3			15				
R <sub>FLAT</sub>	ON resistance flatness <sup>(2)</sup>	1.8	V <sub>S</sub> = V <sub>CC</sub> -5.5V to V <sub>CC</sub> ; I <sub>S</sub> = 100mA		3.0				Ω
		2.7			0.50				
		3.0			0.40				
		3.6			0.25				
		4.3			0.16				
R <sub>SH</sub>	Shunt switch resistance	2.7	S1 or S2 = 10mA		70	100			Ω
I <sub>ON</sub>	Sn ON State Leakage Current	4.3	V <sub>S</sub> = -1.2 to 4.3V V <sub>D</sub> = Open	-0.1		0.1	-1	1	μA

Table 5. DC specifications (continued)

Symbol	Parameter	Test conditions		Value					Unit
		Vcc (V)		T <sub>A</sub> = 25°C			-40 to 85°C		
				Min	Typ	Max	Min	Max	
I <sub>D</sub>	D ON State Leakage Current	4.3	V <sub>S</sub> = Open V <sub>D</sub> = 4.3 to -1.2V	-0.1		0.1	-1	1	μA
I <sub>IH</sub> , I <sub>IL</sub>	SEL Leakage Current	4.3	V <sub>SEL</sub> = 4.3V or GND	-0.1		0.1	-1	1	μA
I <sub>CCLV</sub>	Quiescent Supply Current Low Voltage Driving	4.3	V <sub>1SEL</sub> , V <sub>2SEL</sub> = 1.65V		±37	±50		±100	μA
			V <sub>1SEL</sub> , V <sub>2SEL</sub> = 1.80V		±33	±40		±50	
			V <sub>1SEL</sub> , V <sub>2SEL</sub> = 2.60V		±12	±20		±30	
I <sub>CC</sub>	Quiescent Supply Current	4.3	V <sub>SEL</sub> = V <sub>CC</sub> or GND			±50		±200	nA

- Note 1:  $\Delta R_{on} = \max |mSN - nSNI|$ , where  $m = 1..4$  and  $n = 1..4$ ,  $N = 1..2$
- Flatness is defined as the difference between the maximum and minimum value of on-resistance as measured over the specified analog signal ranges.



Table 6. AC electrical characteristics ( $C_L = 35\text{pF}$ ,  $R_L = 50\Omega$ ,  $t_r = t_f \leq 5\text{ns}$ )

Symbol	Parameter	Test conditions		Value					Unit
		Vcc (V)		T <sub>A</sub> = 25°C			-40 to 85°C		
				Min	Typ	Max	Min	Max	
t <sub>PLH</sub> , t <sub>PHL</sub>	Propagation delay	1.65-1.95			0.45				ns
		2.3-2.7			0.40				
		3.0-3.3			0.30				
		3.6-4.3			0.25				
t <sub>ON</sub>	Turn-ON time	1.65-1.95	V <sub>S</sub> = 0.8V		180	220			ns
		2.3-2.7	V <sub>S</sub> = 1.5V		100	130			
		3.0-3.3			72	95			
		3.6-4.3			58	80			
t <sub>OFF</sub>	Turn-OFF time	1.65-1.95	V <sub>S</sub> = 0.8		64	80			ns
		2.3-2.7	V <sub>S</sub> = 1.5V		41	60			
		3.0-3.3			34	50			
		3.6-4.3			33	50			
t <sub>D</sub>	Break before make time delay	1.65-1.95	C <sub>L</sub> = 35pF R <sub>L</sub> = 50Ω V <sub>S</sub> = V <sub>CC</sub> /2	1	110				ns
		2.3-2.7		1	58				
		3.0-3.3		1	40				
		3.6-4.3		1	23				
Q	Charge injection	1.65-1.95	C <sub>L</sub> = 100pF V <sub>GEN</sub> = 0V		16				pC
		2.3-2.7			25				
		3.0-3.3			34				
		3.6-4.3			46				

Table 7. Analog switch characteristics ( $C_L = 5\text{pF}$ ,  $R_L = 50\Omega$ ,  $T_A = 25^\circ\text{C}$ )

Symbol	Parameter	Test conditions		Value					Unit
		Vcc (V)		$T_A = 25^\circ\text{C}$			$-40 \text{ to } 85^\circ\text{C}$		
				Min	Typ	Max	Min	Max	
OIRR	OFF Isolation <sup>(1)</sup>	2.7 - 4.3	$V_S = 1V_{\text{RMS}}$ , $f = 100\text{kHz}$		-55				dB
Xtalk	Crosstalk	2.7 - 4.3	$V_S = 1V_{\text{RMS}}$ , $f = 100\text{kHz}$		-60				dB
THD	Total harmonic distortion	2.7 - 4.3	$R_L = 32\Omega$ $V_{\text{IN}} = 0.5V_{\text{PP}}$ DC Bias = 0 $f = 20\text{Hz to } 20\text{kHz}$		0.01				%
BW	-3dB bandwidth	2.7 - 4.3	$R_L = 50\Omega$ Signal = 0dBm		33				MHz
$C_{\text{IN}}$	Control pin input capacitance	3.3			6				pF
$C_{\text{D}}$	D Port capacitance when switch is enabled	3.3	$f = 1\text{MHz}$		290				

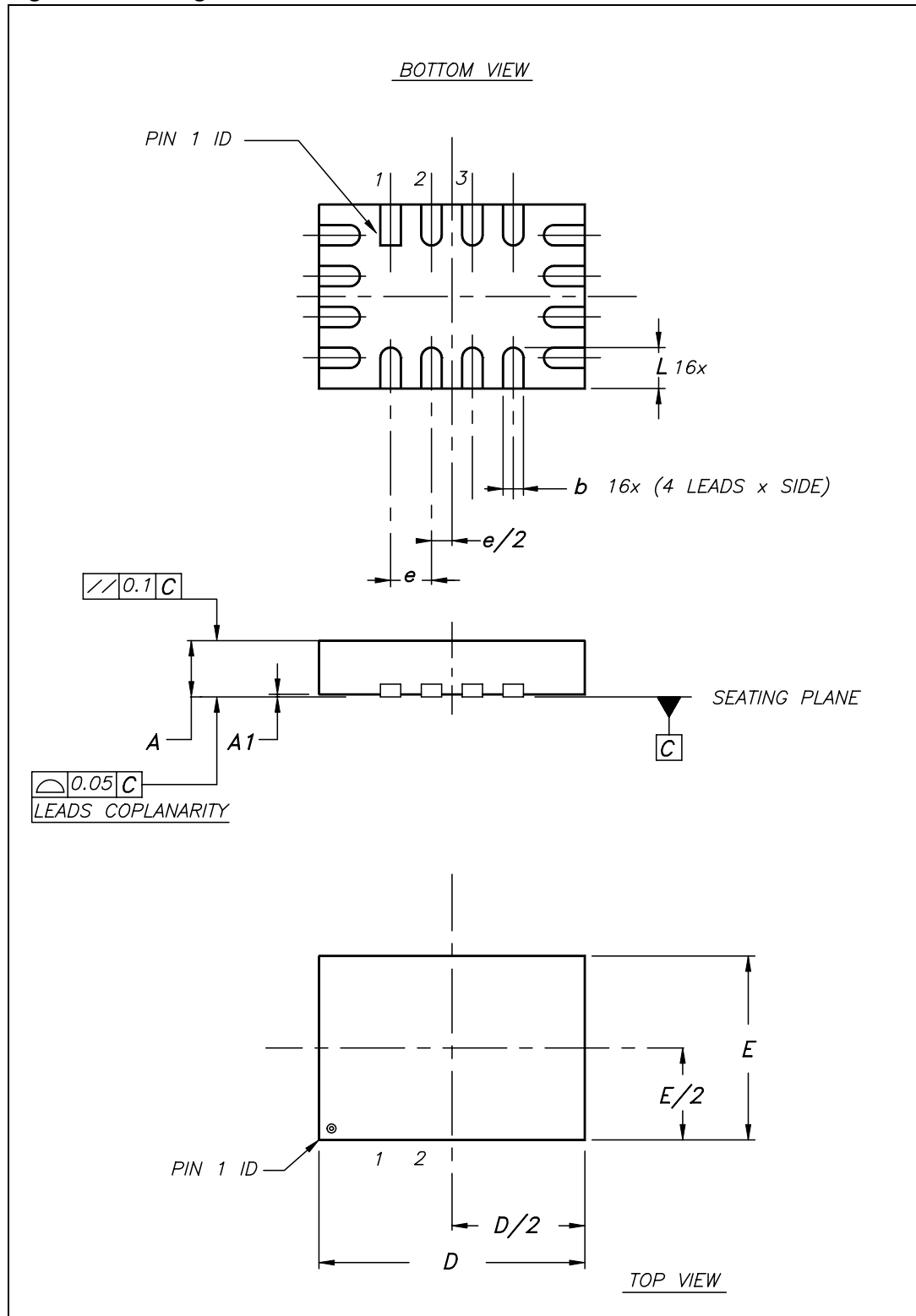
1. Off Isolation =  $20\text{Log}_{10}(V_{\text{D}}/V_{\text{S}})$ ,  $V_{\text{D}}$  = output.  $V_{\text{S}}$  = input to off switch.

## 5 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect . The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: [www.st.com](http://www.st.com)



Figure 5. Package information





## 6 Revision history

**Table 9. Revision history**

Date	Revision	Changes
27-Apr-2007	1	First release
04-May-2007	2	Typo in cover page
05-Jul-2007	3	<a href="#">Table 5 on page 7</a> updated

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