

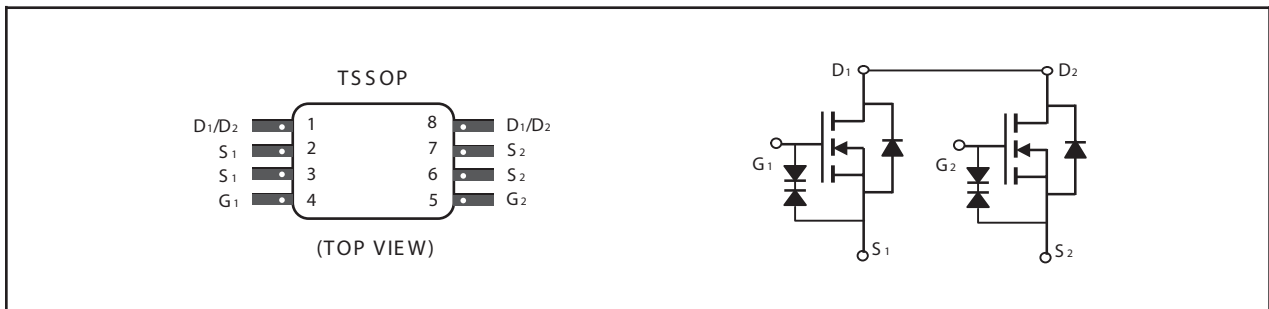


Dual N-Channel Enhancement Mode Field Effect Transistor

PRODUCT SUMMARY		
V _{DSS}	I _D	R _{DS(ON)} (mΩ) Max
20V	7A	14.5 @ V _{GS} =4.5V
		15.0 @ V _{GS} =4.0V
		17.0 @ V _{GS} =3.7V
		19.5 @ V _{GS} =3.1V
		23.0 @ V _{GS} =2.5V

FEATURES

- Super high dense cell design for low R_{DS(ON)}.
- Rugged and reliable.
- Surface Mount Package.
- ESD HBM > 2KV.



ABSOLUTE MAXIMUM RATINGS (T_A=25°C unless otherwise noted)

Symbol	Parameter	Limit	Units
V _{DS}	Drain-Source Voltage	20	V
V _{GS}	Gate-Source Voltage	±12	V
I _D	Drain Current-Continuous ^a	T _A =25°C	7.0
		T _A =70°C	5.6
I _{DM}	-Pulsed ^b	80	A
P _D	Maximum Power Dissipation ^a	T _A =25°C	2.0
		T _A =70°C	1.28
T _J , T _{STG}	Operating Junction and Storage Temperature Range	-55 to 150	°C

THERMAL CHARACTERISTICS

R _{θJA}	Thermal Resistance, Junction-to-Ambient ^a	62.5	°C/W
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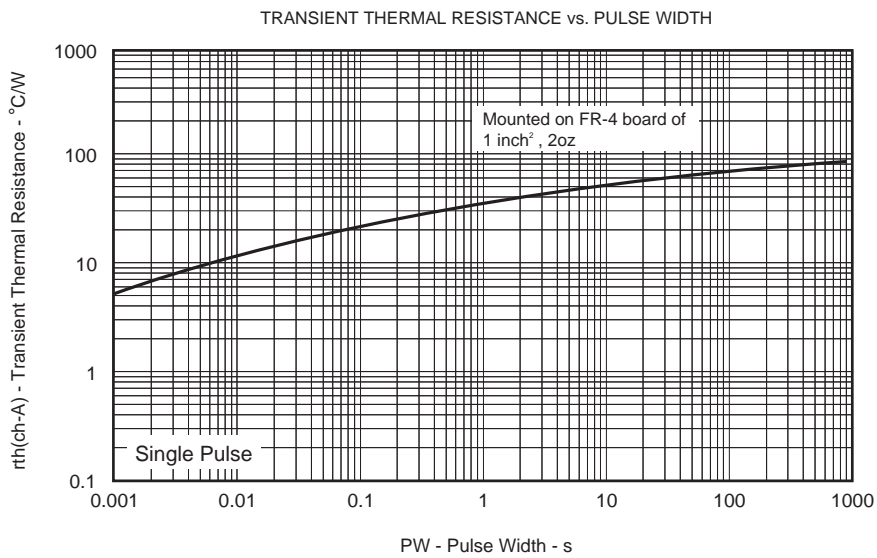
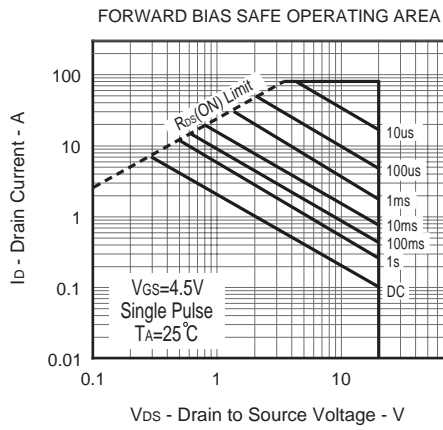
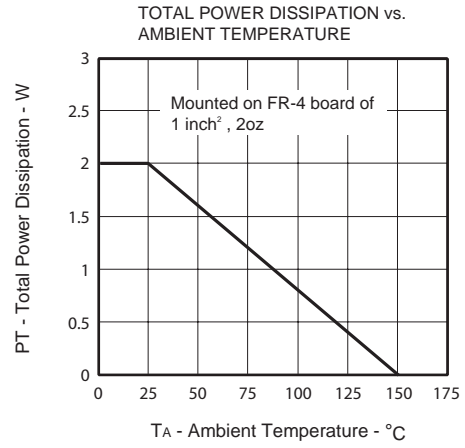
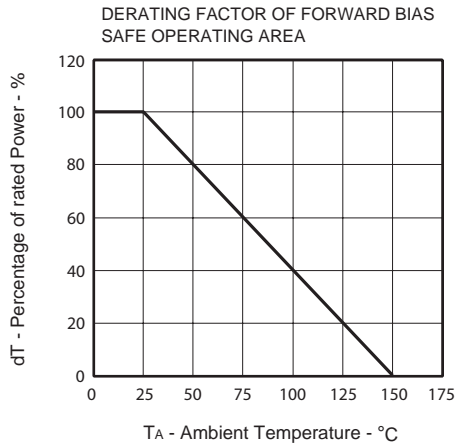
ELECTRICAL CHARACTERISTICS (T_A=25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
OFF CHARACTERISTICS						
BV _{DSS}	Drain-Source Breakdown Voltage	V _{GS} =0V , I _D =250uA	20			V
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} =16V , V _{GS} =0V			1	uA
I _{GSS}	Gate-Body Leakage Current	V _{GS} = ±12V , V _{DS} =0V			±10	uA
ON CHARACTERISTICS						
V _{GS(th)}	Gate Threshold Voltage	V _{DS} =V _{GS} , I _D =1mA	0.5	0.8	1.5	V
R _{DS(ON)}	Drain-Source On-State Resistance	V _{GS} =4.5V , I _D =3.5A	11.5	13.0	14.5	m ohm
		V _{GS} =4.0V , I _D =3.5A	12.0	13.5	15.0	m ohm
		V _{GS} =3.7V , I _D =3.5A	13.0	15.0	17.0	m ohm
		V _{GS} =3.1V , I _D =3.5A	14.0	17.0	19.5	m ohm
		V _{GS} =2.5V , I _D =3.5A	15.0	19.0	23.0	m ohm
g _{FS}	Forward Transconductance	V _{DS} =5V , I _D =3.5A		22		S
DYNAMIC CHARACTERISTICS ^c						
C _{ISS}	Input Capacitance	V _{DS} =10V, V _{GS} =0V f=1.0MHz		316		pF
C _{OSS}	Output Capacitance			159		pF
C _{RSS}	Reverse Transfer Capacitance			92		pF
SWITCHING CHARACTERISTICS ^c						
t _{D(ON)}	Turn-On Delay Time	V _{DD} =16V I _D =3.5A V _{GS} =4.5V R _{GEN} = 6 ohm		64		ns
t _r	Rise Time			275		ns
t _{D(OFF)}	Turn-Off Delay Time			900		ns
t _f	Fall Time			750		ns
Q _g	Total Gate Charge			8.4		nC
Q _{gs}	Gate-Source Charge	V _{DS} =16V, I _D =7A, V _{GS} =4.5V		1.4		nC
Q _{gd}	Gate-Drain Charge			4.5		nC
DRAIN-SOURCE DIODE CHARACTERISTICS AND MAXIMUM RATINGS						
V _{SD}	Diode Forward Voltage	V _{GS} =0V, I _S =1.0A		0.78	1.2	V
Notes a.Surface Mounted on FR4 Board, t < 10sec. b.Pulse Test:Pulse Width < 10us, Duty Cycle < 1%. c.Guaranteed by design, not subject to production testing.						

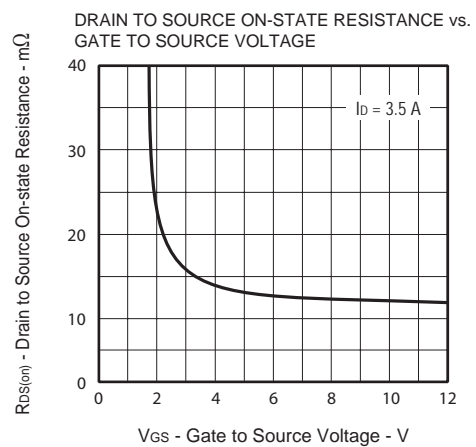
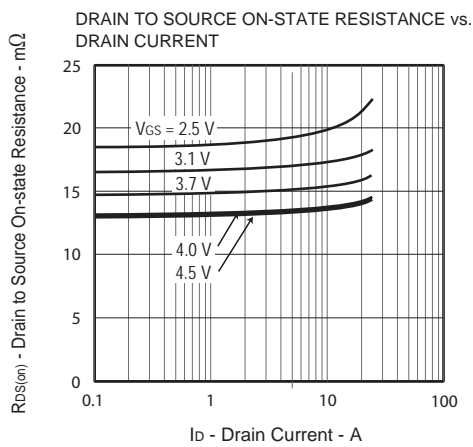
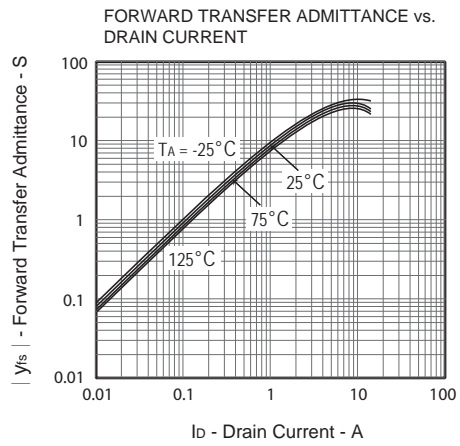
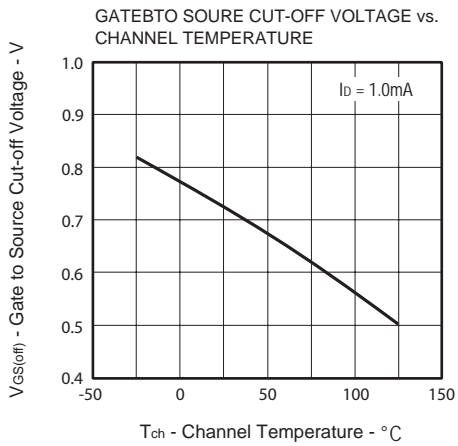
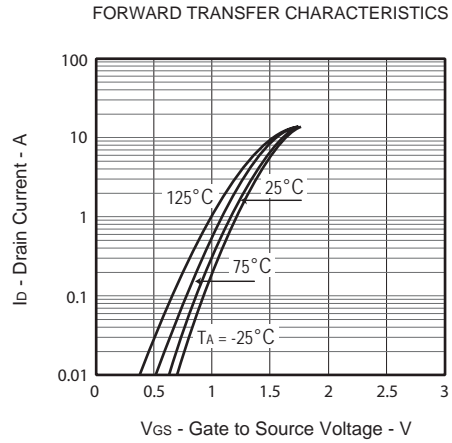
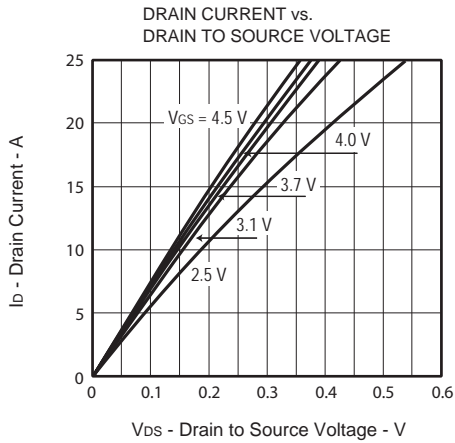
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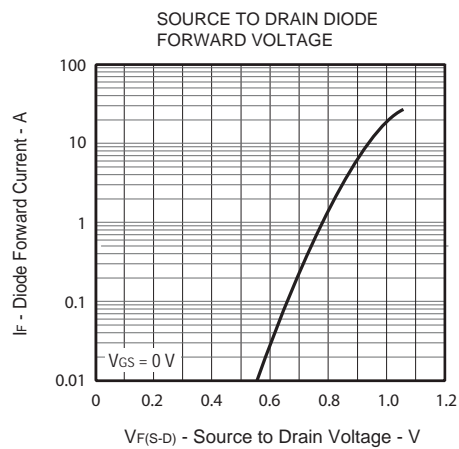
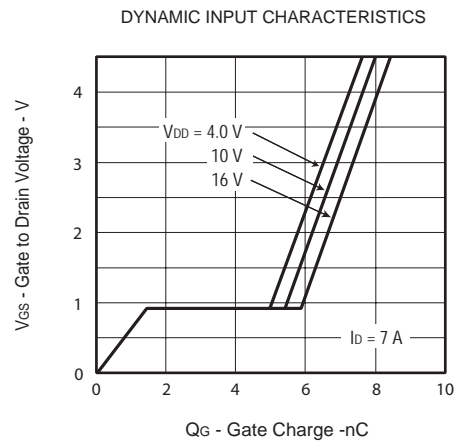
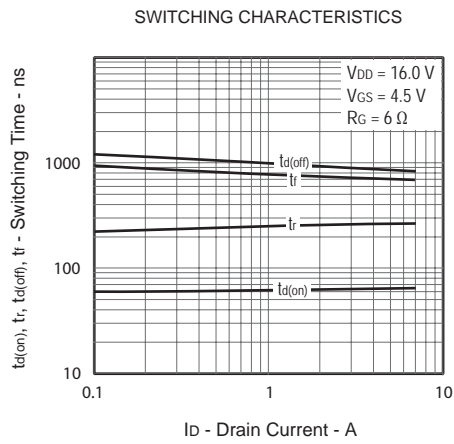
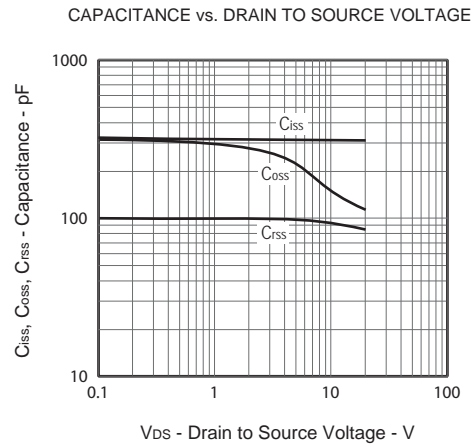
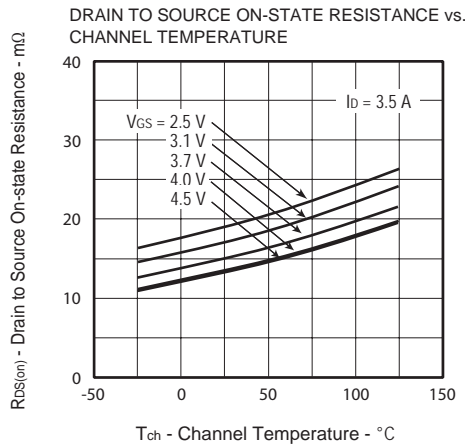


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PACKAGE OUTLINE DIMENSIONS

TSSOP-8

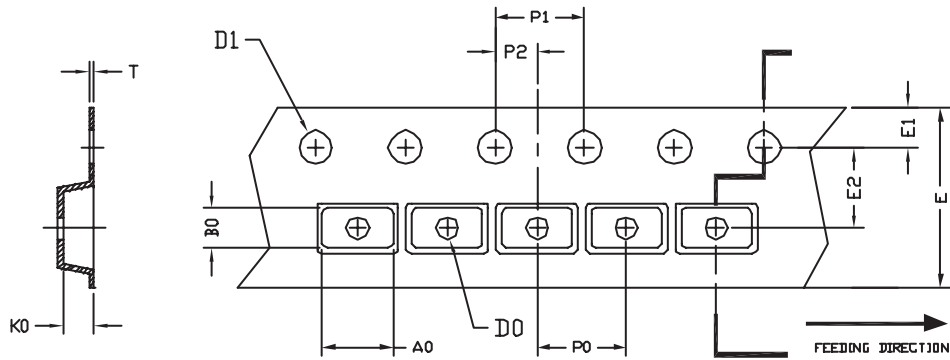
The drawing includes a top view showing a rectangular package with eight leads, a side view showing the lead profile, and two circular detail views labeled 'DETAIL A'. The top view shows dimensions D (width), e (lead pitch), b (lead width), and A1 (lead thickness). The side view shows dimensions E (height), E1 (lead height), and c (lead thickness). The detail views show dimensions A (lead thickness), A2 (lead thickness), L (lead length), L1 (lead length), and theta_1 (lead angle).

SYMBOLS	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	0.85	1.20	0.033	0.047
A1	0.05	0.15	0.002	0.006
A2	0.80	1.05	0.031	0.041
b	0.19	0.30	0.007	0.012
c	0.127		0.005	
D	2.90	3.10 [Ⓢ]	0.114	0.122 [Ⓢ]
E	4.30	4.50 [Ⓢ]	0.169	0.177 [Ⓢ]
E1	6.20	6.60	0.244	0.260
e	0.65BSC		0.025BSC	
L	0.50	0.70	0.020	0.028
L1	1.00		0.039	
theta_1	0°	8°	0°	8°

Notes: 1. This drawing is for general information only. Refer to JEDEC Drawing MO-153, Variation AA, for proper dimensions, tolerances, datums, etc.
 2. Dimension D does not include mold Flash, protrusions or gate burrs. Mold Flash, protrusions and gate burrs shall not exceed 0.15 mm (0.006 in) per side.
 3. Dimension E does not include inter-lead Flash or protrusions. Inter-lead Flash and protrusions shall not exceed 0.25mm (0.010 in) per side.
 4. Dimension b does not include Dambar protrusion. Allowable Dambar protrusion shall be 0.08 mm total in excess of the b dimension at maximum material condition. Dambar cannot be located on the lower radius of the foot. Minimum space between protrusion and adjacent lead is 0.07 mm.
 5. Dimension D and E to be determined at Datum Plane H.

TSSOP-8 Tape and Reel Data

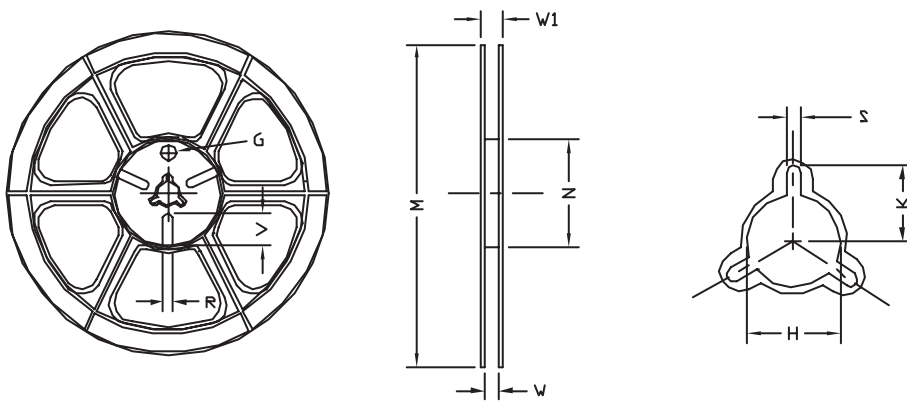
TSSOP-8 Carrier Tape



UNIT : mm

PACKAGE	A0	B0	K0	D0	D1	E	E1	E2	P0	P1	P2	T
TSSOP 8	6.08	4.40	1.60	$\phi 1.50$ +0.1 -0.0	$\phi 1.50$ +0.1 -0.0	12.00 ± 0.3	1.75	5.50 ± 0.05	8.00	4.00	2.00 ± 0.05	0.30 ± 0.05

TSSOP-8 Reel



UNIT : mm

TAPE SIZE	REEL SIZE	M	N	W	W1	H	K	S	G	R	V
12 mm	$\phi 330$	330	100	12.5	16.0	$\phi 13.0$ +0.5 -0.2	10.6	2.0 ± 0.5	---	---	---

TOP MARKING DEFINITION

