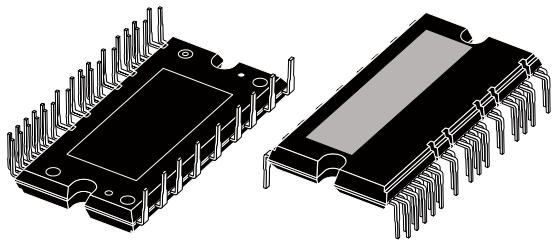
STGIPL30C60

SLLIMM™ (small low-loss intelligent molded module) IPM, 3-phase inverter, 30 A, 600 V short-circuit rugged IGBT

Datasheet - production data



SDIP-38L

Features

- IPM 30 A, 600 V 3-phase IGBT inverter bridge including control ICs for gate driving and free-wheeling diodes
- Short-circuit rugged IGBTs
- $V_{CE(sat)}$ negative temperature coefficient
- 3.3 V, 5 V, 15 V CMOS/TTL input comparators with hysteresis and pull-down/pull-up resistors
- Undervoltage lockout
- Internal bootstrap diode
- Interlocking function
- Smart shutdown function
- Comparators for fault protection against overtemperature and overcurrent
- Op-amps for advanced current sensing
- DBC substrate leading to low thermal resistance
- Isolation rating of 2500 V_{rms}/min.
- 5 kΩ NTC for temperature control
- UL recognized: UL 1557 file E81734

Applications

- 3-phase inverters for motor drives
- Home appliances, such as washing machines, refrigerators, air conditioners and sewing machines

Description

This intelligent power module provides a compact, high performance AC motor drive in a simple, rugged design. Combining ST proprietary control ICs with the most advanced short-circuit rugged IGBT system technology, this device is ideal for 3-phase inverters in applications such as home appliances and air conditioners. SLLIMM™ is a trademark of STMicroelectronics.

Table 1. Device summary

Order code	Marking	Package	Packing
STGIPL30C60	GIPL30C60	SDIP-38L	Tube

Contents

1 Internal block diagram and pin configuration

Figure 1. Internal block diagram

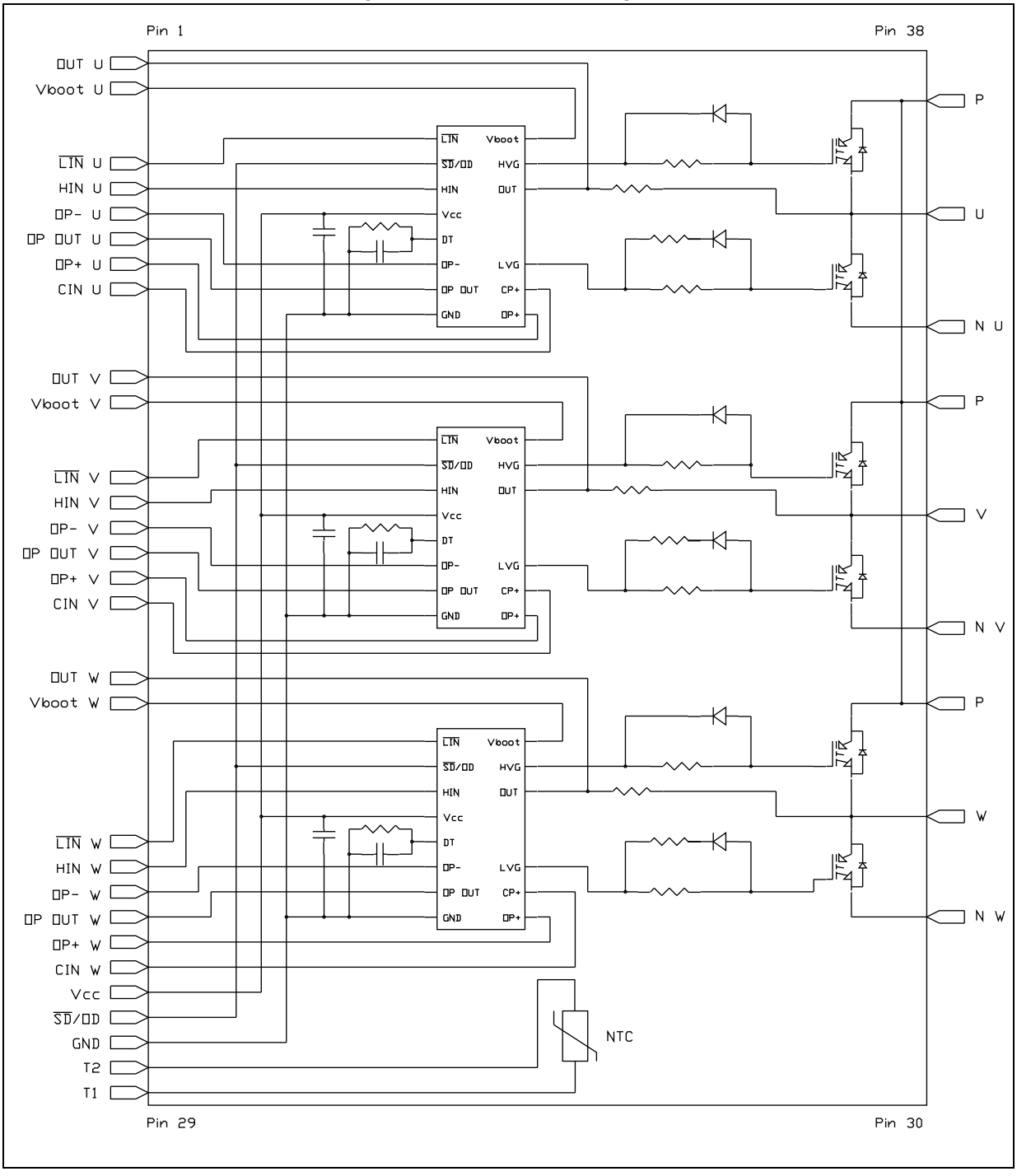


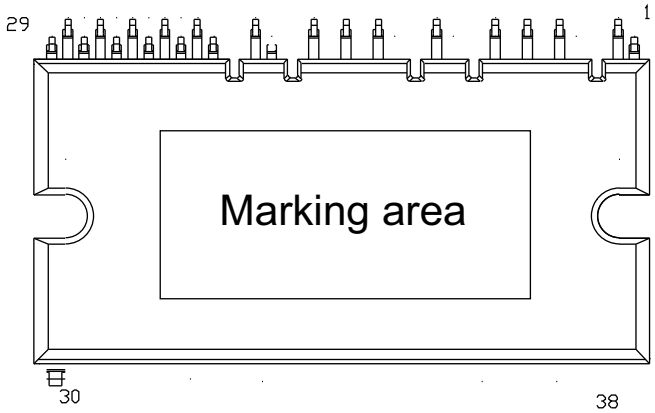
Table 2. Pin description

Pin	Symbol	Description
1	OUT_U	High-side reference output for U phase
2	$V_{boot\ U}$	Bootstrap voltage for U phase
3	$\overline{LIN}_U$	Low-side logic input for U phase
4	HIN_U	High-side logic input for U phase
5	$OP\text{-}_U$	Op-amp inverting input for U phase
6	$OP_{OUT\ U}$	Op-amp output for U phase
7	$OP+_U$	Op-amp non-inverting input for U phase
8	CIN_U	Comparator input for U phase
9	OUT_V	High-side reference output for V phase
10	$V_{boot\ V}$	Bootstrap voltage for V phase
11	$\overline{LIN}_V$	Low-side logic input for V phase
12	HIN_V	High-side logic input for V phase
13	$OP\text{-}_V$	Op-amp inverting input for V phase
14	$OP_{OUT\ V}$	Op-amp output for V phase
15	$OP+_V$	Op-amp non-inverting input for V phase
16	CIN_V	Comparator input for V phase
17	OUT_W	High-side reference output for W phase
18	$V_{boot\ W}$	Bootstrap voltage for W phase
19	$\overline{LIN}_W$	Low-side logic input for W phase
20	HIN_W	High-side logic input for W phase
21	$OP\text{-}_W$	Op-amp inverting input for W phase
22	$OP_{OUT\ W}$	Op-amp output for W phase
23	$OP+_W$	Op-amp non-inverting input for W phase
24	CIN_W	Comparator input for W phase
25	V_{CC}	Low voltage power supply
26	$\overline{SD/OD}$	Shutdown logic input (active low) / open drain (comparator output)
27	GND	Ground
28	T_2	NTC thermistor terminal 2
29	T_1	NTC thermistor terminal 1
30	N_W	Negative DC input for W phase
31	W	W phase output
32	P	Positive DC input
33	N_V	Negative DC input for V phase
34	V	V phase output

Table 2. Pin description (continued)

Pin	Symbol	Description
35	P	Positive DC input
36	N_U	Negative DC input for U phase
37	U	U phase output
38	P	Positive DC input

Figure 2. Pin layout (bottom view)



2 Electrical ratings

2.1 Absolute maximum ratings

Table 3. Inverter part

Symbol	Parameter	Value	Unit
V_{PN}	Supply voltage applied among P-N_U, N_V, N_W	450	V
$V_{PN(surge)}$	Supply voltage (surge) among P-N_U, N_V, N_W	500	V
V_{CES}	Each IGBT collector-emitter voltage (V_{IN}(1) = 0)	600	V
± I_C	Each IGBT continuous collector current at T_C = 25 °C	30	A
± I_{CP}(2)	Each IGBT pulsed collector current	60	A
P_{TOT}	Each IGBT total dissipation at T_C = 25 °C	56	W
t_{scw}	Short-circuit withstand time, V_{CE} = 0.5 $V_{(BR)CES}$ T_j = 125 °C, V_{CC} = V_{boot} = 15 V, V_{IN}(1) = 0 to 5 V	5	µs

1. Applied among HIN_i, $\overline{LIN}$ and GND for i = U, V, W.
2. Pulse width limited by max. junction temperature.

Table 4. Control part

Symbol	Parameter	Min.	Max.	Unit
V_{OUT}	Output voltage applied among OUT_U, OUT_V, OUT_W - GND	V_{boot} - 21	V_{boot} + 0.3	V
V_{CC}	Low voltage power supply	- 0.3	21	V
V_{CIN}	Comparator input voltage	- 0.3	V_{CC} + 0.3	V
V_{op+}	Op-amp non-inverting input	- 0.3	V_{CC} + 0.3	V
V_{op-}	Op-amp inverting input	- 0.3	V_{CC} + 0.3	V
V_{boot}	Bootstrap voltage	- 0.3	620	V
V_{IN}	Logic input voltage applied among HIN, $\overline{LIN}$ and GND	- 0.3	15	V
$V_{SD/\overline{OD}}$	Open drain voltage	- 0.3	15	V
dV_{OUT}/dt	Allowed output slew rate		50	V/ns

Table 5. Total system

Symbol	Parameter	Value	Unit
V_{ISO}	Isolation withstand voltage applied between each pin and heatsink plate (AC voltage, t = 60 s)	2500	V
T_j	Power chip operating junction temperature	-40 to 150	°C
T_C	Module case operation temperature	-40 to 125	°C

2.2 Thermal data

Table 6. Thermal data

Symbol	Parameter	Value	Unit
$R_{th(j-c)}$	Thermal resistance junction-case single IGBT	2.2	°C/W
	Thermal resistance junction-case single diode	5	°C/W

Figure 3. Maximum $I_{C(RMS)}$ current vs switching frequency(1)

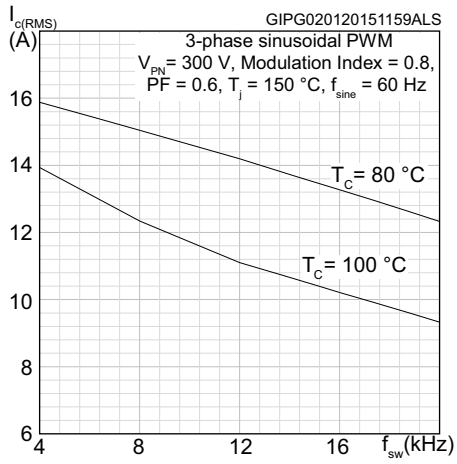
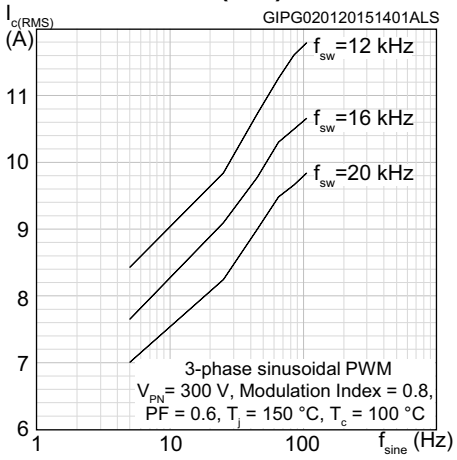


Figure 4. Maximum $I_{C(RMS)}$ current vs f_{sine} (1)



1. Simulated curves refer to typical IGBT parameters and maximum R_{thj-c}.

3 Electrical characteristics

T_j = 25 °C unless otherwise specified.

Table 7. Inverter part

Symbol	Parameter	Test conditions	Value			Unit
			Min.	Typ.	Max.	
$V_{CE(sat)}$	Collector-emitter saturation voltage	V_{CC} = V_{Boot} = 15 V, V_{IN}(1) = 0 to 5 V, I_C = 30 A	-	1.9		V
		V_{CC} = V_{Boot} = 15 V, V_{IN}(1) = 0 to 5 V, I_C = 30 A, T_j = 125 °C	-	2.2		
I_{CES}	Collector-cut off current (V_{IN}(1) = 0 (logic state)	V_{CE} = 550 V V_{CC} = V_{boot} = 15 V	-		150	µA
V_F	Diode forward voltage	V_{IN}(1) = 0 “logic state”, I_C = 30 A	-	2.0	2.3	V
Inductive load switching time and energy						
t_{on}	Turn-on time	V_{DD} = 300 V, V_{CC} = V_{boot} = 15 V, V_{IN}(1)= 0 to 5 V, I_C = 30 A (see *Figure 5*)	-	440		ns
$t_{c(on)}$	Crossover time (on)		-	190		
t_{off}	Turn-off time		-	780		
$t_{c(off)}$	Crossover time (off)		-	135		
t_{rr}	Reverse recovery time		-	100		
E_{on}	Turn-on switching losses		-	870		µJ
E_{off}	Turn-off switching losses		-	740		

1. Applied among HIN_i $\overline{LIN_i}$ and GND for i = U, V, W.

Note: t_{on} and t_{off} include the propagation delay time of the internal drive. $t_{C(ON)}$ and $t_{C(OFF)}$ are the switching time of IGBT itself under the internally given gate driving condition.

Figure 5. Switching time test circuit

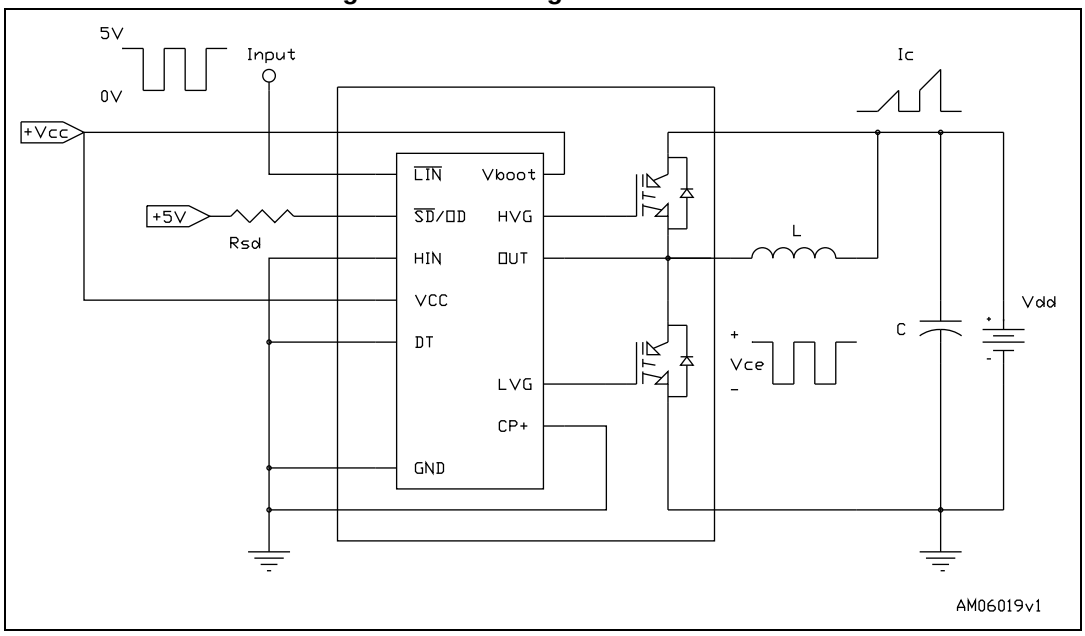
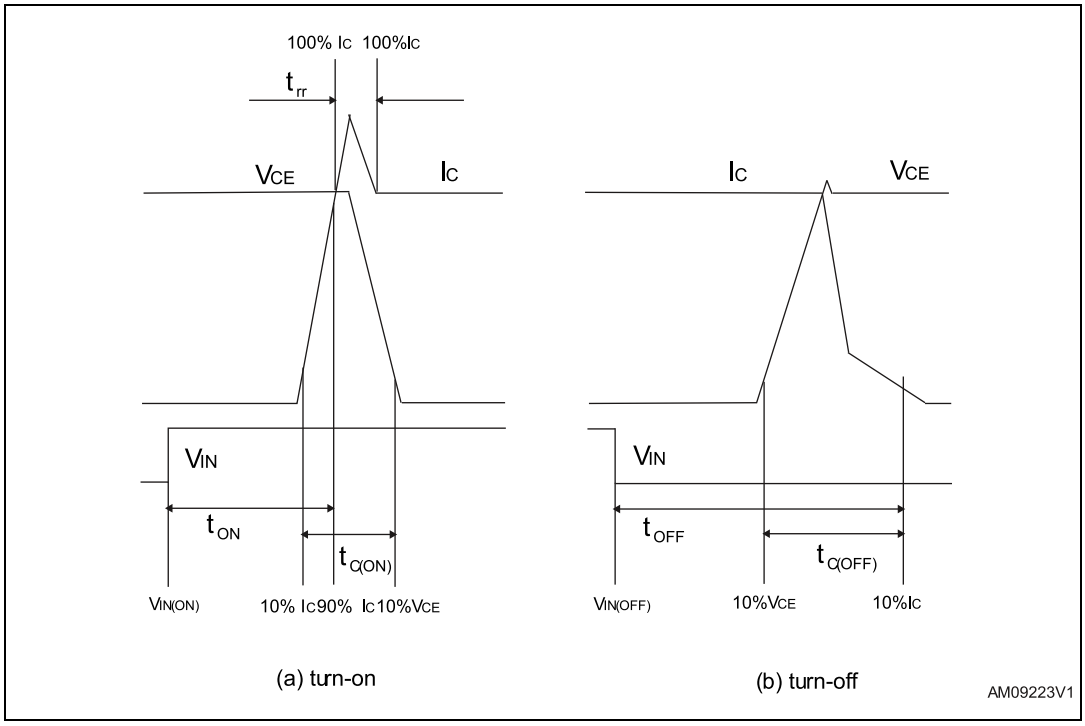


Figure 6. Switching time definition



Note: Figure 5 refers to HIN inputs (active high). For /LIN inputs (active low), VIN polarity has to be inverted for turn-on and turn-off.

3.1 Control part

Table 8. Low voltage power supply (V_{CC} = 15 V unless otherwise specified)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{cc_hys}	V_{cc} UV hysteresis		1.2	1.5	1.8	V
V_{cc_thON}	V_{cc} UV turn-on threshold		11.5	12	12.5	V
V_{cc_thOFF}	V_{cc} UV turn-off threshold		10	10.5	11	V
I_{qccu}	Undervoltage quiescent supply current	V_{CC} = 10 V; $\overline{SD}$/OD = 5 V; $\overline{LIN}$ = 5 V; H_{IN} = 0, C_{IN} = 0			450	µA
I_{qcc}	Quiescent current	V_{CC} = 15 V; $\overline{SD}$/OD = 5 V; $\overline{LIN}$ = 5 V; H_{IN} = 0, C_{IN} = 0			3.5	mA
V_{ref}	Internal comparator (CIN) reference voltage		0.5	0.54	0.58	V

Table 9. Bootstrapped voltage (V_{CC} = 15 V unless otherwise specified)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{BS_hys}	V_{BS} UV hysteresis		1.2	1.5	1.8	V
V_{BS_thON}	V_{BS} UV turn-on threshold		11.1	11.5	12.1	V
V_{BS_thOFF}	V_{BS} UV turn-off threshold		9.8	10	10.6	V
I_{QBSU}	Undervoltage V_{BS} quiescent current	V_{BS} < 9 V; $\overline{SD}$/OD = 5 V; $\overline{LIN}$ and HIN = 5 V; C_{IN} = 0		70	110	µA
I_{QBS}	V_{BS} quiescent current	V_{BS} = 15 V; $\overline{SD}$/OD = 5 V; $\overline{LIN}$ and HIN = 5 V; C_{IN} = 0		200	300	µA
$R_{DS(on)}$	Bootstrap driver on-resistance	LVG on		120		Ω

Table 10. Logic inputs (V_{CC} = 15 V unless otherwise specified)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{il}	Low logic level voltage		0.8		1.1	V
V_{ih}	High logic level voltage		1.9		2.25	V
I_{HINh}	HIN logic “1” input bias current	HIN = 15 V	110	175	260	µA
I_{HINl}	HIN logic “0” input bias current	HIN = 0 V			1	µA
I_{LINl}	$\overline{LIN}$ logic “1” input bias current	$\overline{LIN}$ = 0 V	3	6	20	µA
I_{LINh}	$\overline{LIN}$ logic “0” input bias current	$\overline{LIN}$ = 15 V			1	µA

Table 10. Logic inputs (V_{CC} = 15 V unless otherwise specified) (continued)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SDh}	$\overline{SD}$ logic “0” input bias current	$\overline{SD}$ = 15 V	30	120	300	µA
I_{SDl}	$\overline{SD}$ logic “1” input bias current	$\overline{SD}$ = 0 V			3	µA
Dt	Dead time	see *Figure 9* and *Table 15*		600		ns

Table 11. Op-amp characteristics (V_{CC} = 15 V unless otherwise specified)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{io}	Input offset voltage	V_{ic} = 0 V, V_o = 7.5 V			6	mV
I_{io}	Input offset current	V_{ic} = 0 V, V_o = 7.5 V		4	40	nA
I_{ib}	Input bias current (1)			100	200	nA
V_{icm}	Input common mode voltage range		0			V
V_{OL}	Low level output voltage	R_L = 10 kΩ to V_{CC}		75	150	mV
V_{OH}	High level output voltage	R_L = 10 kΩ to GND	14	14.7		V
I_o	Output short-circuit current	Source, V_{id} = +1; V_o = 0 V	16	30		mA
		Sink, V_{id} = -1; V_o = V_{CC}	50	80		mA
SR	Slew rate	V_i = 1 ¸ 4 V; C_L = 100 pF; unity gain	2.5	3.8		V/ms
GBWP	Gain bandwidth product	V_o = 7.5 V	8	12		MHz
A_{vd}	Large signal voltage gain	R_L = 2 kΩ	70	85		dB
SVR	Supply voltage rejection ratio	vs V_{CC}	60	75		dB
CMRR	Common mode rejection ratio		55	70		dB

1. The direction of input current is out of the IC.

Table 12. Sense comparator characteristics (V_{CC} = 15 V unless otherwise specified)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$I_{ib(i)}$	Input bias current	$V_{CIN(i)}$ = 1 V, i = U, V or W	-		3	µA
V_{ol}	Open drain low level output voltage	I_{od} = 3 mA	-		0.5	V
t_{d_comp}	Comparator delay	$\overline{SD}$/OD pulled to 5 V through 100 kΩ resistor	-	90	130	ns
SR	Slew rate	C_L = 180 pF; R_{pu} = 5 kΩ	-	60		V/µs
t_{sd}	Shutdown to high / low-side driver propagation delay	V_{OUT} = 0, V_{boot} = V_{CC}, V_{IN} = 0 to 3.3 V	50	125	200	ns
t_{isd}	Comparator triggering to high / low-side driver turn-off propagation delay	Measured applying a voltage step from 0 V to 3.3 V to pin CIN_i	50	200	250	

Table 13. Truth table

Conditions	Logic input (V_I)			Output	
	$\overline{SD}$/OD	$\overline{LIN}$	HIN	LVG	HVG
Shutdown enable half-bridge 3-state	L	X	X	L	L
Interlocking half-bridge 3-state	H	L	H	L	L
0 “logic state” half-bridge 3-state	H	H	L	L	L
1 “logic state” low-side direct driving	H	L	L	H	L
1 “logic state” high-side direct driving	H	H	H	L	H

Note: X: don’t care

3.1.1 NTC thermistor

Table 14. NTC thermistor

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
R_{25}	Resistance	T = 25 °C		5		kΩ
R_{125}	Resistance	T = 125 °C		300		Ω
B	B-constant	T = 25 °C to 85 °C		3340		K
T	Operating temperature		-40		125	°C

Below the relation between resistance variation vs temperature:

Equation 1:

$$R(T) = R_{25} \cdot e^{B\left(\frac{1}{T} - \frac{1}{298}\right)}$$

Where T is the temperature in Kelvin.

Figure 7. NTC resistance vs temperature

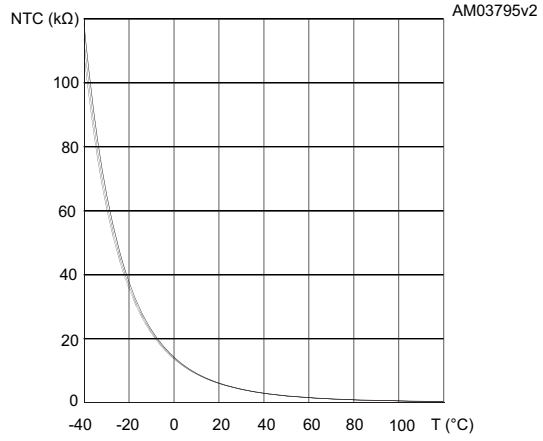
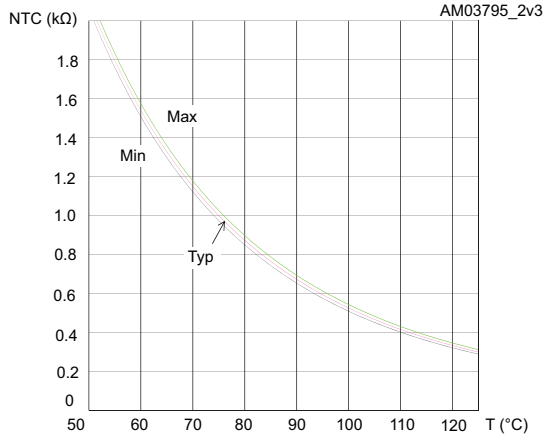
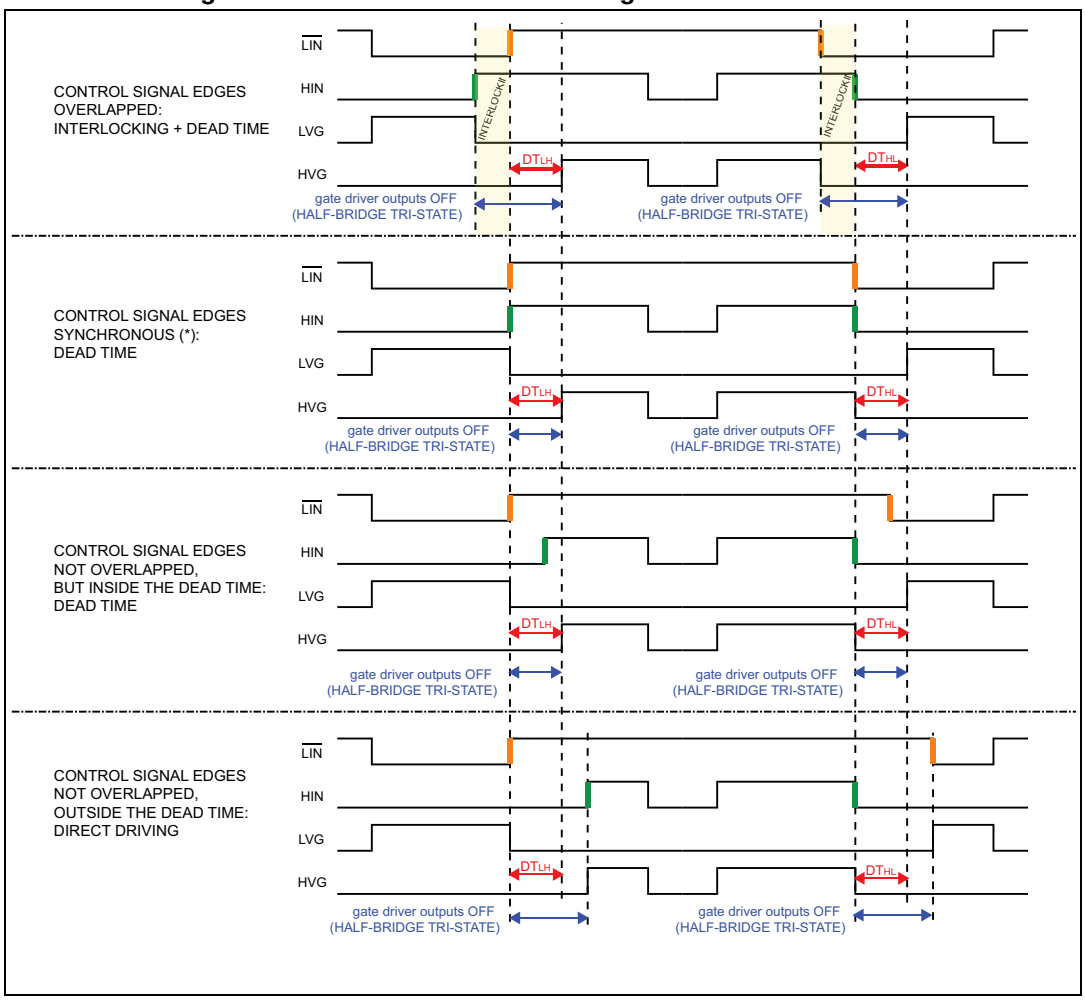


Figure 8. NTC resistance vs temperature zoom



3.2 Waveform definitions

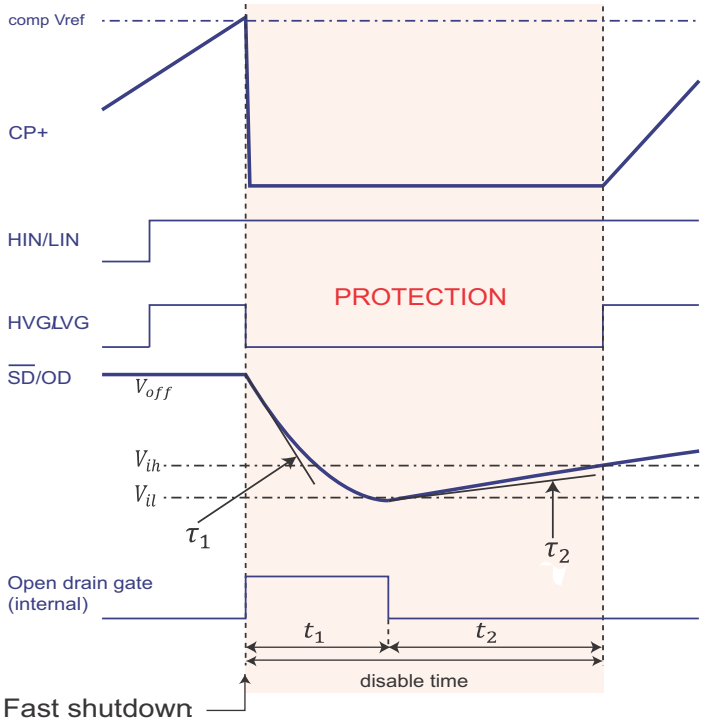
Figure 9. Dead time and interlocking waveform definitions



4 Smart shutdown function

The STGIPL30C60 integrates a comparator for fault sensing purposes. The comparator has an internal voltage reference V_{REF} connected to the inverting input, while the non-inverting input, available on pin (CIN), can be connected to an external shunt resistor in order to implement the overcurrent protection function. When the comparator triggers, the device is set in shutdown state and both of its outputs are set to low level leading the half-bridge to tri-state. In the common overcurrent protection architectures the comparator output is usually connected to the shutdown input through an RC network, in order to provide a mono-stable circuit, which implements protection time that follows the fault condition. Our smart shutdown architecture allows the output gate driver to be immediately turned off in case of overcurrent, the fault signal has a preferential path which directly switches off the outputs. The time delay between the fault and the output turn-off is no more dependent of RC values of the external network connected to the shutdown pin. At the same time the DMOS connected to the open drain output (pin $\overline{SD}$/OD) is turned on by the internal logic which holds it on until the shutdown voltage is lower than the lowest logic input threshold (V_{il}). Finally, the smart shutdown function provides the possibility to increase the real disable time without increasing the constant time of the external RC network.

Figure 10. Smart shutdown timing waveforms



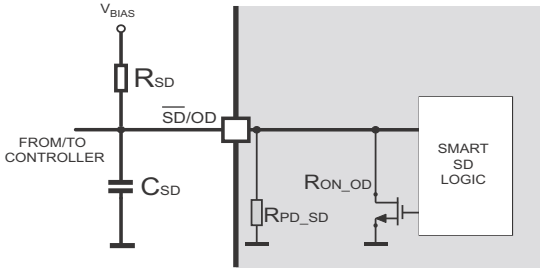
Driver outputs are set in SD state immediately after the comparator triggering even if SD signal has not reached yet the lowest input threshold

An approximation of the disable time is given by:

$$t_1 \cong \tau_1 \cdot ln\left(\frac{V_{off} - V_{on}}{V_{il} - V_{on}}\right)$$

$$t_2 \cong \tau_2 \cdot ln\left(\frac{V_{il} - V_{off}}{V_{ih} - V_{off}}\right)$$

SHUTDOWN CIRCUIT



where:

$$\tau_1 = \left(R_{ON\_OD} // R_{SD}\right) \cdot C_{SD}$$

$$\tau_2 = \left(R_{PD\_SD} // R_{SD}\right) \cdot C_{SD}$$

$$V_{on} = \frac{R_{ON\_OD}}{R_{ON\_OD} + R_{SD}} \cdot V_{BIAS}$$

$$V_{off} = \frac{R_{PD\_SD}}{R_{PD\_SD} + R_{SD}} \cdot \ BIAS$$

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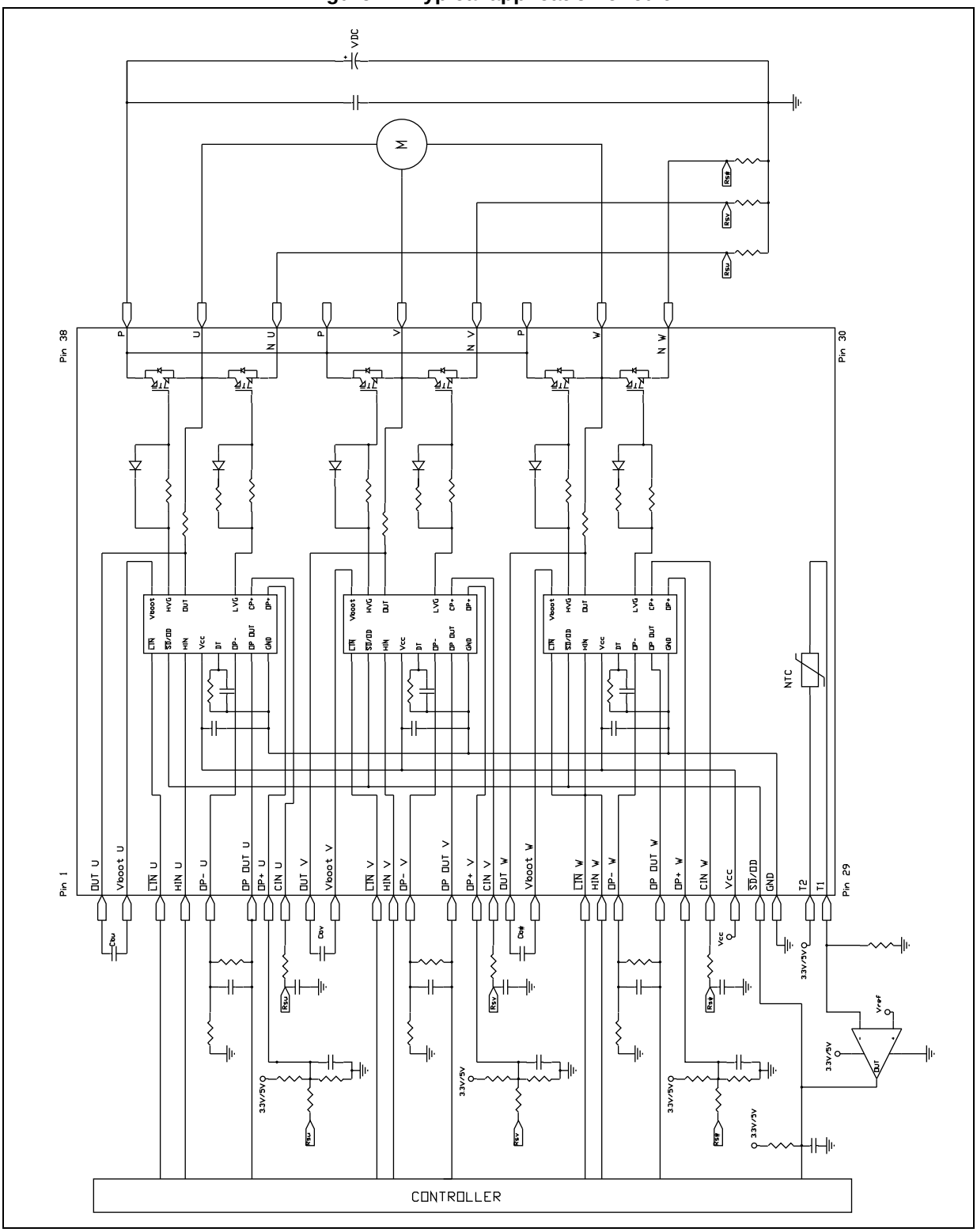
Note: Please refer to Table 12 for internal propagation delay time details.

5 Application information

Figure 11. Typical application circuit



5.1 Recommendations

- Input signal HIN is active high logic. A 85 kΩ (typ.) pull-down resistor is built-in for each high-side input. If an external RC filter is used for noise immunity, pay attention to the variation of the input signal level.
- Input signal $\overline{\text{LIN}}$ is active low logic. A 720 kΩ (typ.) pull-up resistor, connected to an internal 5 V regulator through a diode, is built-in for each low-side input.
- To avoid the input signal oscillation, the wiring of each input should be as short as possible.
- By integrating HVIC application inside the module, direct coupling to MCU terminals without any optocoupler.
- Each capacitor should be very close to IPM pins.
- Low inductance shunt resistors should be used for phase leg current sensing.
- Electrolytic bus capacitors should be mounted on the module bus terminals as closer as possible. Additional high frequency ceramic capacitors, mounted on module pins, improve the performance.
- The $\overline{\text{SD}}$/OD signal should be pulled up to 5 V / 3.3 V with an external resistor (see *Section 4: Smart shutdown function* for detailed information).

Table 15. Recommended operating conditions

Symbol	Parameter	Conditions	Value			Unit
			Min.	Typ.	Max.	
V_{PN}	Supply voltage	Applied among P-Nu, Nv, Nw		300	400	V
V_{CC}	Control supply voltage	Applied between V_{CC} - GND	13.5	15	18	V
V_{BS}	High-side bias voltage	Applied between V_{BOOTi} - OUT_i for i = U, V, W	13		18	V
t_{dead}	Blanking time to prevent arm-short	For each input signal	1.5			µs
f_{PWM}	PWM input signal	-40 °C < T_c < 100 °C -40 °C < T_j < 125 °C			20	kHz
T_C	Case operation temperature				100	°C

Note: For further details refer to AN3338.

6 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK® is an ST trademark.

Please refer to dedicated technical note TN0107 for mounting instructions.

6.1 SDIP-38L package information

Figure 12. SDIP-38L package outline

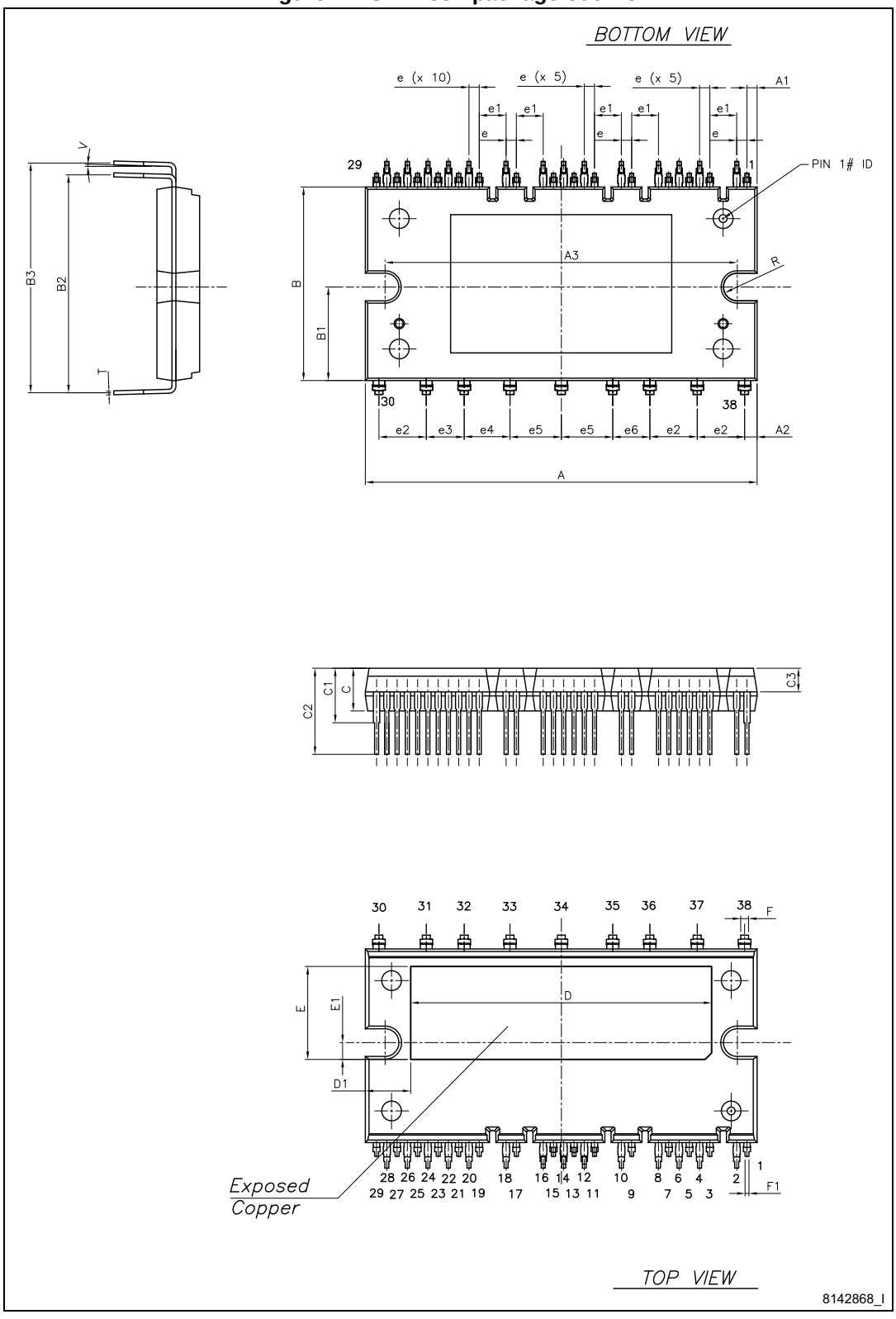


Table 16. SDIP-38L package mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	49.10	49.60	50.10
A1	1.10	1.30	1.50
A2	1.40	1.60	1.80
A3	44.10	44.60	45.10
B	24.00	24.50	25.00
B1	11.25	11.85	12.45
B2	27.10	27.60	28.10
B3	28.60	29.10	29.60
C	5.00	5.40	6.00
C1	6.50	7.00	7.50
C2	10.35	10.85	11.35
C3	2.90	3.00	3.10
e	1.10	1.30	1.50
e1	3.20	3.40	3.60
e2	5.80	6.00	6.20
e3	4.60	4.80	5.00
e4	5.60	5.80	6.00
e5	6.30	6.50	6.70
e6	4.50	4.70	4.90
D		38.10	
D1		5.75	
E		11.80	
E1		2.15	
F	0.85	1.00	1.15
F1	0.35	0.50	0.65
R	1.55	1.75	1.95
T	0.45	0.55	0.65
V	0 °		6 °

7 Revision history

Table 17. Document revision history

Date	Revision	Changes
12-Apr-2016	1	Initial release.