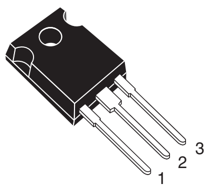
STGW35NC120HD

35 A - 1200 V - very fast IGBT

Features

- Low on-losses
- Low on-voltage drop ($V_{CE(sat)}$)
- High current capability
- High input impedance (voltage driven)
- Low gate charge
- Ideal for soft switching application



TO-247

Application

- Induction heating

Description

This IGBT utilizes the advanced PowerMESH™ process resulting in an excellent trade-off between switching performance and low on-state behavior.

Figure 1. Internal schematic diagram

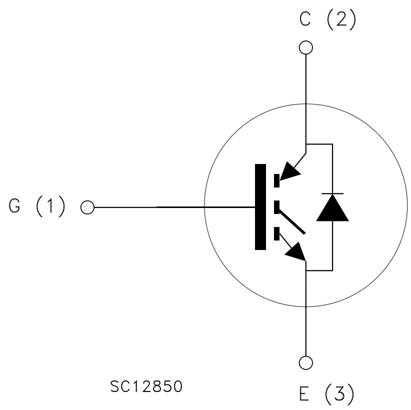


Table 1. Device summary

Order code	Marking	Package	Packaging
STGW35NC120HD	GW35NC120HD	TO-247	Tube

Contents

1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{CES}	Collector-emitter voltage (V_{GE} = 0)	1200	V
I_C (1)	Collector current (continuous) at 25 °C	58	A
I_C (1)	Collector current (continuous) at 100 °C	34	A
I_{CL} (2)	Turn-off latching current	135	A
I_{CP} (3)	Pulsed collector current	135	A
V_{GE}	Gate-emitter voltage	±25	V
P_{TOT}	Total dissipation at T_C = 25 °C	220	W
I_F	Diode RMS forward current at T_C = 25 °C	30	A
I_{FSM}	Surge non repetitive forward current t_p = 10 ms sinusoidal	100	A
T_j	Operating junction temperature	–55 to 150	°C
T_{stg}	Storage temperature		

1. Calculated according to the iterative formula:

$$I_C(T_C) = \frac{T_{JMAX} - T_C}{R_{THJ-C} \times V_{CESAT(MAX)}(T_C, I_C)}$$

2. Vclamp = 80% of V_{CES}, T_j =150 °C, R_G=10 Ω, V_{GE}=15 V
3. Pulse width limited by max. junction temperature allowed

Table 3. Thermal resistance

Symbol	Parameter	Min.	Typ.	Max.	Unit
$R_{thj-case}$	Thermal resistance junction-case IGBT			0.562	°C/W
	Thermal resistance junction-case diode			1.5	°C/W
$R_{thj-amb}$	Thermal resistance junction-ambient			50	°C/W

2 Electrical characteristics

(T_{CASE}=25°C unless otherwise specified)

Table 4. Static

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{BR(CES)}$	Collector-emitter breakdown voltage (V_{GE} = 0)	I_C = 1 mA	1200			V
$V_{CE(SAT)}$	Collector-emitter saturation voltage	V_{GE}= 15 V, I_C= 20 A, V_{GE}= 15 V, I_C= 20 A, T_C=125 °C		2.2 2.0	2.75	V V
$V_{GE(th)}$	Gate threshold voltage	V_{CE}= V_{GE}, I_C= 250µA	3.75		5.75	V
I_{CES}	Collector-emitter leakage current (V_{GE} = 0)	V_{CE} =1200 V V_{CE} =1200 V, T_C=125 °C			500 10	µA mA
I_{GES}	Gate-emitter leakage current (V_{CE} = 0)	V_{GE} =± 20 V			± 100	nA
g_{fs} (1)	Forward transconductance	V_{CE} = 25 V, I_C= 20 A		14		S

1. Pulse duration = 300 µs, duty cycle 1.5%

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{ies} C_{oes} C_{res}	Input capacitance Output capacitance Reverse transfer capacitance	V_{CE} = 25 V, f = 1 MHz, V_{GE}=0		2510 175 30		pF pF pF
Q_g Q_{ge} Q_{gc}	Total gate charge Gate-emitter charge Gate-collector charge	V_{CE} = 960 V, I_C= 20 A,V_{GE}=15 V		110 16 49	120	nC nC nC

Table 6. Switching on/off (inductive load)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$ t_r $(di/dt)_{on}$	Turn-on delay time Current rise time Turn-on current slope	V_{CC} = 960 V, I_C = 20 A R_G= 10 Ω, V_{GE}= 15 V, *(see Figure 17)*		29 11 1820		ns ns A/µs
$t_{d(on)}$ t_r $(di/dt)_{on}$	Turn-on delay time Current rise time Turn-on current slope	V_{CC} = 960 V, I_C = 20 A R_G= 10 Ω, V_{GE}= 15 V, T_C=125 °C *(see Figure 17)*		27 14 1580		ns ns A/µs
$t_r(V_{off})$ $t_d(_{off})$ t_f	Off voltage rise time Turn-off delay time Current fall time	V_{CC} = 960 V, I_C = 20 A R_G= 10 Ω, V_{GE}= 15 V, *(see Figure 17)*		90 275 312		ns ns ns
$t_r(V_{off})$ $t_d(_{off})$ t_f	Off voltage rise time Turn-off delay time Current fall time	V_{CC} = 960 V, I_C = 20 A R_G= 10 Ω, V_{GE}= 15 V, T_C=125 °C *(see Figure 17)*		150 336 592		ns ns ns

Table 7. Switching energy (inductive load)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
Eon (1) E_{off} (2) E_{ts}	Turn-on switching losses Turn-off switching losses Total switching losses	V_{CC} = 960 V, I_C = 20 A R_G= 10 Ω, V_{GE}= 15 V, *(see Figure 17)*		1660 4438 6098		µJ µJ µJ
Eon (1) E_{off} (2) E_{ts}	Turn-on switching losses Turn-off switching losses Total switching losses	V_{CC} = 960 V, I_C = 20 A R_G= 10 Ω, V_{GE}= 15 V, T_C=125 °C *(see Figure 17)*		3015 6900 9915		µJ µJ µJ

1. Eon is the turn-on losses when a typical diode is used in the test circuit in figure 2. If the IGBT is offered in a package with a co-pack diode, the co-pack diode is used as external diode. IGBTs & Diode are at the same temperature (25°C and 125°C)
2. Turn-off losses include also the tail of the collector current

Table 8. Collector-emitter diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_F	Forward on-voltage	I_F = 20 A I_F = 20 A, T_C = 125 °C		1.9 1.7	2.5	V V
t_{rr} Q_{rr} I_{rrm}	Reverse recovery time Reverse recovery charge Reverse recovery current	I_F = 20 A, V_R = 27 V, T_C=125 °C, di/dt = 100 A/µs *(see Figure 20)*		152 722 9		ns nC A

2.1 Electrical characteristics (curves)

Figure 2. Output characteristics

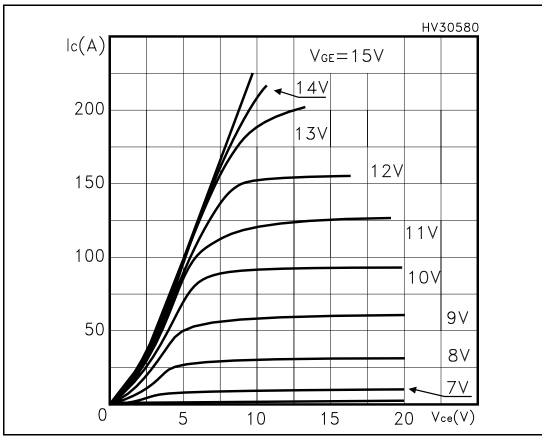


Figure 3. Transfer characteristics

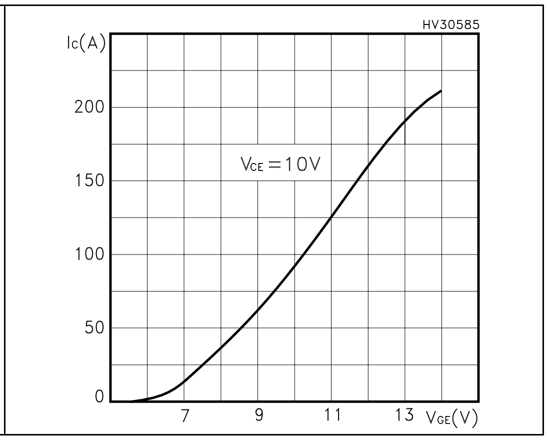


Figure 4. Transconductance

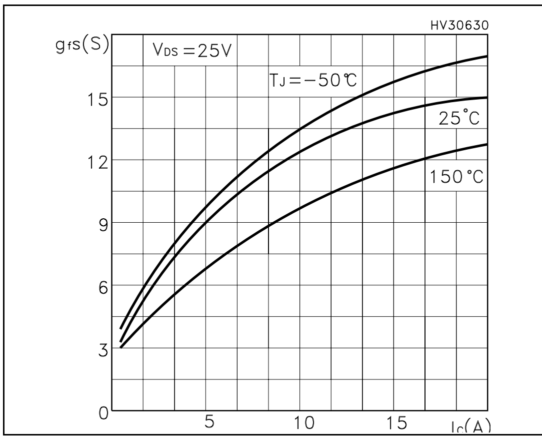


Figure 5. Collector-emitter on voltage vs. temperature

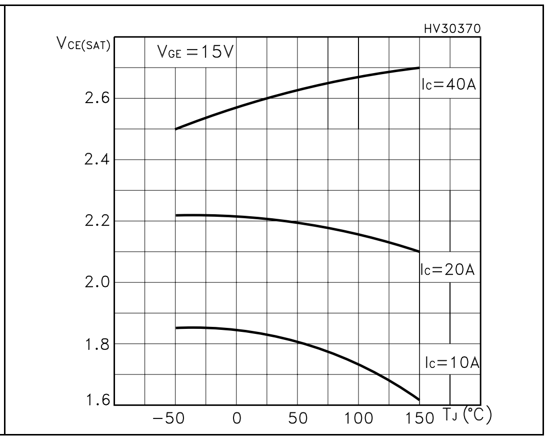


Figure 6. Gate charge vs. gate-source voltage

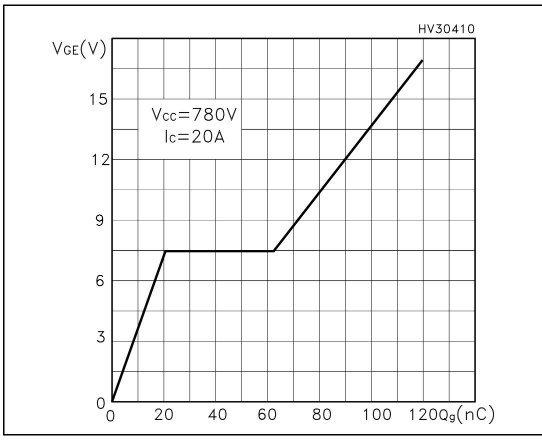


Figure 7. Capacitance variations

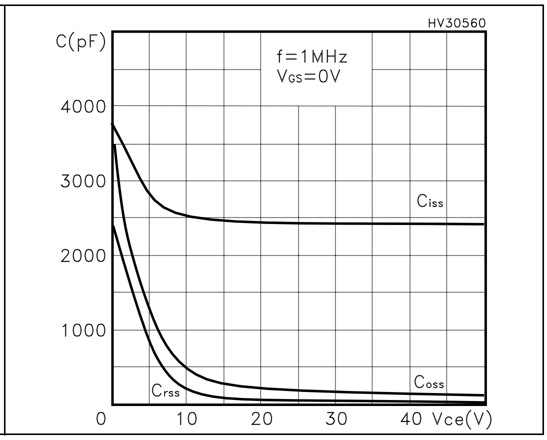


Figure 8. Normalized gate threshold voltage vs. temperature

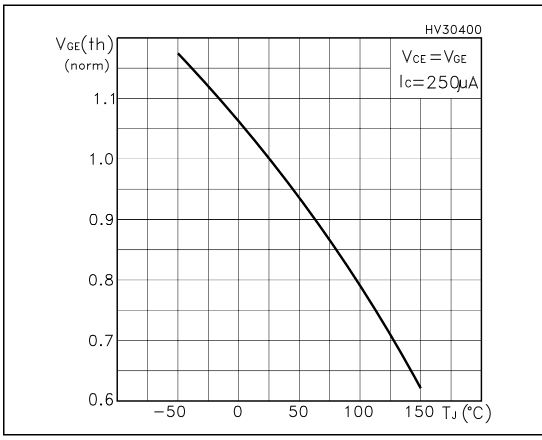


Figure 9. Collector-emitter on voltage vs. collector current

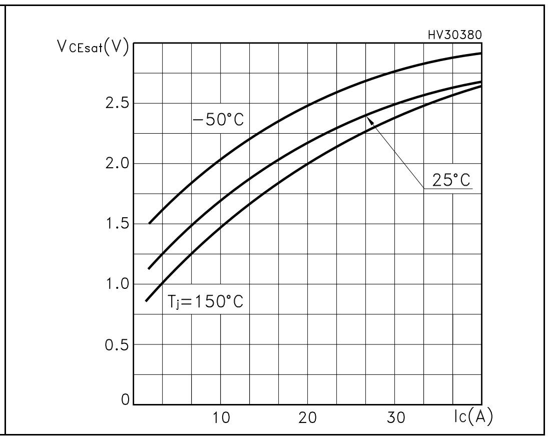


Figure 10. Normalized breakdown voltage vs. temperature

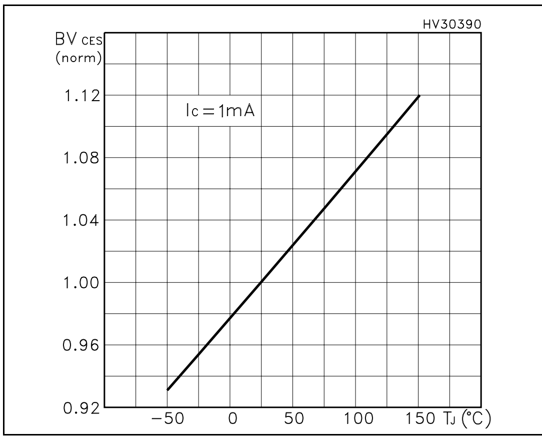


Figure 11. Switching losses vs. temperature

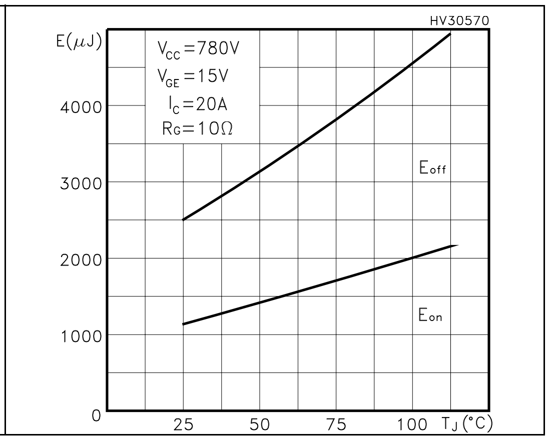


Figure 12. Switching losses vs. gate resistance

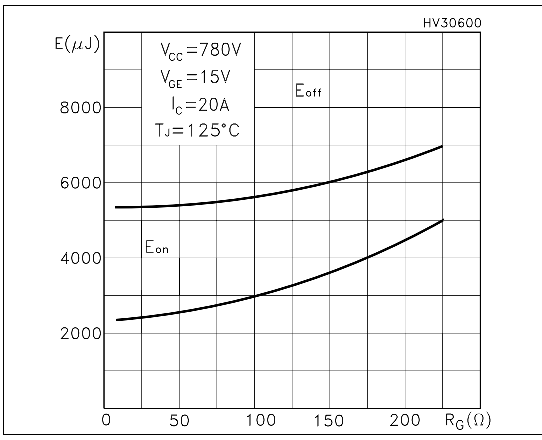


Figure 13. Switching losses vs. collector current

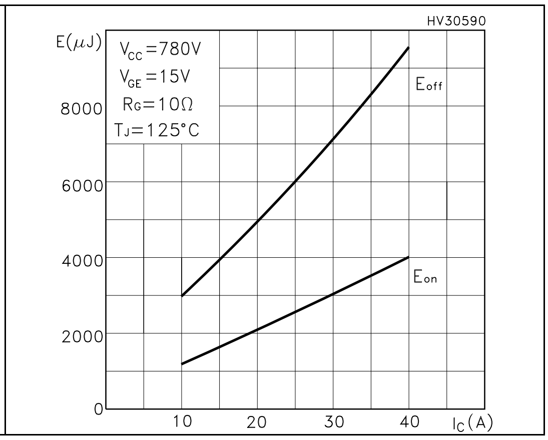


Figure 14. Thermal Impedance

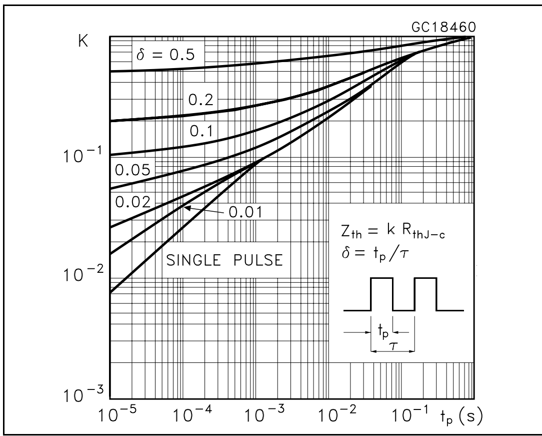


Figure 15. Turn-off SOA

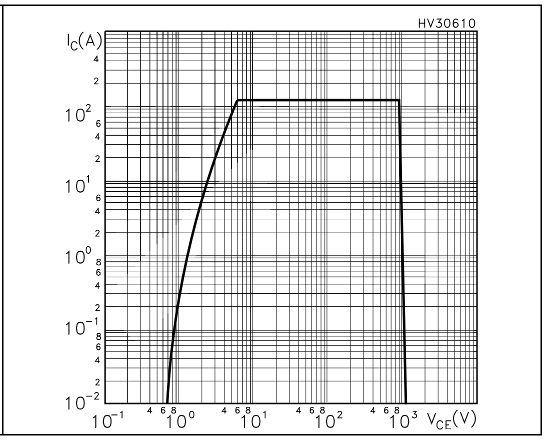
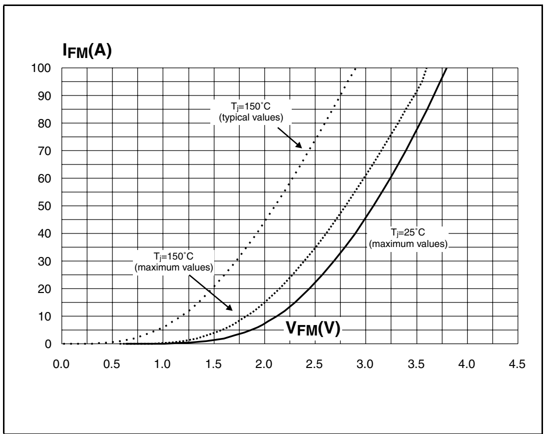


Figure 16. Forward voltage drop vs. forward current



3 Test circuit

Figure 17. Test circuit for inductive load switching

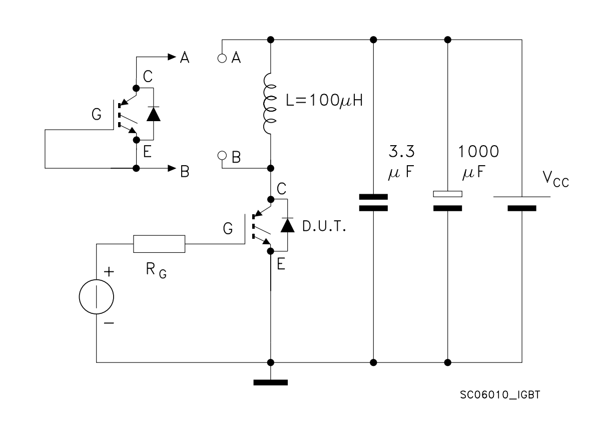


Figure 18. Gate charge test circuit

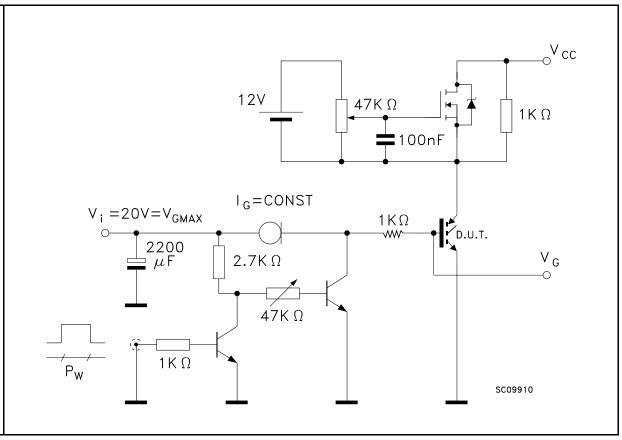


Figure 19. Switching waveform

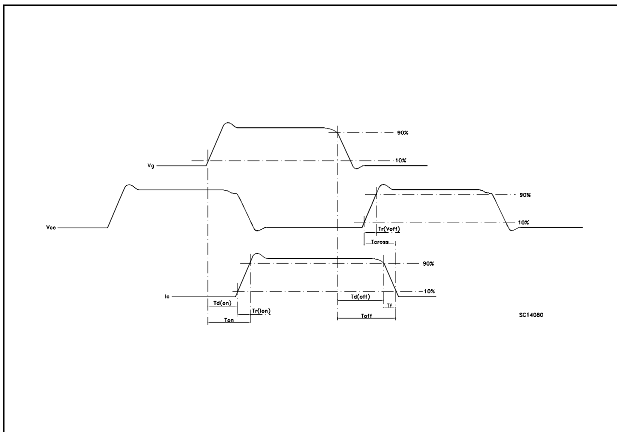
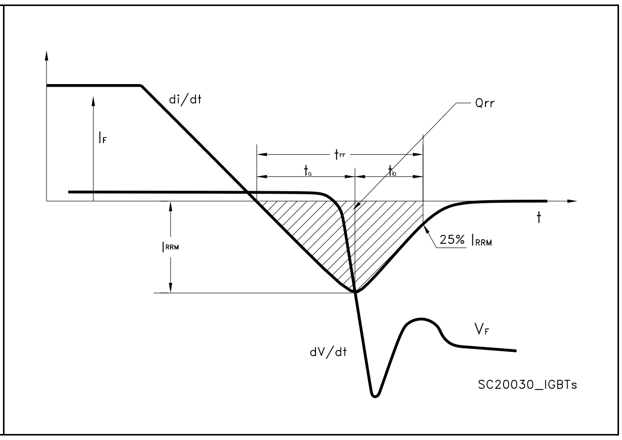


Figure 20. Diode recovery time waveform

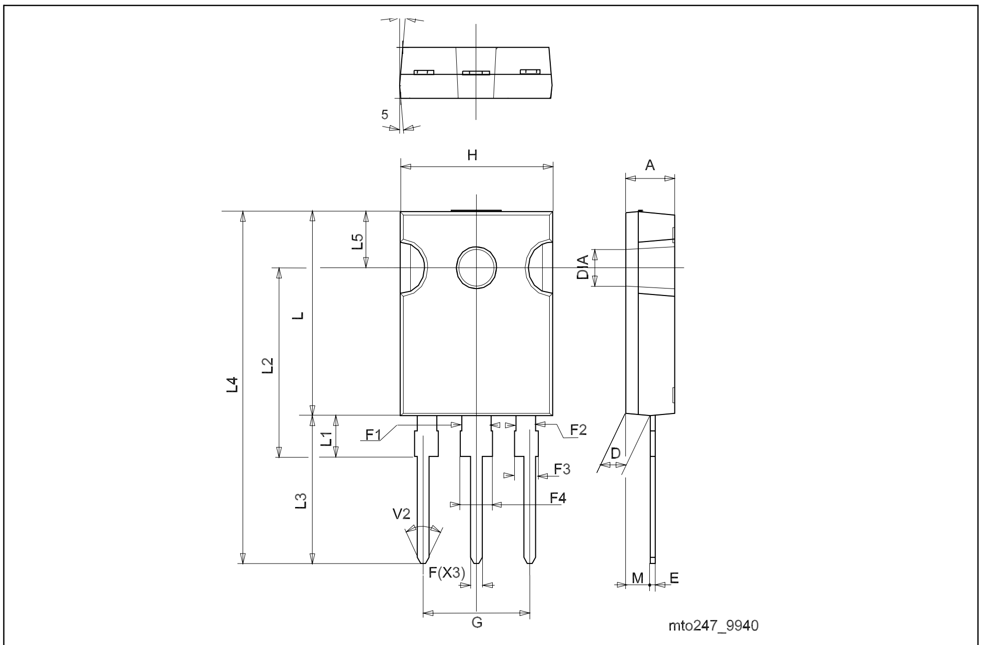


4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect. The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: *www.st.com*

TO-247 MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A	4.90		5.16	0.193		0.203
D	2.35		2.45	0.093		0.096
E	0.6		0.76	0.024		0.030
F	1.2		1.33	0.047		0.052
F1		3			0.118	
F2		2			0.078	
F3	1.9		2.13	0.075		0.084
F4	3.04		3.2	0.120		0.126
G		10.90			0.429	
H	15.77		16.03	0.621		0.631
L	20.83		21.09	0.820		0.830
L1	3.93		4.45	0.155		0.175
L2	18.72		19.18	0.737		0.755
L3	20.04		20.31	0.789		0.800
L4	40.88		41.40	1.609		1.630
L5	6.04		6.30	0.238		0.248
M	2		3		0.078	0.118
V		5°			5°	
V2		60°			60°	
Diam	3.56		3.66	0.140		0.144



5 Revision history

Table 9. Document revision history

Date	Revision	Changes
25-Jan-2008	1	First issue.