

Features

- High frequency operation
- Lower C_{RES} / C_{IES} ratio (no cross-conduction susceptibility)

Applications

- High frequency motor controls, inverters, UPS
- HF, SMPS and PFC in both hard switch and resonant topologies

Description

This IGBT utilizes the advanced PowerMESH™ process resulting in an excellent trade-off between switching performance and low on-state behavior.

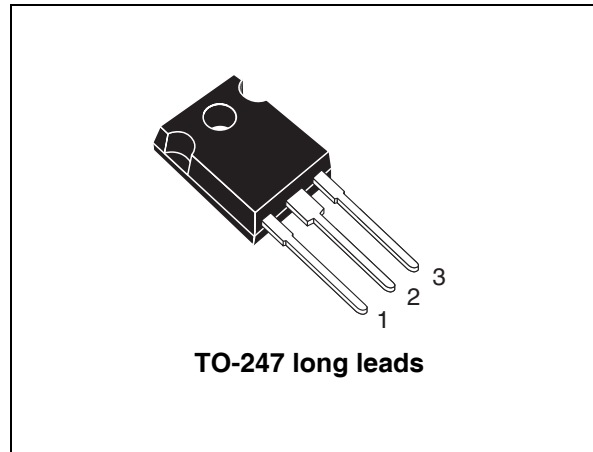


Figure 1. Internal schematic diagram

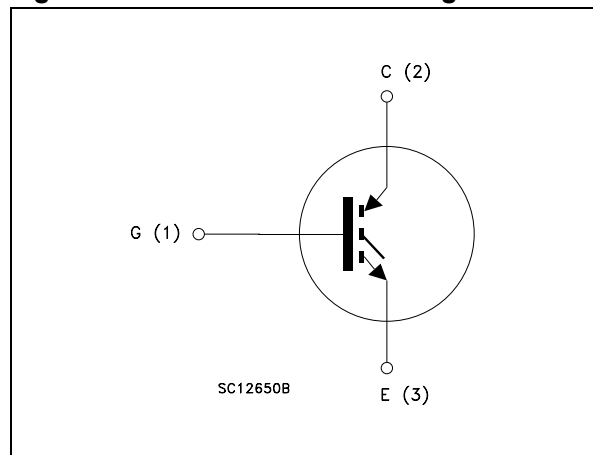


Table 1. Device summary

Order code	Marking	Package	Packaging
STGW35NC60W	GW35NC60W	TO-247 long leads	Tube

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1 Electrical ratings

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Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{CES}	Collector-emitter voltage ($V_{GE} = 0$)	600	V
$I_C^{(1)}$	Collector current (continuous) at 25 °C	70	A
$I_C^{(1)}$	Collector current (continuous) at 100 °C	40	A
$I_{CP}^{(2)}$	Collector current (pulsed)	150	A
$I_{CL}^{(3)}$	Turn-off latching current	150	A
V_{GE}	Gate-emitter voltage	± 20	V
P_{TOT}	Total dissipation at $T_C = 25$ °C	260	W
T_{stg}	Storage temperature	- 55 to 150	°C
T_j	Operating junction temperature		

1. Calculated according to the iterative formula:

$$I_C(T_C) = \frac{T_{j(max)} - T_C}{R_{thj-c} \times V_{CE(sat)(max)}(T_{j(max)}, I_C(T_C))}$$

2. Pulse width limited by max junction temperature
 3. $V_{CLAMP} = 80\% (V_{CES})$, $V_{GE} = 15$ V, $R_G = 10$ Ω, $T_J = 150$ °C

Table 3. Thermal resistance

Symbol	Parameter	Value	Unit
$R_{thj-case}$	Thermal resistance junction-case IGBT max.	0.48	°C/W
$R_{thj-amb}$	Thermal resistance junction-ambient max.	50	°C/W

2 Electrical characteristics

($T_{CASE} = 25^{\circ}C$ unless otherwise specified)

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Table 4. Static electrical characteristics

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)CES}$	Collector-emitter breakdown voltage ($V_{GE} = 0$)	$I_C = 1 \text{ mA}$	600			V
$V_{CE(sat)}$	Collector-emitter saturation voltage	$V_{GE} = 15 \text{ V}, I_C = 20 \text{ A}$ $V_{GE} = 15 \text{ V}, I_C = 20 \text{ A}, T_C = 125^{\circ}C$		2.2 1.8	2.6	V V
$V_{GE(th)}$	Gate threshold voltage	$V_{CE} = V_{GE}, I_C = 250 \mu\text{A}$	3.75		5.75	V
I_{CES}	Collector cut-off current ($V_{GE} = 0$)	$V_{CE} = 600 \text{ V}$ $V_{CE} = 600 \text{ V}, T_C = 125^{\circ}C$			250 1	μA mA
I_{GES}	Gate-emitter leakage current ($V_{CE} = 0$)	$V_{GE} = \pm 20 \text{ V}$			± 100	nA
g_{fs}	Forward transconductance	$V_{CE} = 15 \text{ V}, I_C = 20 \text{ A}$		15		S

Table 5. Dynamic electrical characteristics

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{ies}	Input capacitance	$V_{CE} = 25 \text{ V}, f = 1 \text{ MHz},$ $V_{GE} = 0$		2080		pF
C_{oes}	Output capacitance			175		pF
C_{res}	Reverse transfer capacitance			52		pF
Q_g	Total gate charge	$V_{CE} = 390 \text{ V}, I_C = 20 \text{ A},$ $V_{GE} = 15 \text{ V},$ <i>(see Figure 17)</i>		102	140	nC
Q_{ge}	Gate-emitter charge			17.5		nC
Q_{gc}	Gate-collector charge			47		nC

Table 6. Switching on/off (inductive load)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{CC} = 390\text{ V}$, $I_C = 20\text{ A}$		29.5		ns
t_r	Current rise time	$R_G = 10\ \Omega$, $V_{GE} = 15\text{ V}$,		12		ns
$(di/dt)_{on}$	Turn-on current slope	(see Figure 16)		1640		A/ μ s
$t_{d(on)}$	Turn-on delay time	$V_{CC} = 390\text{ V}$, $I_C = 20\text{ A}$		29		ns
t_r	Current rise time	$R_G = 10\ \Omega$, $V_{GE} = 15\text{ V}$,		13.5		ns
$(di/dt)_{on}$	Turn-on current slope	$T_C = 125\text{ }^\circ\text{C}$ (see Figure 16)		1600		A/ μ s
$t_r(V_{off})$	Off voltage rise time	$V_{CC} = 390\text{ V}$, $I_C = 20\text{ A}$,		19.5		ns
$t_{d(off)}$	Turn-off delay time	$R_{GE} = 10\ \Omega$, $V_{GE} = 15\text{ V}$		118		ns
t_f	Current fall time	(see Figure 16)		27		ns
$t_r(V_{off})$	Off voltage rise time	$V_{CC} = 390\text{ V}$, $I_C = 20\text{ A}$,		46		ns
$t_{d(off)}$	Turn-off delay time	$R_{GE} = 10\ \Omega$, $V_{GE} = 15\text{ V}$,		151		ns
t_f	Current fall time	$T_C = 125\text{ }^\circ\text{C}$ (see Figure 16)		38		ns

Table 7. Switching energy (inductive load)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$E_{on}^{(1)}$	Turn-on switching losses	$V_{CC} = 390\text{ V}$, $I_C = 20\text{ A}$		305		μ J
E_{off}	Turn-off switching losses	$R_G = 10\ \Omega$, $V_{GE} = 15\text{ V}$,		181		μ J
E_{ts}	Total switching losses	(see Figure 18)		486		μ J
$E_{on}^{(1)}$	Turn-on switching losses	$V_{CC} = 390\text{ V}$, $I_C = 20\text{ A}$		455		μ J
E_{off}	Turn-off switching losses	$R_G = 10\ \Omega$, $V_{GE} = 15\text{ V}$,		355		μ J
E_{ts}	Total switching losses	$T_C = 125\text{ }^\circ\text{C}$ (see Figure 18)		810		μ J

1. E_{on} is the turn-on losses when a typical diode is used in the test circuit in Figure 18. If the IGBT is offered in a package with a co-pak diode, the co-pak diode is used as external diode. IGBTs & Diode are at the same temperature (25°C and 125°C). E_{on} include diode recovery energy.

2.1 Electrical characteristics (curves)

Figure 2. Output characteristics

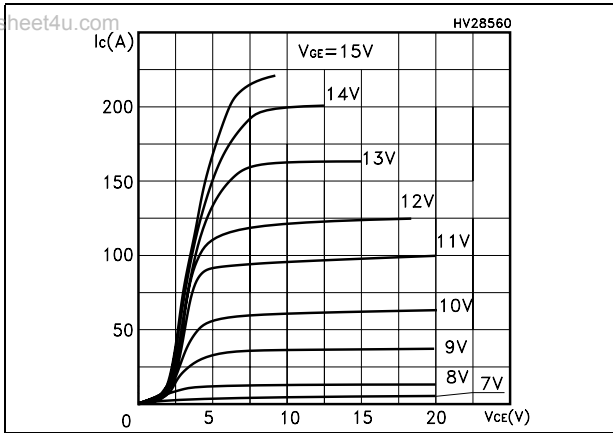


Figure 3. Transfer characteristics

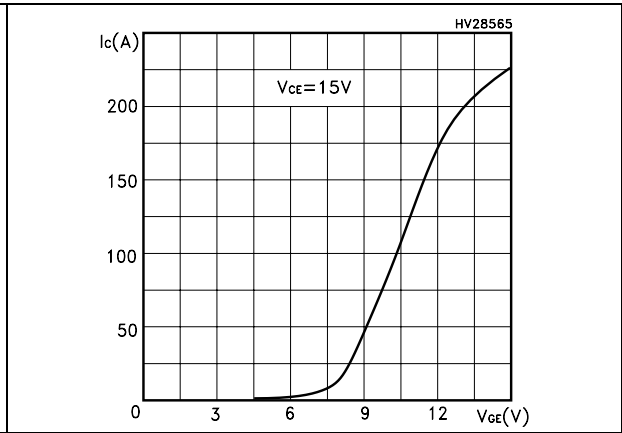


Figure 4. Transconductance

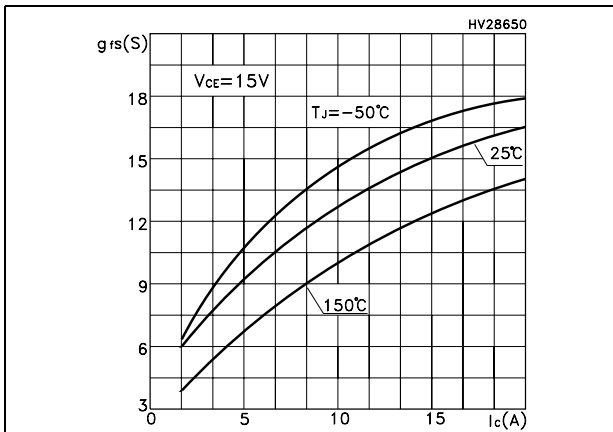


Figure 5. Collector-emitter on voltage vs temperature

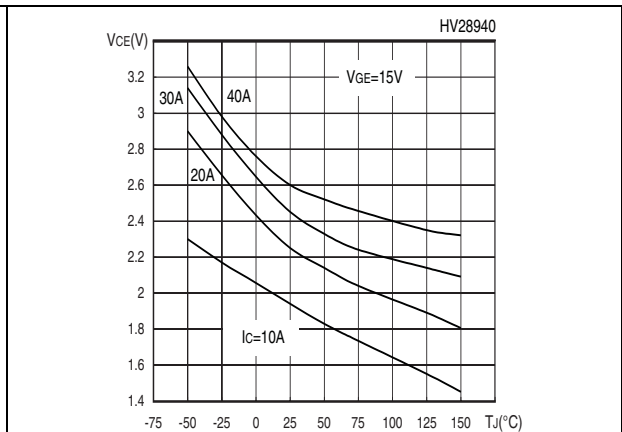


Figure 6. Gate charge vs gate-source voltage Figure 7. Capacitance variations

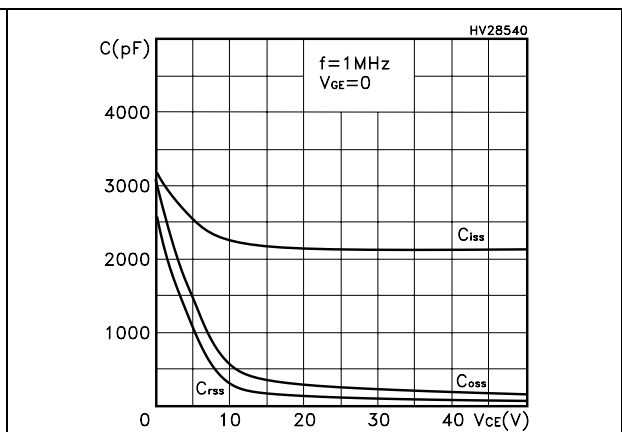
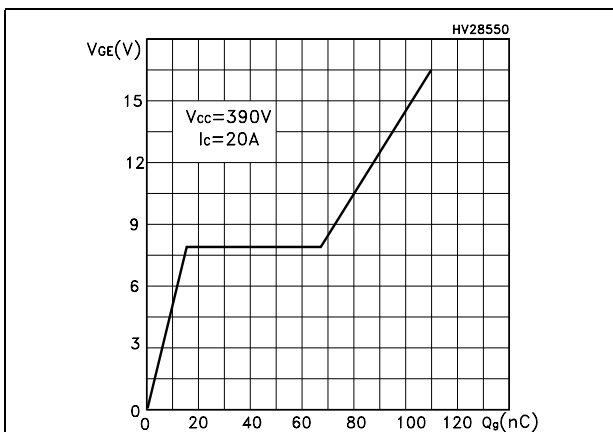


Figure 8. Normalized gate threshold voltage vs temperature

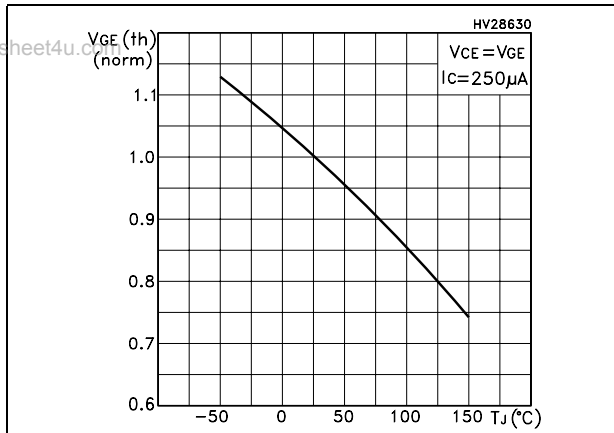


Figure 9. Collector-emitter on voltage vs collector current

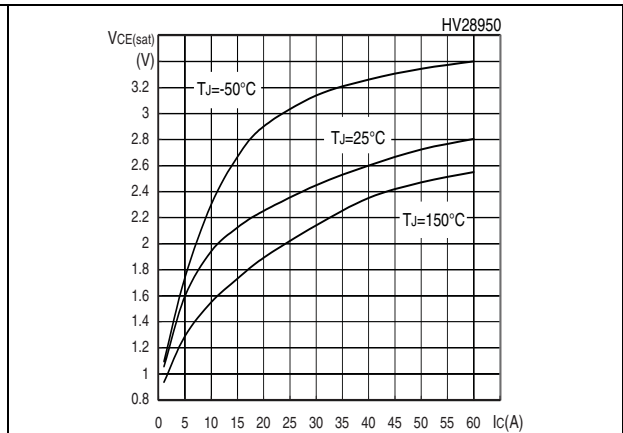


Figure 10. Normalized breakdown voltage vs temperature

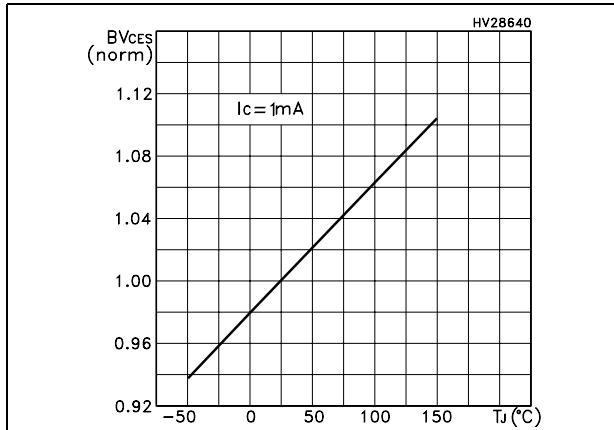


Figure 11. Switching losses vs temperature

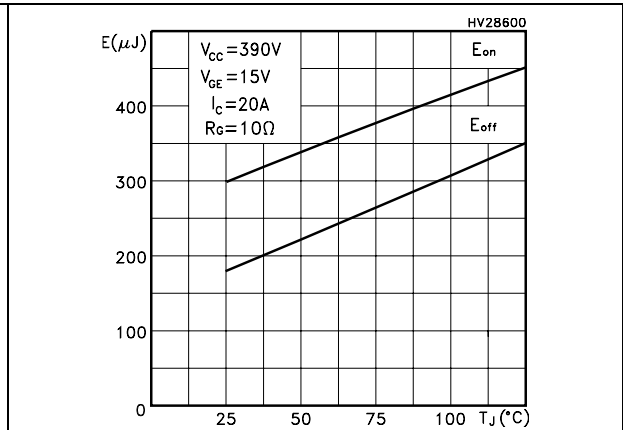


Figure 12. Switching losses vs gate resistance

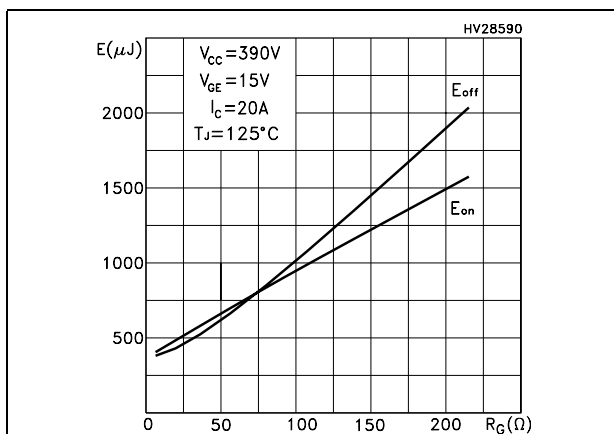


Figure 13. Switching losses vs collector current

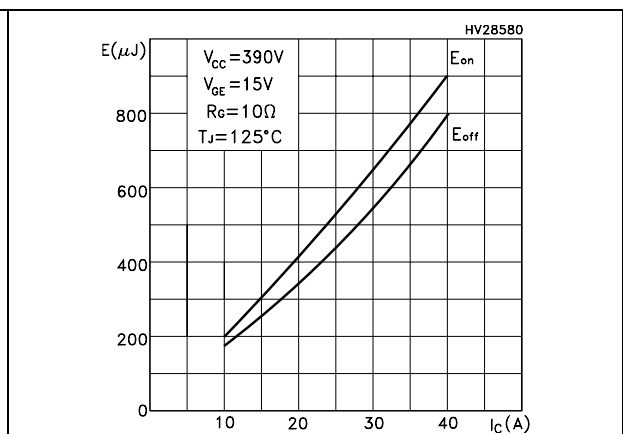
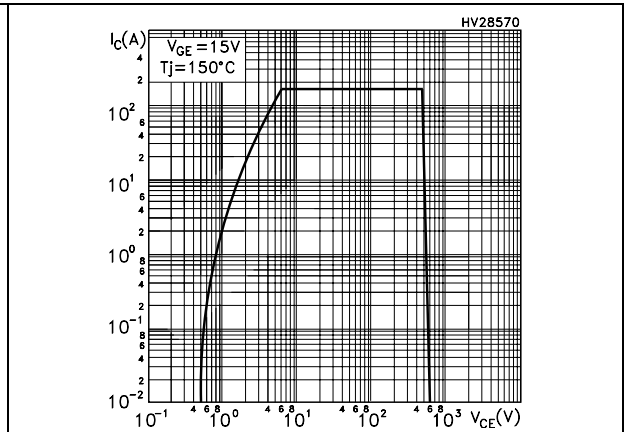
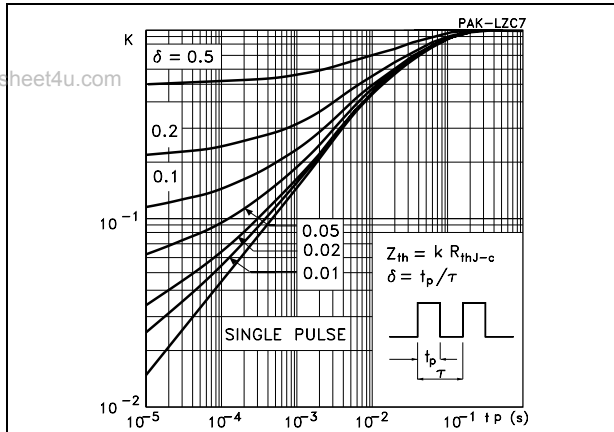


Figure 14. Thermal impedance

Figure 15. Turn-off SOA



3 Test circuit

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Figure 16. Test circuit for inductive load switching

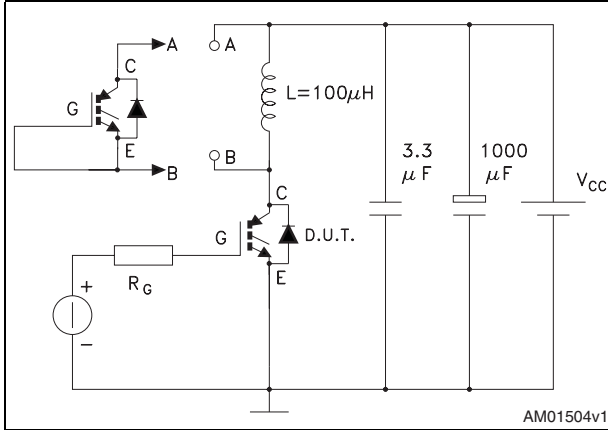


Figure 17. Gate charge test circuit

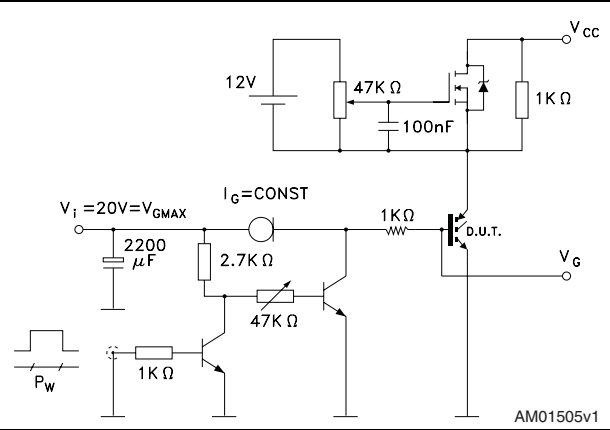
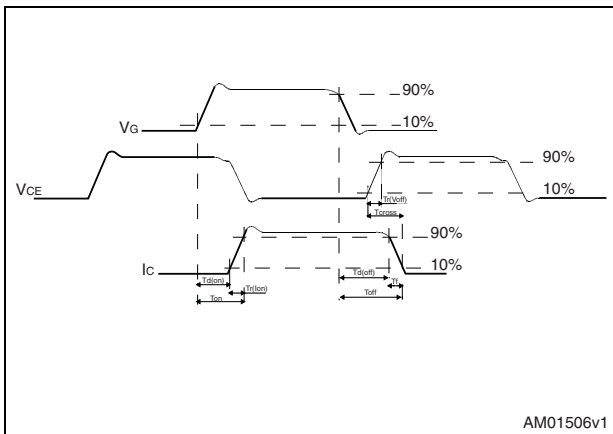


Figure 18. Switching waveform



4 Package mechanical data

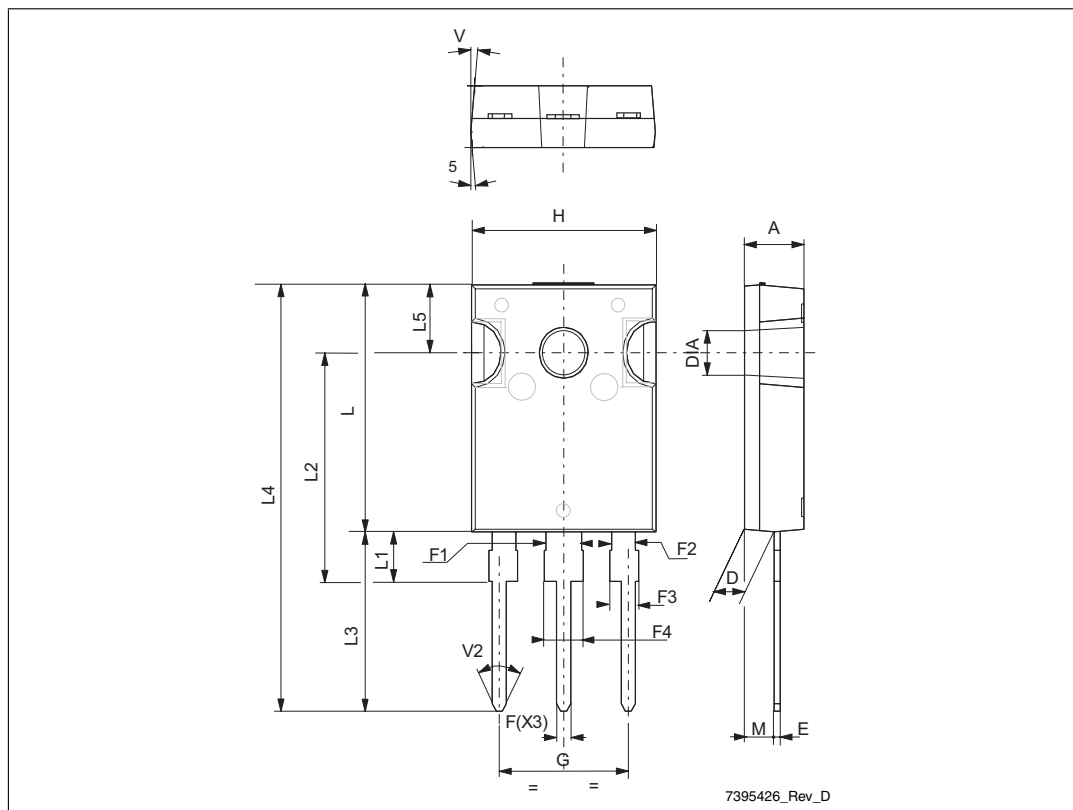
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In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect. The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com

TO-247 long leads mechanical data

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Dim.	mm		
	Min.	Typ.	Max.
A	4.85		5.16
D	2.2		2.6
E	0.4		0.8
F	1		1.4
F1		3	
F2		2	
F3	1.9		2.4
F4	3		3.4
G		10.9	
H	15.45		16.03
L	19.85		21.09
L1	3.7		4.3
L2	18.3		19.13
L3	14.2		20.3
L4	34.05		41.38
L5	5.35		6.3
M	2		3
V		5°	
V2		60°	
DIAM	3.55		3.65



5 Revision history

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Table 8. Document revision history

Date	Revision	Changes
17-Nov-2008	1	Initial release.

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