

## N-channel 100 V, 0.0034 $\Omega$ typ., 110 A, STripFET™ F7 Power MOSFET in a H<sup>2</sup>PAK-2 package

Datasheet – production data

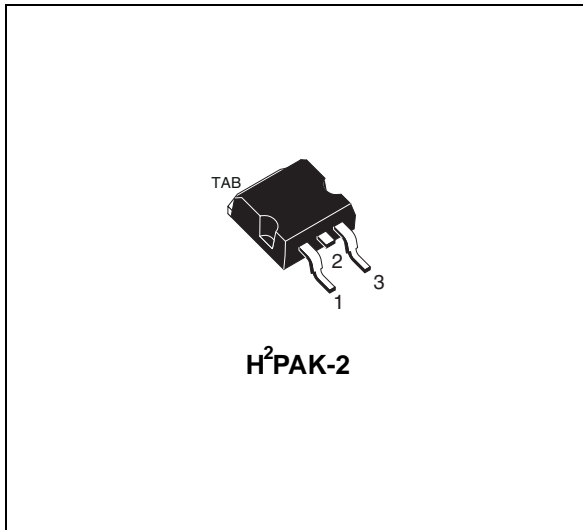
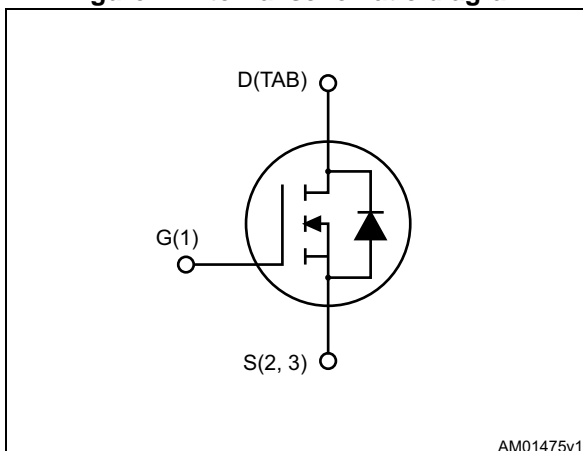


Figure 1. Internal schematic diagram



### Features

Order code	V <sub>DS</sub>	R <sub>DS(on)max</sub>	I <sub>D</sub>	P <sub>TOT</sub>
STH150N10F7-2	100 V	0.0039 $\Omega$	110 A	250 W

- Among the lowest R<sub>DS(on)</sub> on the market
- Excellent figure of merit (FoM)
- Low C<sub>rss</sub>/C<sub>iss</sub> ratio for EMI immunity
- High avalanche ruggedness

### Applications

- Switching applications

### Description

This N-channel Power MOSFET utilizes STripFET™ F7 technology with an enhanced trench gate structure that results in very low on-state resistance, while also reducing internal capacitance and gate charge for faster and more efficient switching.

Table 1. Device summary

Order code	Marking	Package	Packaging
STH150N10F7-2	150N10F7	H <sup>2</sup> PAK-2	Tape and reel

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# 1 Electrical ratings

**Table 2. Absolute maximum ratings**

Symbol	Parameter	Value	Unit
$V_{DS}$	Drain-source voltage	100	V
$V_{GS}$	Gate- source voltage	$\pm 20$	V
$I_D$	Drain current (continuous) at $T_C = 25\text{ }^\circ\text{C}$	110	A
$I_D$	Drain current (continuous) at $T_C = 100\text{ }^\circ\text{C}$	110	A
$I_{DM}^{(1)}$	Drain current (pulsed) $T_C = 25\text{ }^\circ\text{C}$	440	A
$P_{TOT}$	Total dissipation at $T_C = 25\text{ }^\circ\text{C}$	250	W
$E_{AS}^{(2)}$	Single pulse avalanche energy	495	mJ
$T_J$	Operating junction temperature range	-55 to 175	$^\circ\text{C}$
$T_{stg}$	Storage temperature range		$^\circ\text{C}$

1. Pulse width is limited by safe operating area

2. Starting  $T_j = 25\text{ }^\circ\text{C}$ ,  $I_D = 30\text{ A}$ ,  $V_{DD} = 50\text{ V}$

**Table 3. Thermal data**

Symbol	Parameter	Value	Unit
$R_{thj-case}$	Thermal resistance junction-case max	0.6	$^\circ\text{C/W}$
$R_{thj-pcb}^{(1)}$	Thermal resistance junction-pcb max	35	$^\circ\text{C/W}$

1. When mounted on 1 inch<sup>2</sup> FR-4 board, 2 oz Cu

## 2 Electrical characteristics

( $T_C = 25\text{ °C}$  unless otherwise specified)

**Table 4. On /off states**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$V_{GS} = 0\text{ V}$ , $I_D = 250\text{ }\mu\text{A}$	100			V
$I_{DSS}$	Zero gate voltage drain current	$V_{GS} = 0\text{ V}$ , $V_{DS} = 100\text{ V}$			1	$\mu\text{A}$
		$V_{GS} = 0\text{ V}$ , $V_{DS} = 100\text{ V}$ , $T_C = 125\text{ °C}$ (1)			100	$\mu\text{A}$
$I_{GSS}$	Gate-body leakage current	$V_{DS} = 0\text{ V}$ , $V_{GS} = +20\text{ V}$			100	nA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}$ , $I_D = 250\text{ }\mu\text{A}$	2.5		4.5	V
$R_{DS(on)}$	Static drain-source on-resistance	$V_{GS} = 10\text{ V}$ , $I_D = 55\text{ A}$		0.0034	0.0039	$\Omega$

1. Defined by design, not subject to production test.

**Table 5. Dynamic**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$C_{iss}$	Input capacitance	$V_{DS} = 50\text{ V}$ , $f = 1\text{ MHz}$ , $V_{GS} = 0\text{ V}$	-	8115	-	pF
$C_{oss}$	Output capacitance		-	1510	-	pF
$C_{riss}$	Reverse transfer capacitance		-	67	-	pF
$Q_g$	Total gate charge	$V_{DD} = 50\text{ V}$ , $I_D = 110\text{ A}$ , $V_{GS} = 10\text{ V}$ (see <a href="#">Figure 14</a> )	-	117	-	nC
$Q_{gs}$	Gate-source charge		-	47	-	nC
$Q_{gd}$	Gate-drain charge		-	26	-	nC

**Table 6. Switching times**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 50\text{ V}$ , $I_D = 55\text{ A}$ , $R_G = 4.7\text{ }\Omega$ , $V_{GS} = 10\text{ V}$ (see <a href="#">Figure 13</a> )	-	33	-	ns
$t_r$	Rise time		-	57	-	ns
$t_{d(off)}$	Turn-off delay time		-	72	-	ns
$t_f$	Fall time		-	33	-	ns

Table 7. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$I_{SD}$	Source-drain current		-		110	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)		-		440	A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD} = 110 \text{ A}$ , $V_{GS} = 0$	-		1.2	V
$t_{rr}$	Reverse recovery time	$I_{SD} = 110 \text{ A}$ , $di/dt = 100 \text{ A}/\mu\text{s}$ $V_{DD} = 80 \text{ V}$ , $T_J = 150 \text{ }^\circ\text{C}$ (see <a href="#">Figure 15</a> )	-	70		ns
$Q_{rr}$	Reverse recovery charge		-	165		nC
$I_{RRM}$	Reverse recovery current		-	4.7		A

1. Pulse width limited by safe operating area
2. Pulsed: pulse duration = 300  $\mu\text{s}$ , duty cycle 1.5%.

## 2.1 Electrical characteristics (curves)

Figure 2. Safe operating area

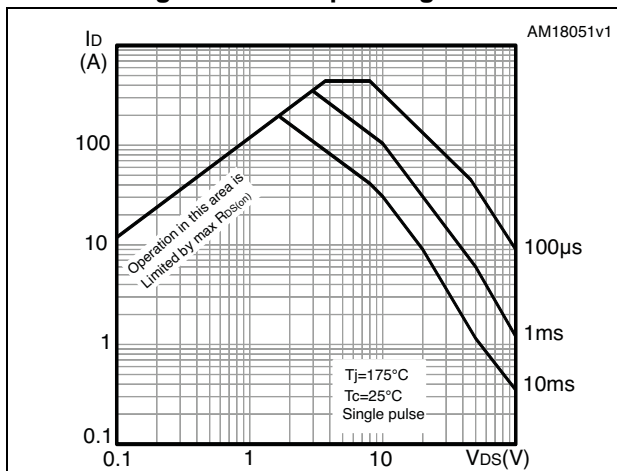


Figure 3. Thermal impedance

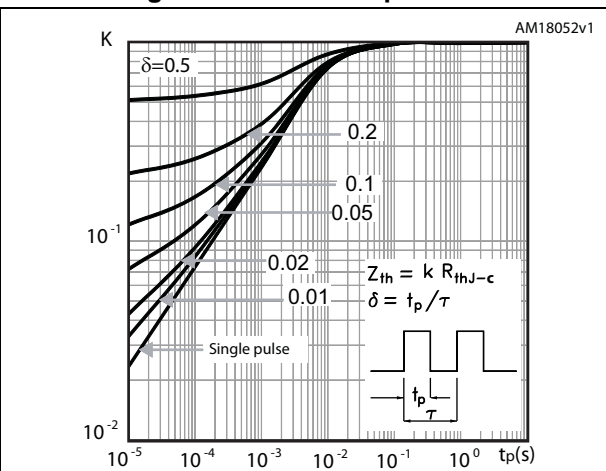


Figure 4. Output characteristics

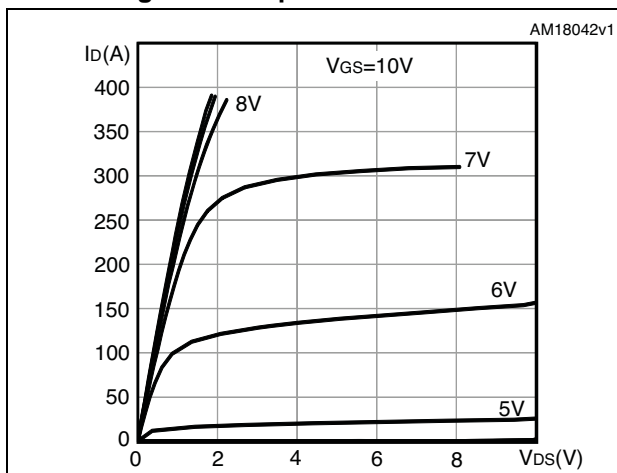


Figure 5. Transfer characteristics

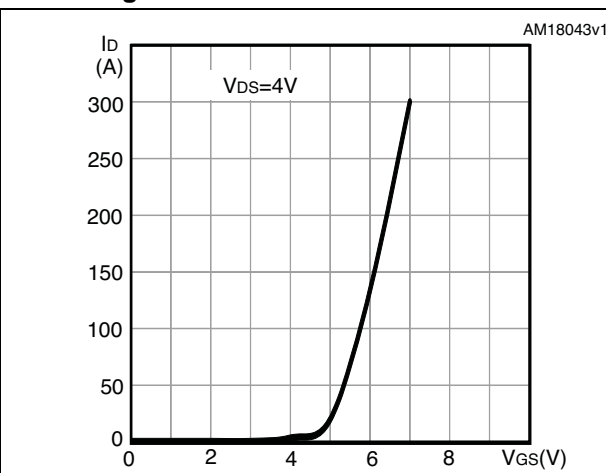


Figure 6. Gate charge vs gate-source voltage

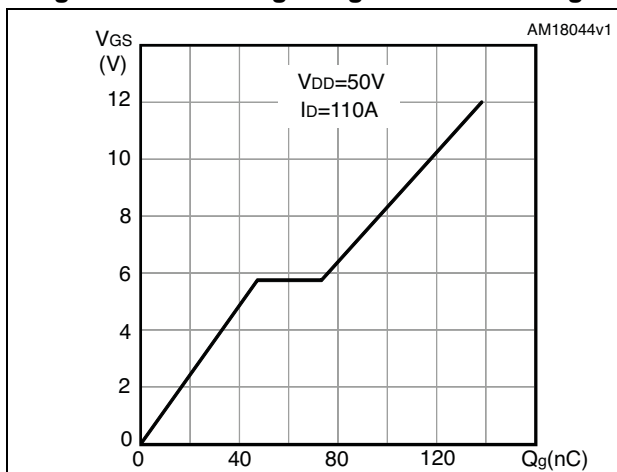


Figure 7. Static drain-source on-resistance

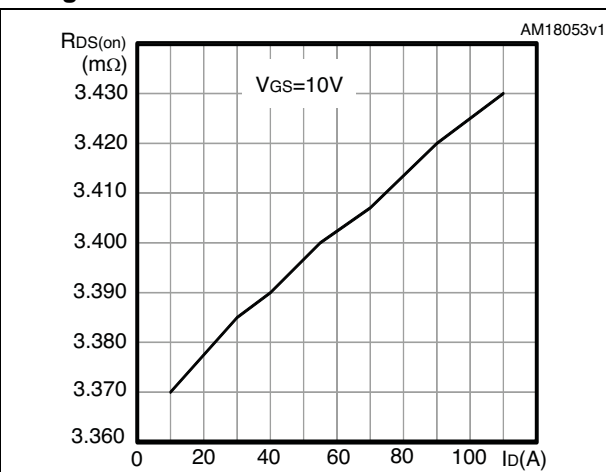


Figure 8. Capacitance variations

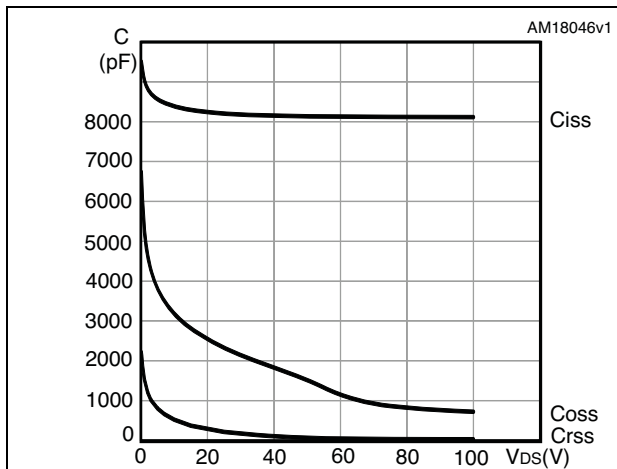


Figure 9. Normalized gate threshold voltage vs temperature

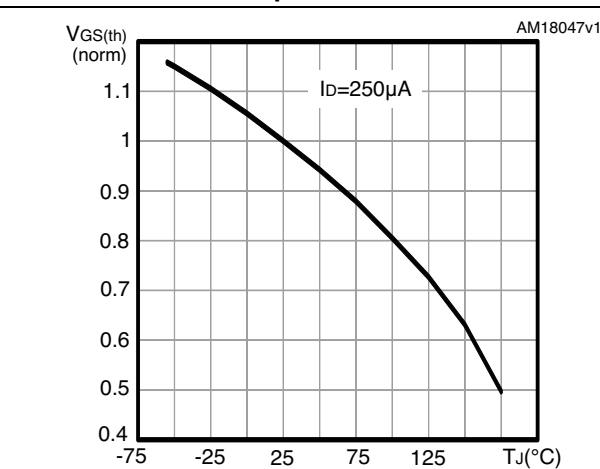


Figure 10. Normalized on-resistance vs temperature

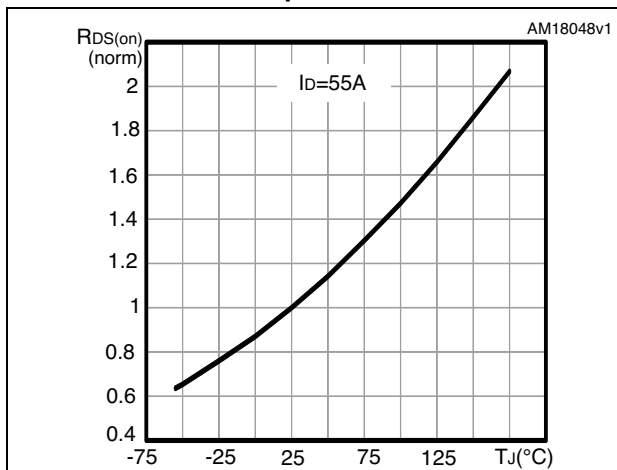


Figure 11. Normalized VDS vs temperature

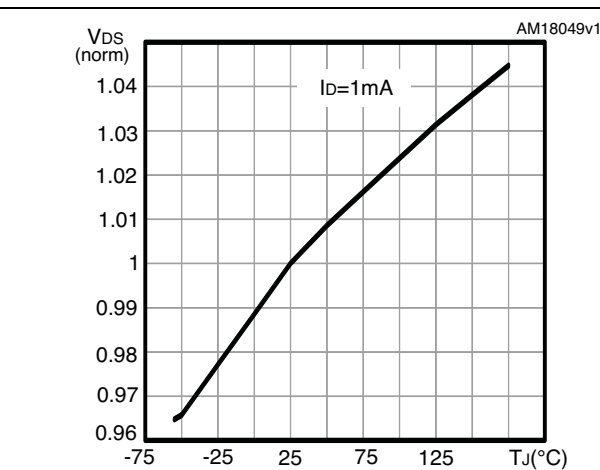
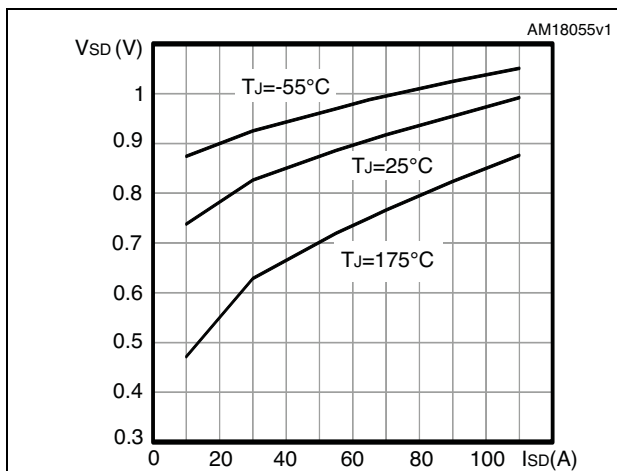


Figure 12. Source-drain diode forward characteristics



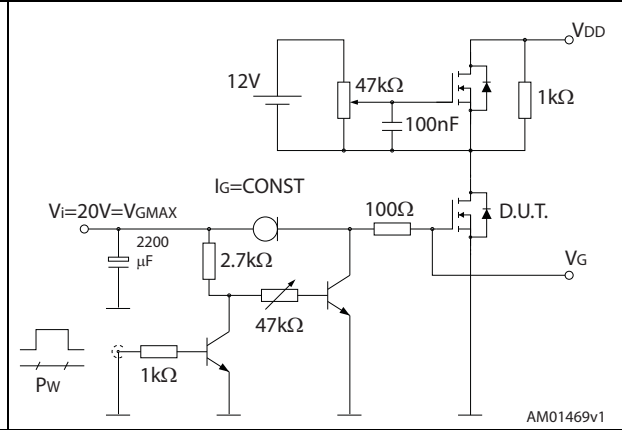
### 3 Test circuits

**Figure 13. Switching times test circuit for resistive load**



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**Figure 14. Gate charge test circuit**



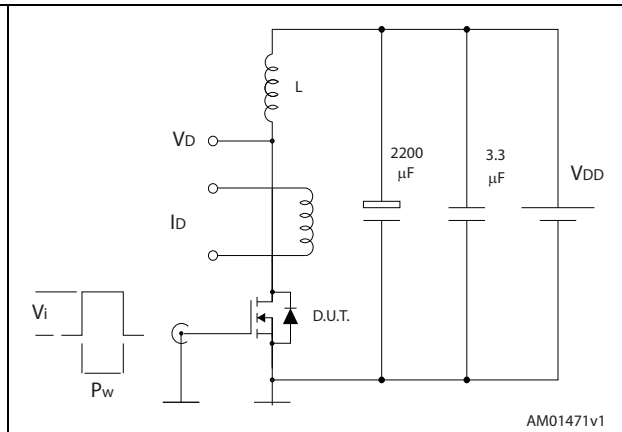
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**Figure 15. Test circuit for inductive load switching and diode recovery times**



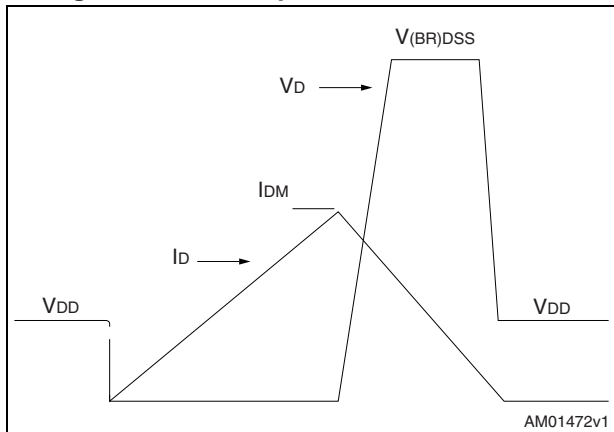
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**Figure 16. Unclamped inductive load test circuit**



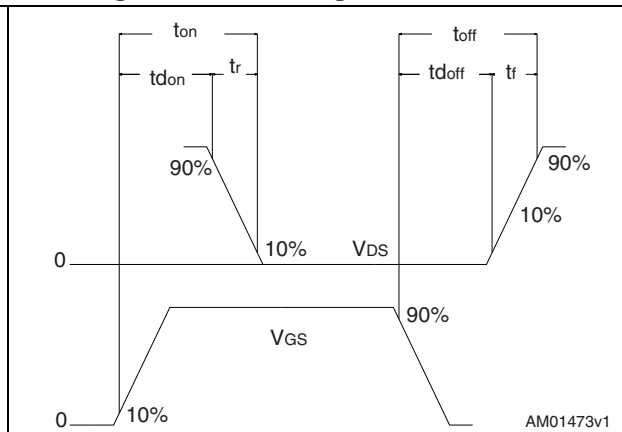
AM01471v1

**Figure 17. Unclamped inductive waveform**



AM01472v1

**Figure 18. Switching time waveform**



AM01473v1



## 4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK<sup>®</sup> packages, depending on their level of environmental compliance. ECOPACK<sup>®</sup> specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com). ECOPACK<sup>®</sup> is an ST trademark.

Figure 19. H<sup>2</sup>PAK-2 package outline

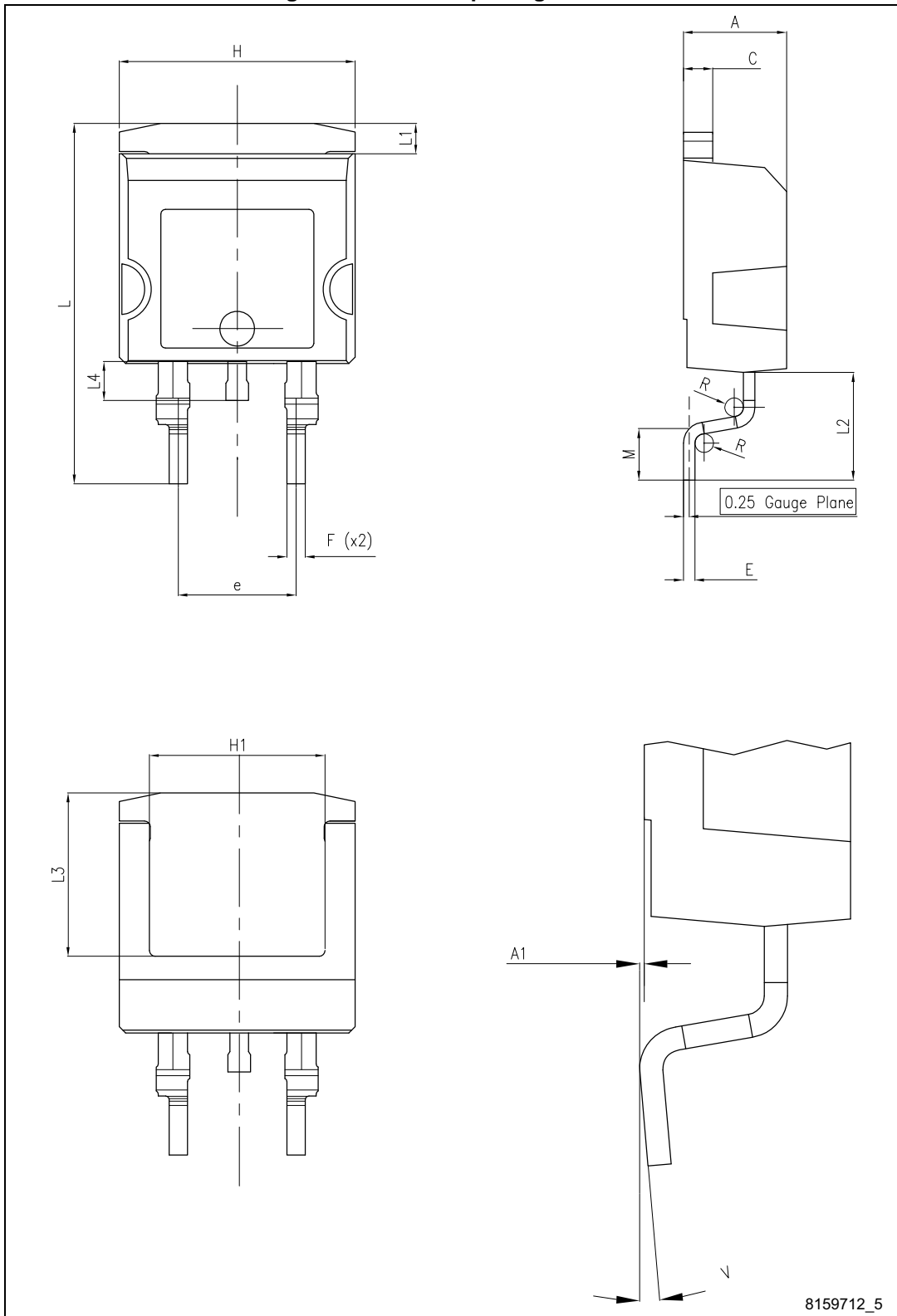
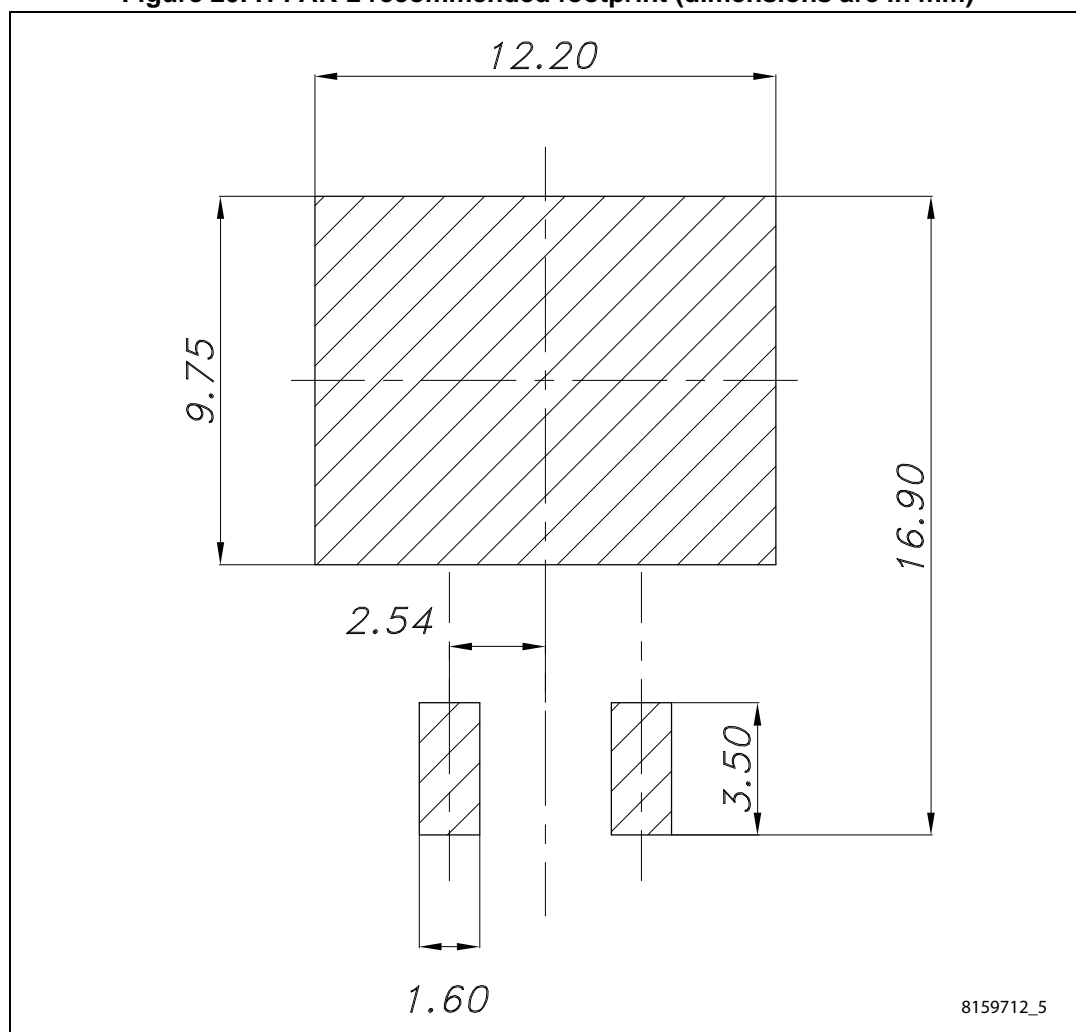


Table 8. H<sup>2</sup>PAK-2 package mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.30		4.70
A1	0.03		0.20
C	1.17		1.37
e	4.98		5.18
E	0.50		0.90
F	0.78		0.85
H	10.00		10.40
H1	7.40		7.80
L	15.30		15.80
L1	1.27		1.40
L2	4.93		5.23
L3	6.85		7.25
L4	1.5		1.7
M	2.6		2.9
R	0.20		0.60
V	0°		8°

Figure 20. H<sup>2</sup>PAK-2 recommended footprint (dimensions are in mm)



8159712\_5

# 5 Packing information

Figure 21. Tape

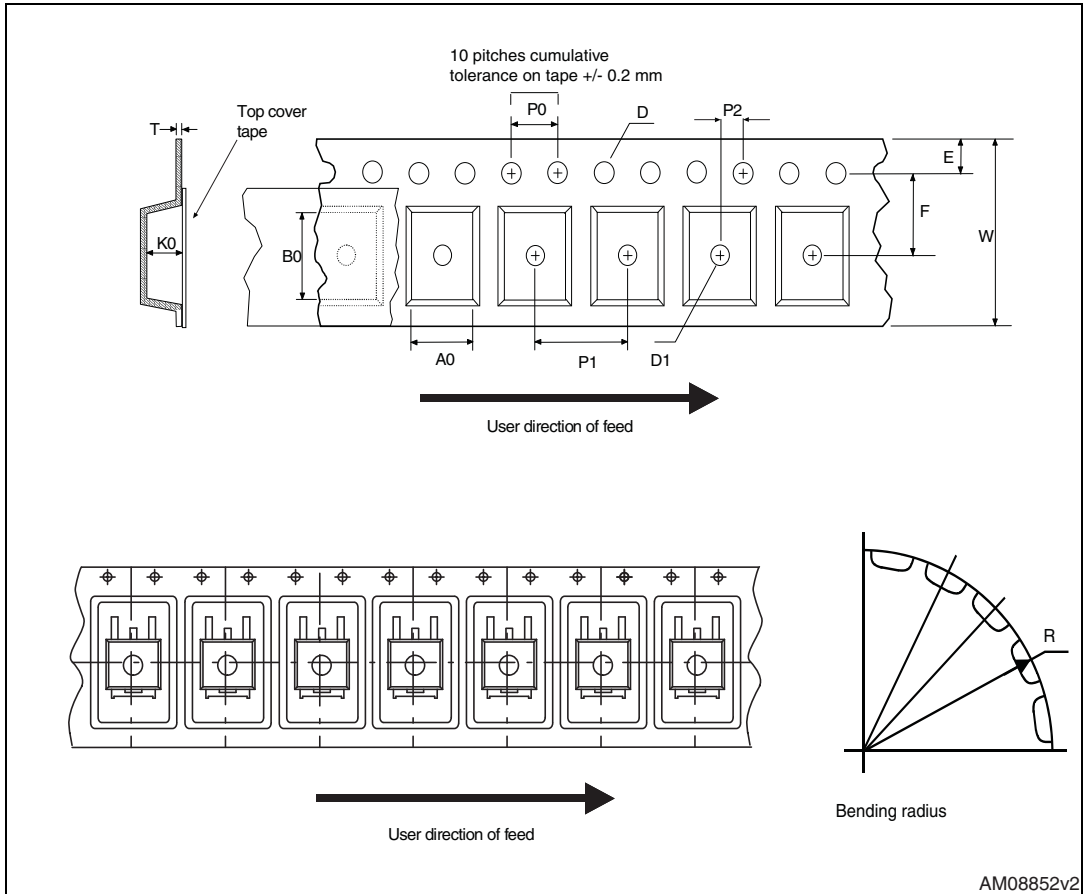


Figure 22. Reel

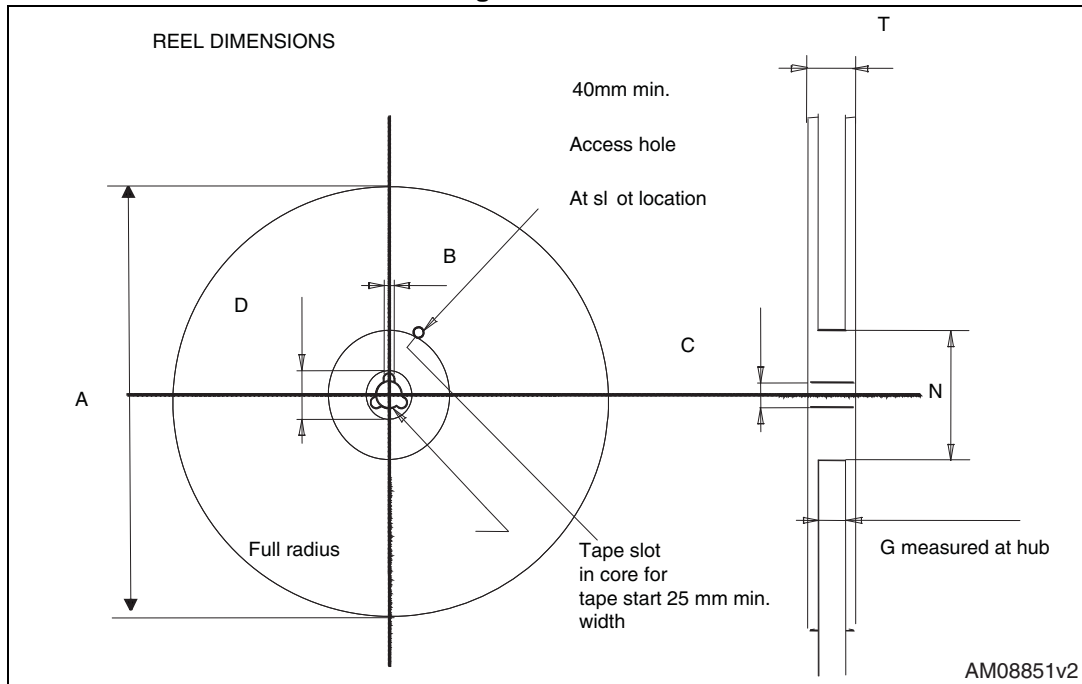


Table 9. H<sup>2</sup>PAK-2 tape and reel mechanical data

Tape			Reel		
Dim.	mm		Dim.	mm	
	Min.	Max.		Min.	Max.
A0	10.5	10.7	A		330
B0	15.7	15.9	B	1.5	
D	1.5	1.6	C	12.8	13.2
D1	1.59	1.61	D	20.2	
E	1.65	1.85	G	24.4	26.4
F	11.4	11.6	N	100	
K0	4.8	5.0	T		30.4
P0	3.9	4.1			
P1	11.9	12.1	Base qty		1000
P2	1.9	2.1	Bulk qty		1000
R	50				
T	0.25	0.35			
W	23.7	24.3			

## 6 Revision history

**Table 10. Document revision history**

Date	Revision	Changes
31-Jan-2014	1	First release. The part number previously included in datasheet DocID024552.
20-Aug-2014	2	Updated title, features and description in cover page. Updated <i>Figure 3: Thermal impedance</i> .
22-Sep-2016	3	Updated <a href="#">Section 4: Package information</a> . Minor text changes.

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