



# STH260N6F6-2

N-channel 60 V, 1.7 mΩ typ., 180 A STripFET™ VI DeepGATE™  
Power MOSFET in H<sup>2</sup>PAK-2 package

Datasheet — production data

## Features

| Order code   | V <sub>DSS</sub> | R <sub>DS(on)</sub> max | I <sub>D</sub> |
|--------------|------------------|-------------------------|----------------|
| STH260N6F6-2 | 60 V             | < 2.4 mΩ                | 180 A          |

- Low gate charge
- Very low on-resistance
- High avalanche ruggedness

## Applications

- Switching applications

## Description

This device is an N-channel Power MOSFET developed using the 6<sup>th</sup> generation of STripFET™ DeepGATE™ technology, with a new gate structure. The resulting Power MOSFET exhibits the lowest R<sub>DS(on)</sub> in all packages.

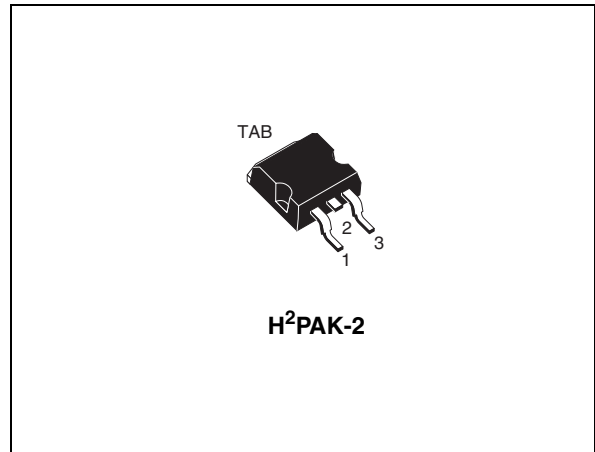


Figure 1. Internal schematic diagram

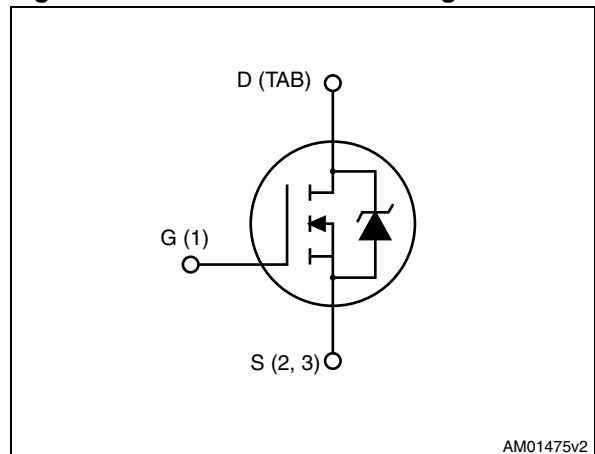


Table 1. Device summary

| Order code   | Marking | Package              | Packaging     |
|--------------|---------|----------------------|---------------|
| STH260N6F6-2 | 260N6F6 | H <sup>2</sup> PAK-2 | Tape and reel |

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# 1 Electrical ratings

**Table 2. Absolute maximum ratings**

| Symbol         | Parameter                                                         | Value       | Unit                  |
|----------------|-------------------------------------------------------------------|-------------|-----------------------|
| $V_{DS}$       | Drain-source voltage                                              | 60          | V                     |
| $V_{GS}$       | Gate-source voltage                                               | $\pm 20$    | V                     |
| $I_D$          | Drain current (continuous) at $T_C = 25\text{ }^{\circ}\text{C}$  | 180         | A                     |
| $I_D$          | Drain current (continuous) at $T_C = 100\text{ }^{\circ}\text{C}$ | 180         | A                     |
| $I_{DM}^{(1)}$ | Drain current (pulsed)                                            | 720         | A                     |
| $P_{TOT}$      | Total dissipation at $T_C = 25\text{ }^{\circ}\text{C}$           | 300         | W                     |
|                | Derating factor                                                   | 2           | W/ $^{\circ}\text{C}$ |
| $T_{stg}$      | Storage temperature                                               | - 55 to 175 | $^{\circ}\text{C}$    |
| $T_j$          | Operating junction temperature                                    |             |                       |

1. Current limited by package.

**Table 3. Thermal data**

| Symbol              | Parameter                                      | Value | Unit                        |
|---------------------|------------------------------------------------|-------|-----------------------------|
| $R_{thj-case}$      | Thermal resistance junction-case max           | 0.5   | $^{\circ}\text{C}/\text{W}$ |
| $R_{thj-pcb}^{(1)}$ | Thermal resistance junction-pcb max            | 35    | $^{\circ}\text{C}/\text{W}$ |
| $T_l$               | Maximum lead temperature for soldering purpose | 300   | $^{\circ}\text{C}$          |

1. When mounted on FR-4 board of 1 inch<sup>2</sup>, 2 oz Cu.

## 2 Electrical characteristics

( $T_{CASE} = 25\text{ °C}$  unless otherwise specified)

**Table 4. On/off states**

| Symbol        | Parameter                                        | Test conditions                                                       | Min. | Typ. | Max.      | Unit                           |
|---------------|--------------------------------------------------|-----------------------------------------------------------------------|------|------|-----------|--------------------------------|
| $V_{(BR)DSS}$ | Drain-source breakdown voltage ( $V_{GS} = 0$ )  | $I_D = 250\text{ }\mu\text{A}$                                        | 60   |      |           | V                              |
| $I_{DSS}$     | Zero gate voltage Drain current ( $V_{GS} = 0$ ) | $V_{DS} = 60\text{ V}$<br>$V_{DS} = 60\text{ V}, T_C = 125\text{ °C}$ |      |      | 1<br>100  | $\mu\text{A}$<br>$\mu\text{A}$ |
| $I_{GSS}$     | Gate-body leakage current ( $V_{DS} = 0$ )       | $V_{GS} = \pm 20\text{ V}$                                            |      |      | $\pm 100$ | nA                             |
| $V_{GS(th)}$  | Gate threshold voltage                           | $V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$                       | 2    |      | 4         | V                              |
| $R_{DS(on)}$  | Static drain-source on-resistance                | $V_{GS} = 10\text{ V}, I_D = 60\text{ A}$                             |      | 1.7  | 2.4       | m $\Omega$                     |

**Table 5. Dynamic**

| Symbol    | Parameter                    | Test conditions                                                                          | Min. | Typ.  | Max. | Unit |
|-----------|------------------------------|------------------------------------------------------------------------------------------|------|-------|------|------|
| $C_{iss}$ | Input capacitance            | $V_{DS} = 25\text{ V}, f = 1\text{ MHz},$<br>$V_{GS} = 0$                                | -    | 11800 | -    | pF   |
| $C_{oss}$ | Output capacitance           |                                                                                          |      | 1235  |      | pF   |
| $C_{rss}$ | Reverse transfer capacitance |                                                                                          |      | 488   |      | pF   |
| $Q_g$     | Total gate charge            | $V_{DD} = 30\text{ V}, I_D = 120\text{ A},$<br>$V_{GS} = 10\text{ V}$<br>(see Figure 14) | -    | 183   | -    | nC   |
| $Q_{gs}$  | Gate-source charge           |                                                                                          |      | 53    |      | nC   |
| $Q_{gd}$  | Gate-drain charge            |                                                                                          |      | 41    |      | nC   |

**Table 6. Switching times**

| Symbol       | Parameter           | Test conditions                                                                                                 | Min. | Typ.  | Max. | Unit |
|--------------|---------------------|-----------------------------------------------------------------------------------------------------------------|------|-------|------|------|
| $t_{d(on)}$  | Turn-on delay time  | $V_{DD} = 30\text{ V}, I_D = 60\text{ A}$<br>$R_G = 4.7\text{ }\Omega, V_{GS} = 10\text{ V}$<br>(see Figure 13) | -    | 31.4  | -    | ns   |
| $t_r$        | Rise time           |                                                                                                                 |      | 165   |      | ns   |
| $t_{d(off)}$ | Turn-off-delay time |                                                                                                                 | -    | 144.4 | -    | ns   |
| $t_f$        | Fall time           |                                                                                                                 |      | 62.6  |      | ns   |

**Table 7. Source drain diode**

| Symbol          | Parameter                     | Test conditions                                                                                                                                             | Min. | Typ. | Max. | Unit |
|-----------------|-------------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------|------|------|------|------|
| $I_{SD}$        | Source-drain current          |                                                                                                                                                             |      |      | 180  | A    |
| $I_{SDM}^{(1)}$ | Source-drain current (pulsed) |                                                                                                                                                             |      |      | 720  | A    |
| $V_{SD}^{(2)}$  | Forward on voltage            | $I_{SD} = 180 \text{ A}$ , $V_{GS} = 0$                                                                                                                     |      |      | 1.1  | V    |
| $t_{rr}$        | Reverse recovery time         | $I_{SD} = 120 \text{ A}$ , $V_{DD} = 48 \text{ V}$<br>$di/dt = 100 \text{ A}/\mu\text{s}$ ,<br>$T_j = 150 \text{ }^\circ\text{C}$<br><i>(see Figure 15)</i> | -    | 55.6 |      | ns   |
| $Q_{rr}$        | Reverse recovery charge       |                                                                                                                                                             |      | 116  |      | nC   |
| $I_{RRM}$       | Reverse recovery current      |                                                                                                                                                             |      | 3.8  |      | A    |

1. Current limited by package.
2. Pulsed: pulse duration = 300  $\mu\text{s}$ , duty cycle 1.5%

## 2.1 Electrical characteristics (curves)

Figure 2. Safe operating area

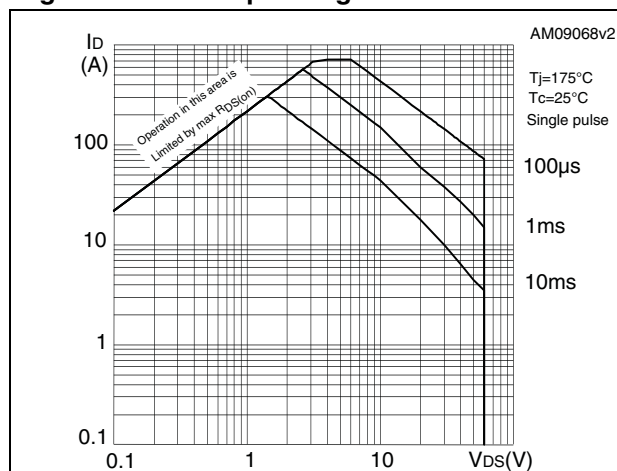


Figure 3. Thermal impedance

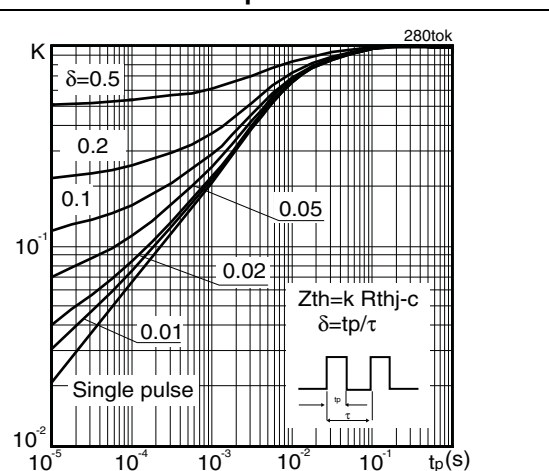


Figure 4. Output characteristics

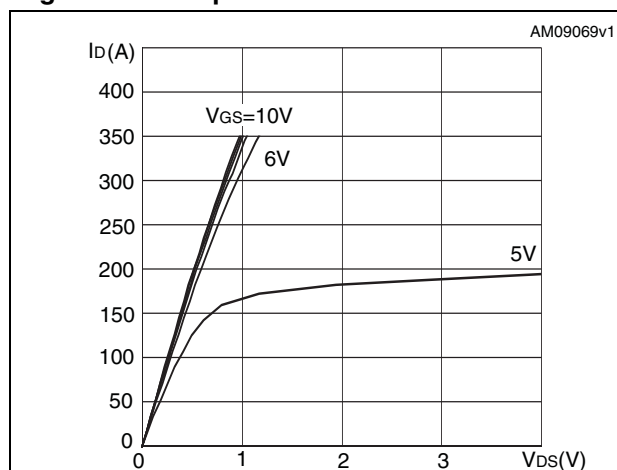


Figure 5. Transfer characteristics

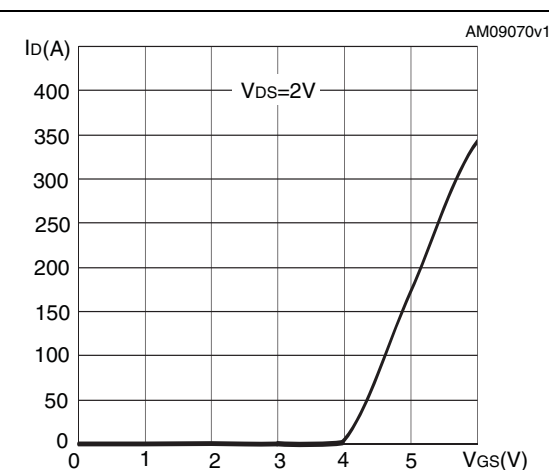
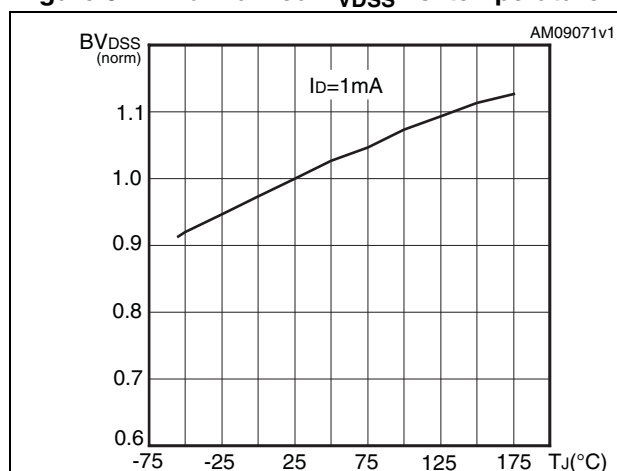
Figure 6. Normalized  $B_{V_{DS}}$  vs. temperature

Figure 7. Static drain-source on-resistance

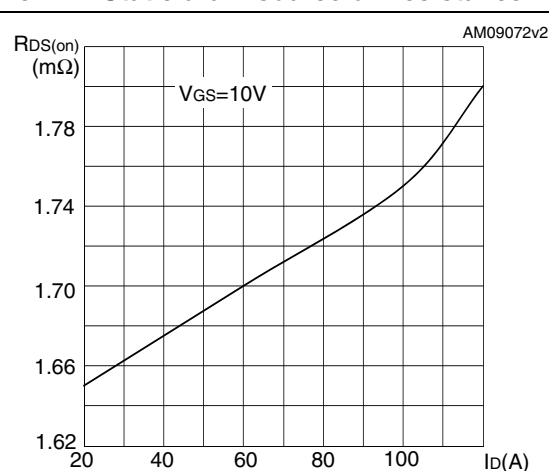


Figure 8. Gate charge vs. gate-source voltage

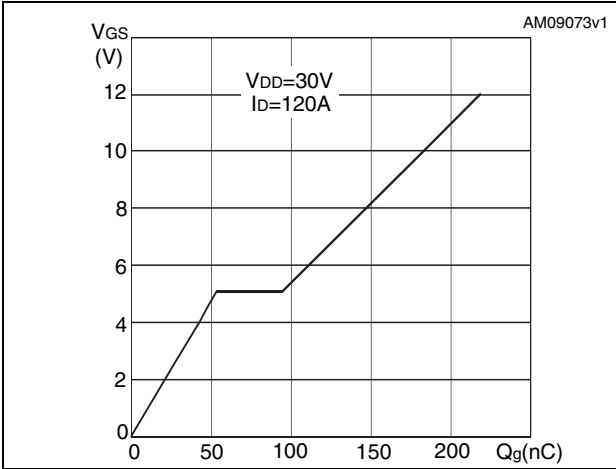


Figure 9. Capacitance variations

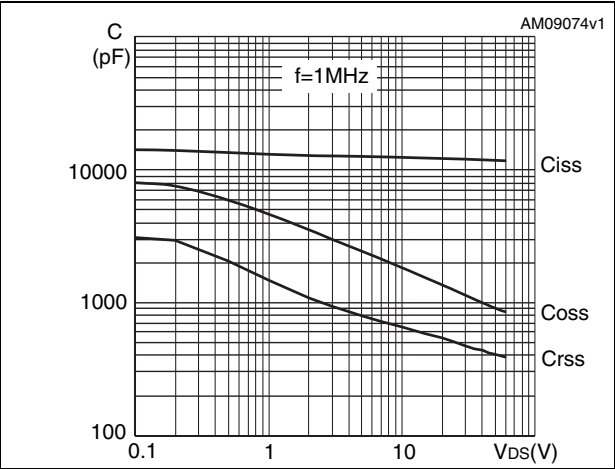


Figure 10. Normalized gate threshold voltage vs. temperature

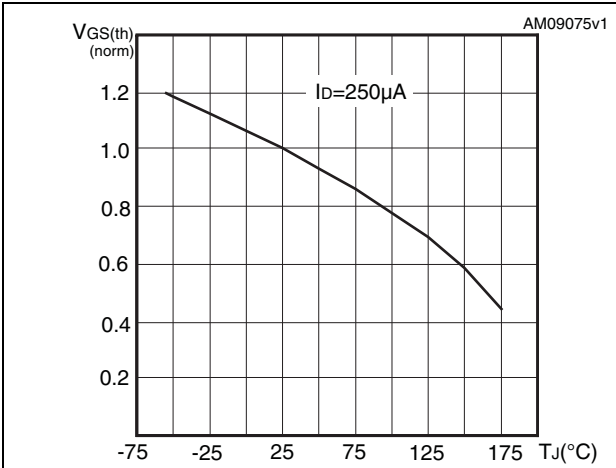


Figure 11. Normalized on-resistance vs. temperature

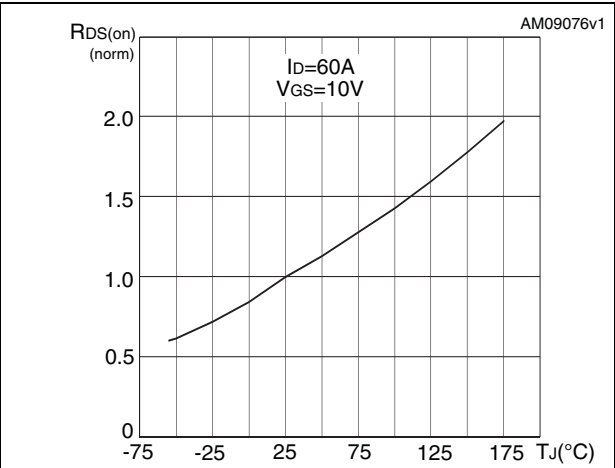
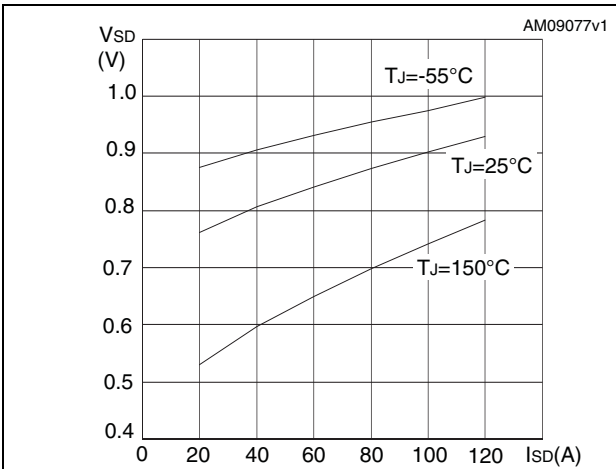
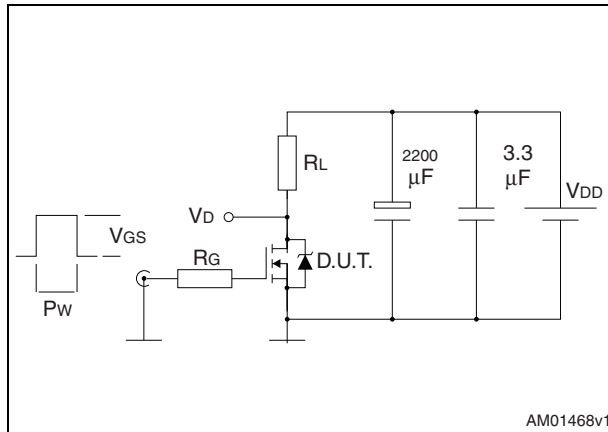


Figure 12. Source-drain diode forward characteristics

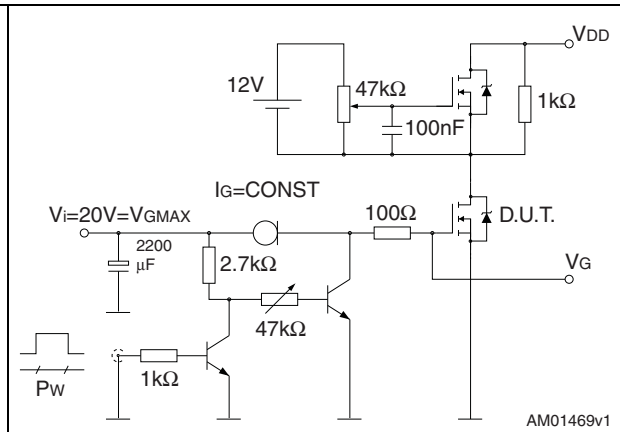


### 3 Test circuits

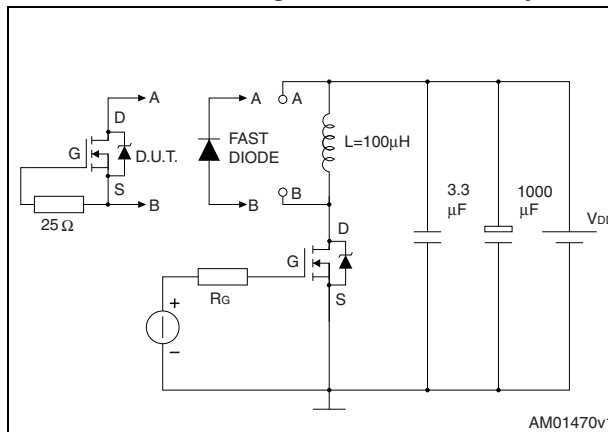
**Figure 13. Switching times test circuit for resistive load**



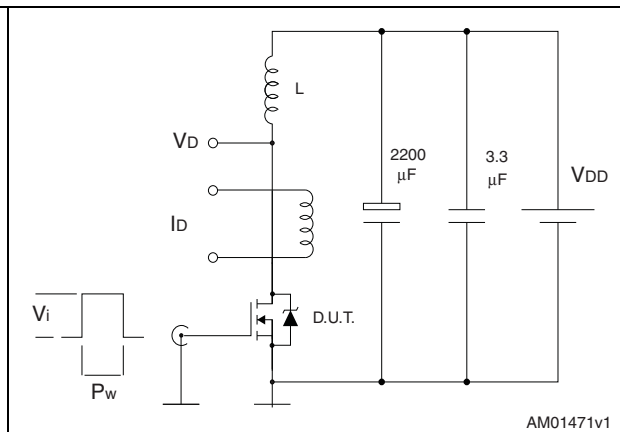
**Figure 14. Gate charge test circuit**



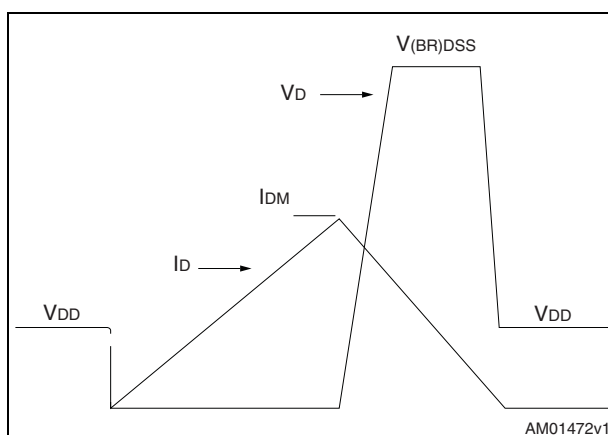
**Figure 15. Test circuit for inductive load switching and diode recovery times**



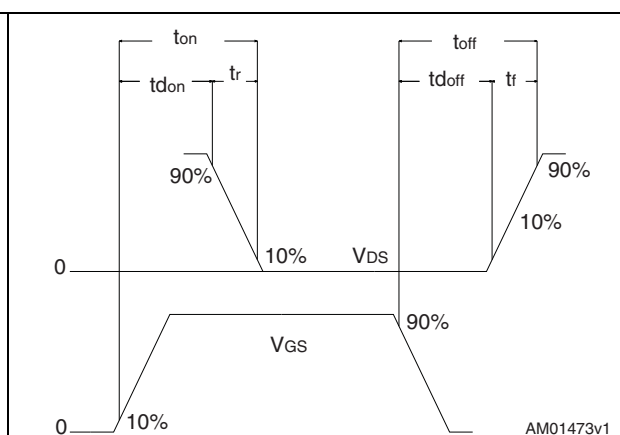
**Figure 16. Unclamped inductive load test circuit**



**Figure 17. Unclamped inductive waveform**



**Figure 18. Switching time waveform**



## 4      **Package mechanical data**

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com). ECOPACK is an ST trademark.

Table 8. H<sup>2</sup>PAK 2 leads mechanical data

| Dim. | mm    |      |       |
|------|-------|------|-------|
|      | Min.  | Typ. | Max.  |
| A    | 4.30  | -    | 4.80  |
| A1   | 0.03  |      | 0.20  |
| C    | 1.17  |      | 1.37  |
| e    | 4.98  |      | 5.18  |
| E    | 0.50  |      | 0.90  |
| F    | 0.78  |      | 0.85  |
| H    | 10.00 |      | 10.40 |
| H1   | 7.40  |      | 7.80  |
| L    | 15.30 |      | 15.80 |
| L1   | 1.27  |      | 1.40  |
| L2   | 4.93  |      | 5.23  |
| L3   | 6.85  |      | 7.25  |
| L4   | 1.5   |      | 1.7   |
| M    | 2.6   |      | 2.9   |
| R    | 0.20  |      | 0.60  |
| V    | 0°    |      | 8°    |

Figure 19. H<sup>2</sup>PAK 2 leads drawing

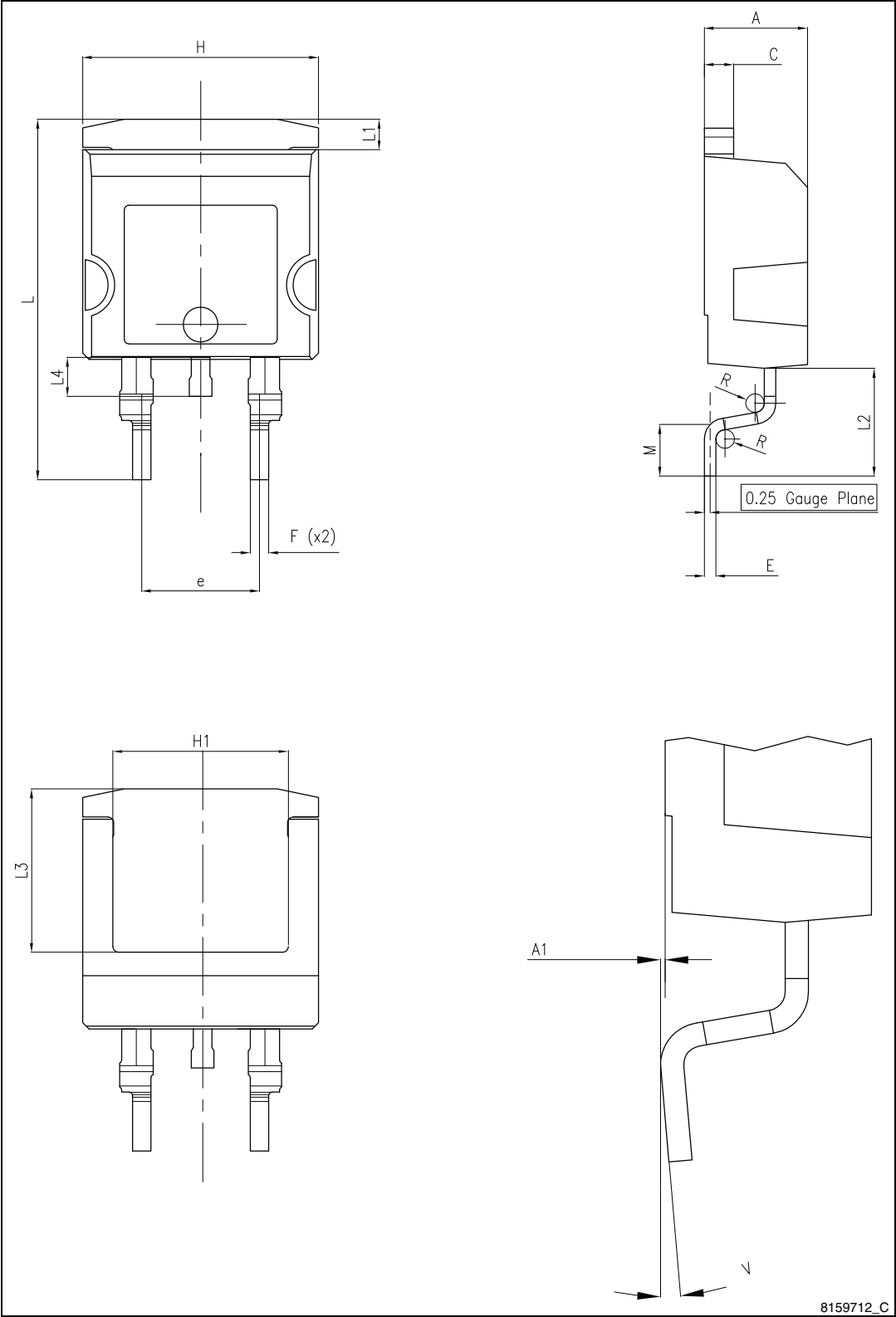
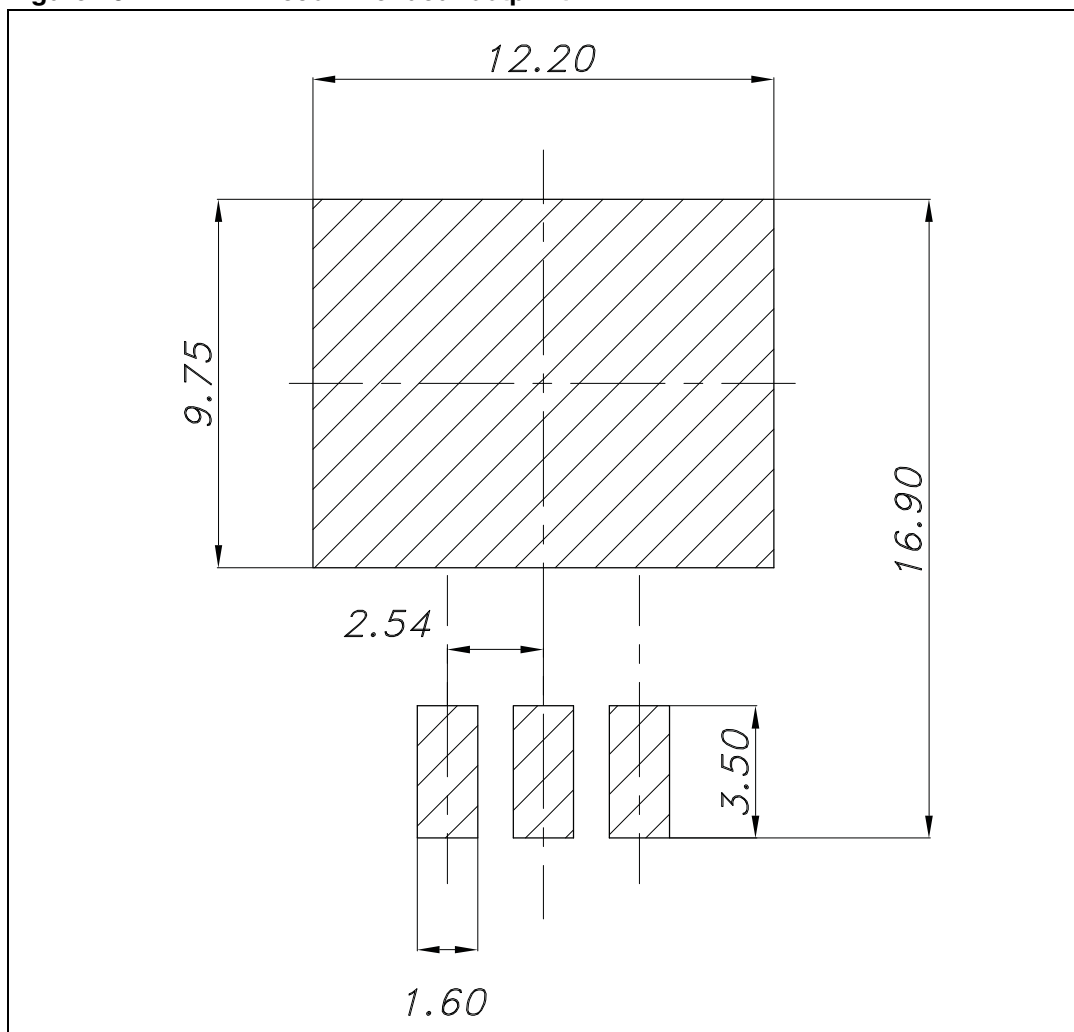


Figure 20. H<sup>2</sup>PAK 2 recommended footprint

## 5 Revision history

**Table 9. Document revision history**

| Date        | Revision | Changes                                                                            |
|-------------|----------|------------------------------------------------------------------------------------|
| 31-May-2011 | 1        | First release.                                                                     |
| 25-Aug-2011 | 2        | Updated mechanical data.                                                           |
| 01-Feb-2012 | 3        | Updated <a href="#">Table 2: Absolute maximum ratings</a> .<br>Minor text changes. |
| 06-Jul-2012 | 4        | <a href="#">Section 2.1: Electrical characteristics (curves)</a> has been added.   |

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