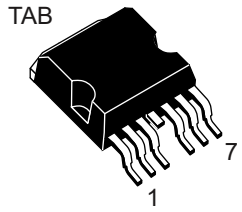
STH270N4F3-6

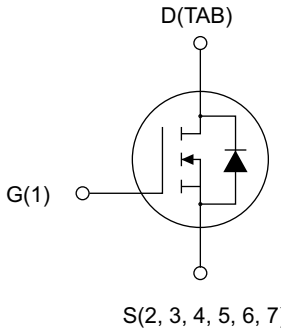
Automotive-grade N-channel 40 V, 1.4 mΩ typ., 180 A STripFET™ F3 Power MOSFET in H^{2}PAK-6 package

Datasheet – production data



H^{2}PAK-6

Figure 1. Internal schematic diagram



Features

Order codes	V_{DS}	$R_{DS(on)}$ max	I_D
STH270N4F3-6	40 V	1.7 mΩ	180 A

- Designed for automotive applications and AEC-Q101 qualified
- Conduction losses reduced
- Low profile, very low parasitic inductance, high current package

Applications

- Switching applications

Description

This device is an N-channel Power MOSFET developed using STripFET™ F3 technology. It is designed to minimize on-resistance and gate charge to provide superior switching performance.

Table 1. Device summary

Order code	Marking	Package	Packaging
STH270N4F3-6	270N4F3	H^{2}PAK-6	Tape and reel

Contents

1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage	40	
V_{GS}	Gate-source voltage	± 20	V
I_D (1)	Drain current (continuous) at T_C = 25 °C	180	A
I_D (1)	Drain current (continuous) at T_C = 100 °C	180	A
I_{DM} (2)	Drain current (pulsed)	720	A
P_{TOT}	Total dissipation at T_C = 25 °C	300	W
E_{AS} (3)	Single pulse avalanche energy	1000	mJ
T_{stg}	Storage temperature	- 55 to 175	°C
T_j	Operating junction temperature		°C

1. Current limited by package.
2. Pulse width limited by safe operating area
3. Starting T_J=25°C, I_D=80 A, V_{DD}=32 V

Table 3. Thermal data

Symbol	Parameter	Value	Unit
$R_{thj\text{-}case}$	Thermal resistance junction-case max	0.5	°C/W
$R_{thj\text{-}pcb}$ (1)	Thermal resistance junction-pcb max	35	°C/W

1. When mounted on FR-4 board of 1 inch², 2oz Cu.

2 Electrical characteristics

(T_C = 25 °C unless otherwise specified)

Table 4. On /off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0, I_D = 250 µA	40			V
I_{DSS}	Zero gate voltage drain current	V_{GS} = 0, V_{DS} = 40 V			10	µA
		V_{GS} = 0, V_{DS} = 40 V, T_C=125 °C			100	µA
I_{GSS}	Gate-body leakage current	V_{DS} = 0, V_{GS} = ± 20 V			±200	nA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 250 µA	2		4	V
$R_{DS(on)}$	Static drain-source on-resistance	V_{GS} = 10 V, I_D = 80 A		1.4	1.7	mΩ

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	V_{DS} = 25 V, f = 1 MHz, V_{GS} = 0	-	7400	-	pF
C_{oss}	Output capacitance		-	1800	-	pF
C_{rss}	Reverse transfer capacitance		-	50	-	pF
Q_g	Total gate charge	V_{DD} = 20 V, I_D = 160 A, V_{GS} = 10 V (see *Figure 14*)	-	110	150	nC
Q_{gs}	Gate-source charge		-	30	-	nC
Q_{gd}	Gate-drain charge		-	25	-	nC

Table 6. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	V_{DD} = 20 V, I_D = 80 A, R_G = 4.7 Ω, V_{GS} = 10 V (see *Figure 2*)	-	25	-	ns
t_r	Rise time		-	180	-	ns
$t_{d(off)}$	Turn-off delay time		-	110	-	ns
t_f	Fall time		-	45	-	ns

Table 7. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD} (1)	Source-drain current		-		180	A
I_{SDM} (2)	Source-drain current (pulsed)		-		720	A
V_{SD} (3)	Forward on voltage	I_{SD} = 180 A, V_{GS} = 0	-		1.5	V
t_{rr}	Reverse recovery time	I_{SD} = 160 A, di/dt = 100 A/µs V_{DD} = 32 V, T_J=150 °C (see *Figure 15*)	-	70		ns
Q_{rr}	Reverse recovery charge		-	225		nC
I_{RRM}	Reverse recovery current		-	3.2		A

1. Current limited by package
2. Pulse width limited by safe operating area.
3. Pulsed: pulse duration=300 µs, duty cycle 1.5%

2.1 Electrical characteristics (curves)

Figure 2. Safe operating area

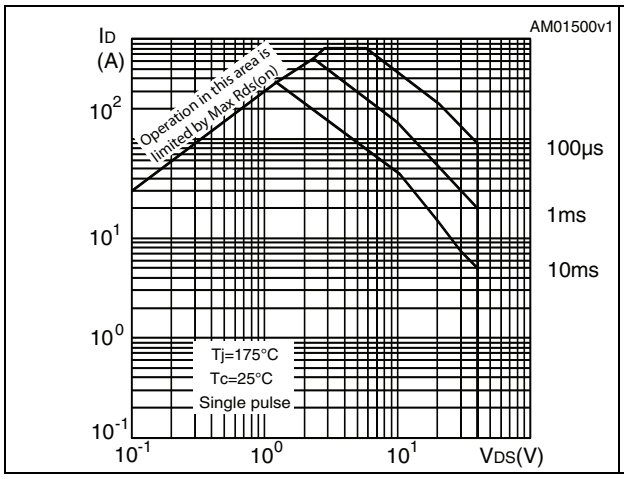


Figure 3. Thermal impedance

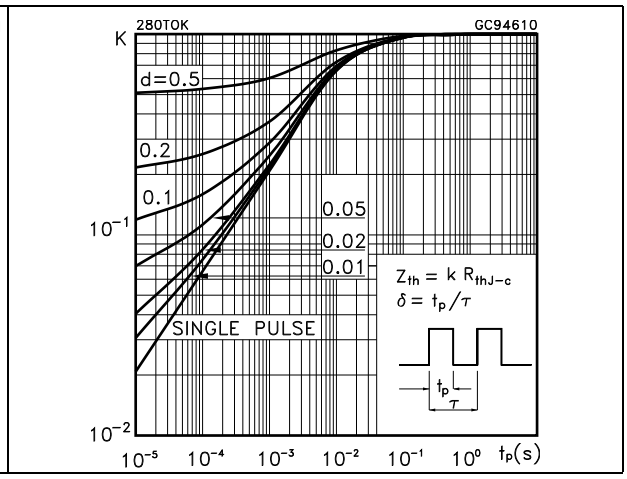


Figure 4. Output characteristics

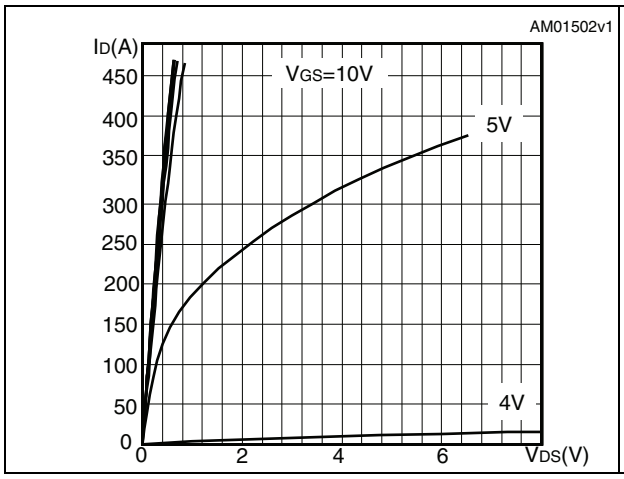


Figure 5. Transfer characteristics

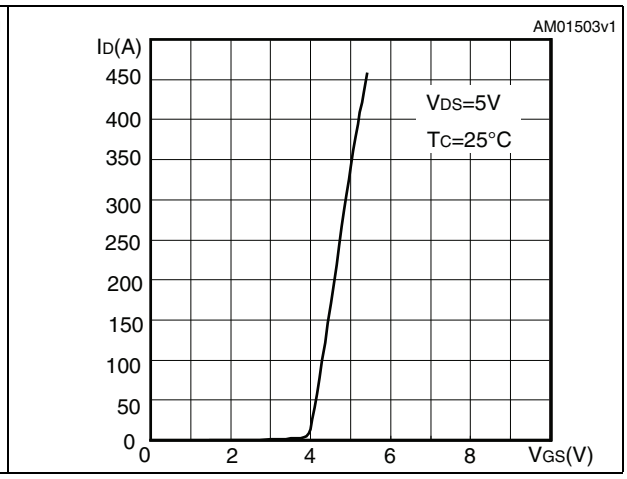


Figure 6. Gate charge vs gate-source voltage

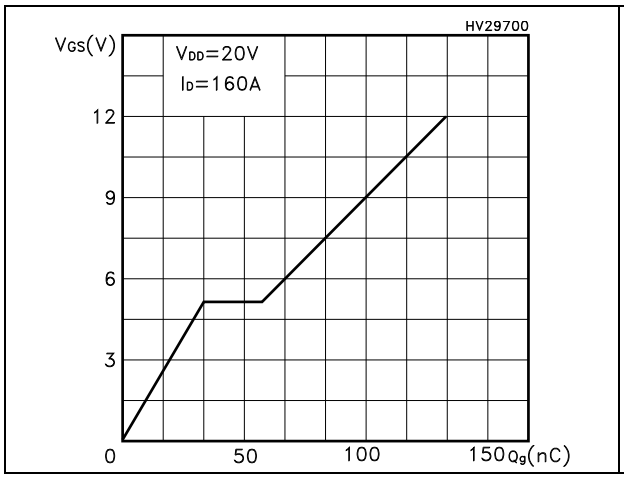


Figure 7. Static drain-source on-resistance

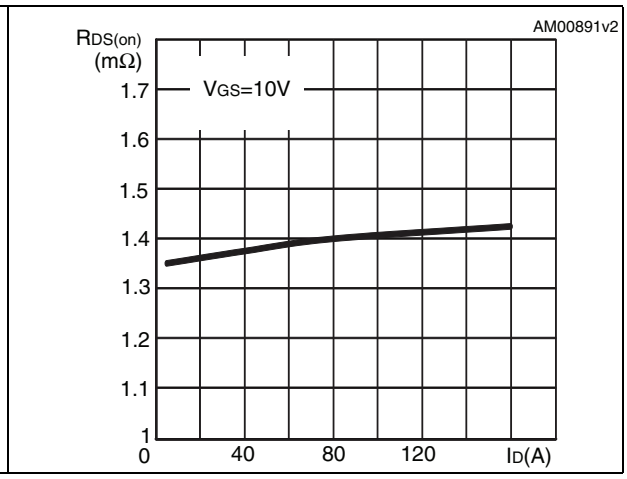


Figure 8. Capacitance variations

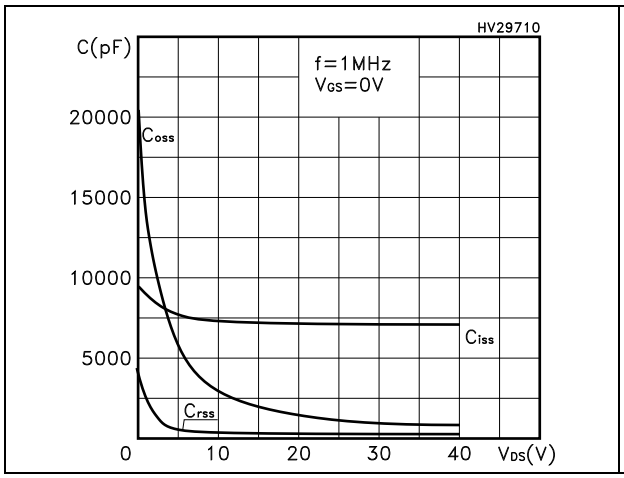


Figure 9. Normalized gate threshold voltage vs temperature

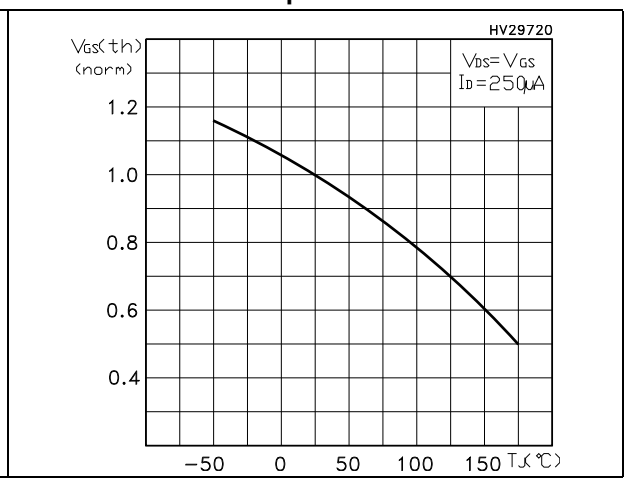


Figure 10. Normalized on-resistance vs temperature

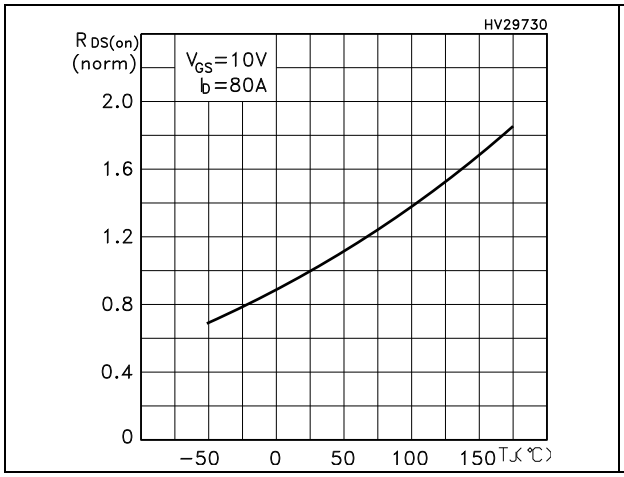


Figure 11. Normalized $V_{(BR)DSS}$ vs temperature

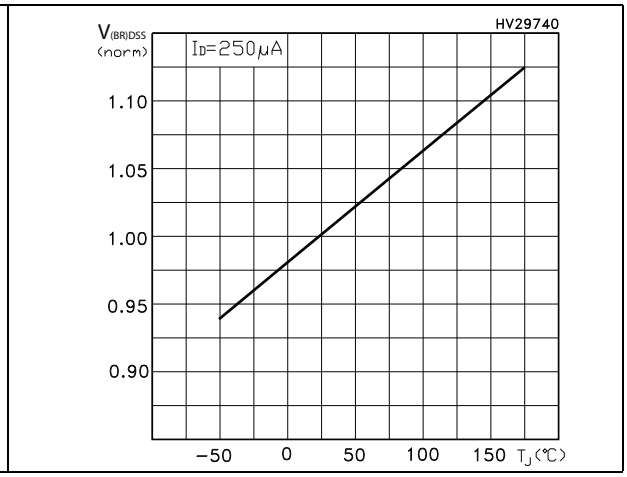
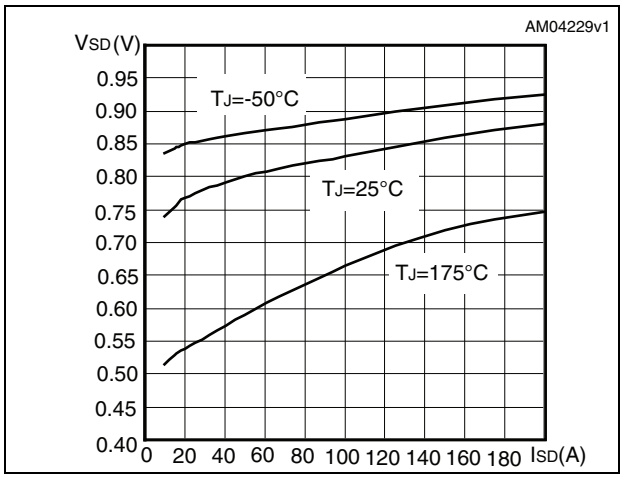


Figure 12. Drain-source diode forward characteristics



3 Test circuits

Figure 13. Switching times test circuit for resistive load

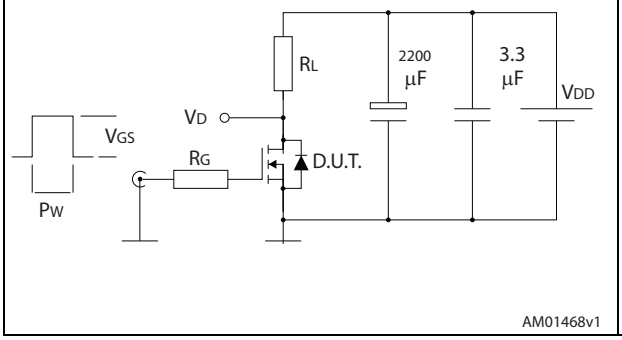


Figure 14. Gate charge test circuit

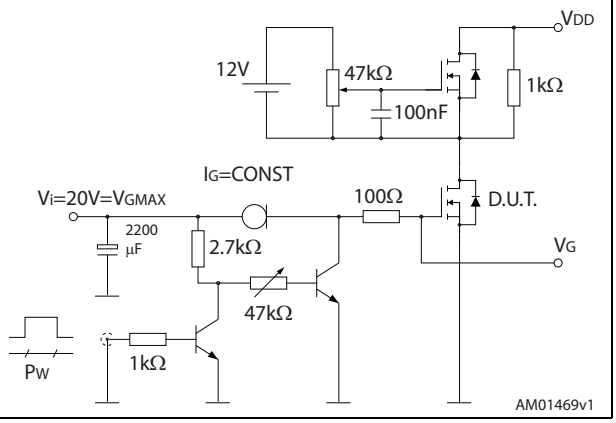


Figure 15. Test circuit for inductive load switching and diode recovery times

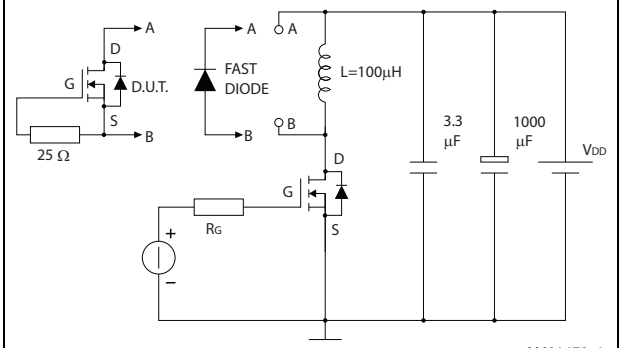


Figure 16. Unclamped inductive load test circuit

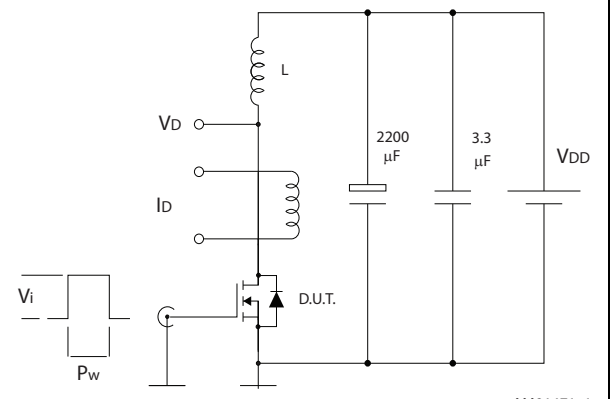


Figure 17. Unclamped inductive waveform

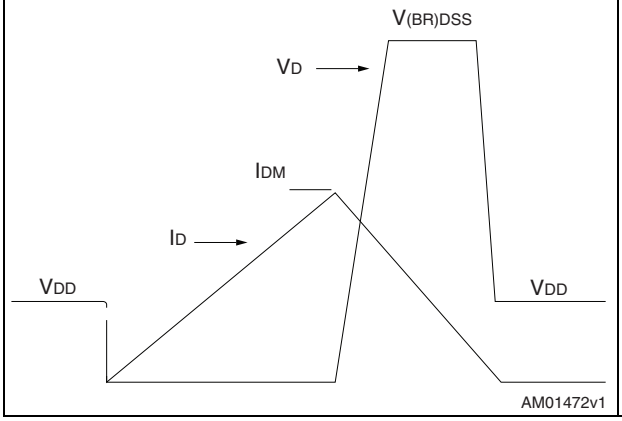
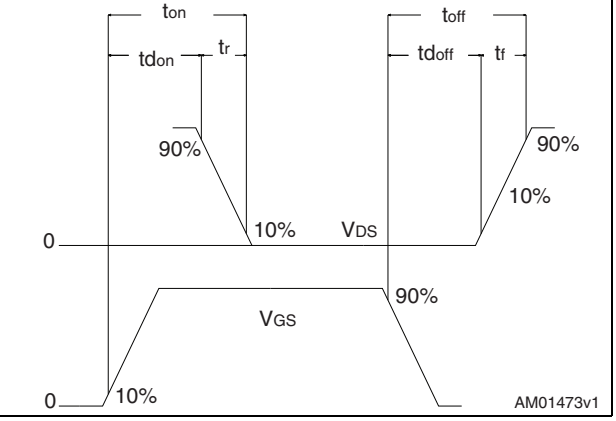


Figure 18. Switching time waveform



4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK® is an ST trademark.

4.1 H²PAK-6 package information

Figure 19. H²PAK-6 package outline

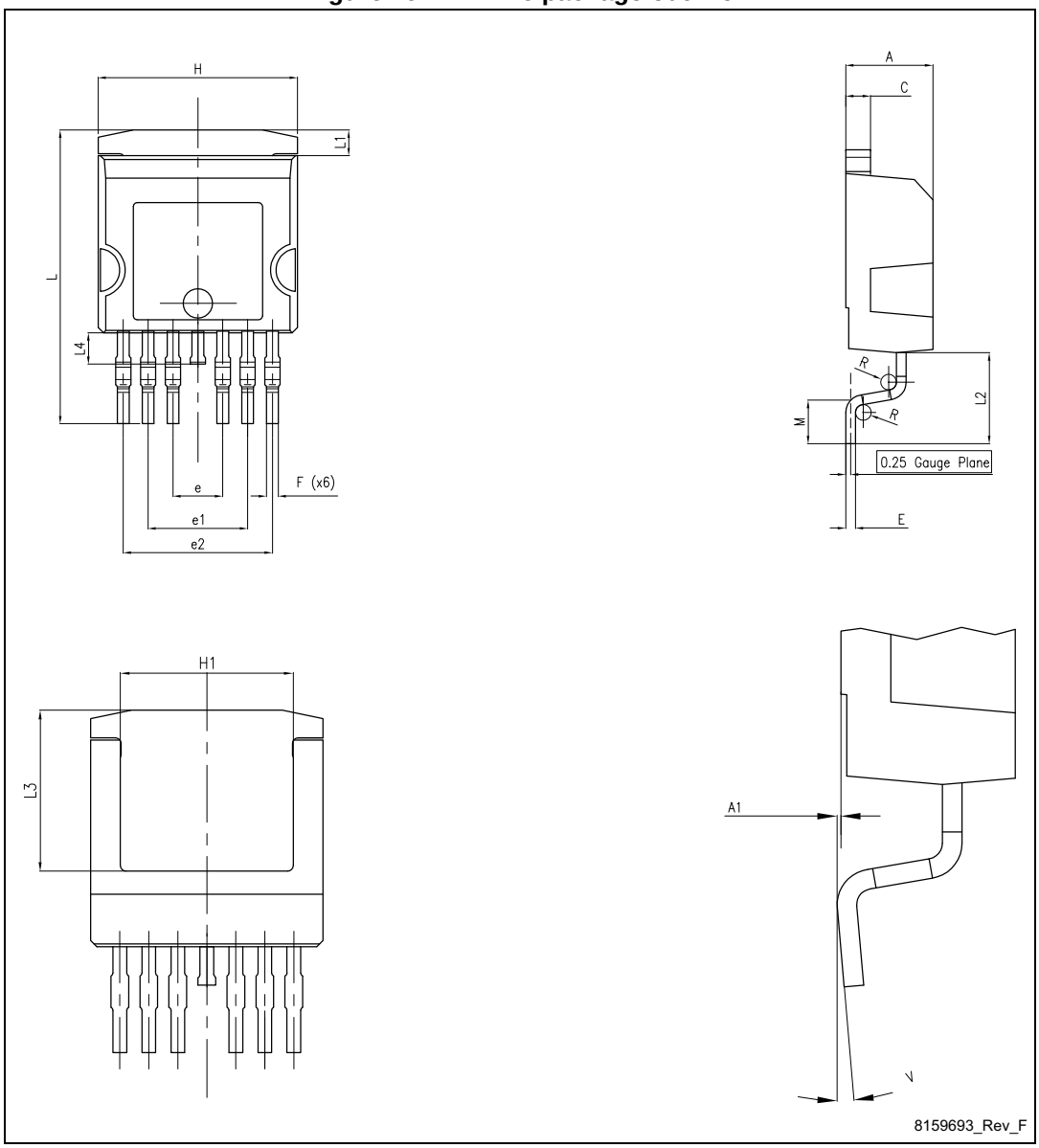
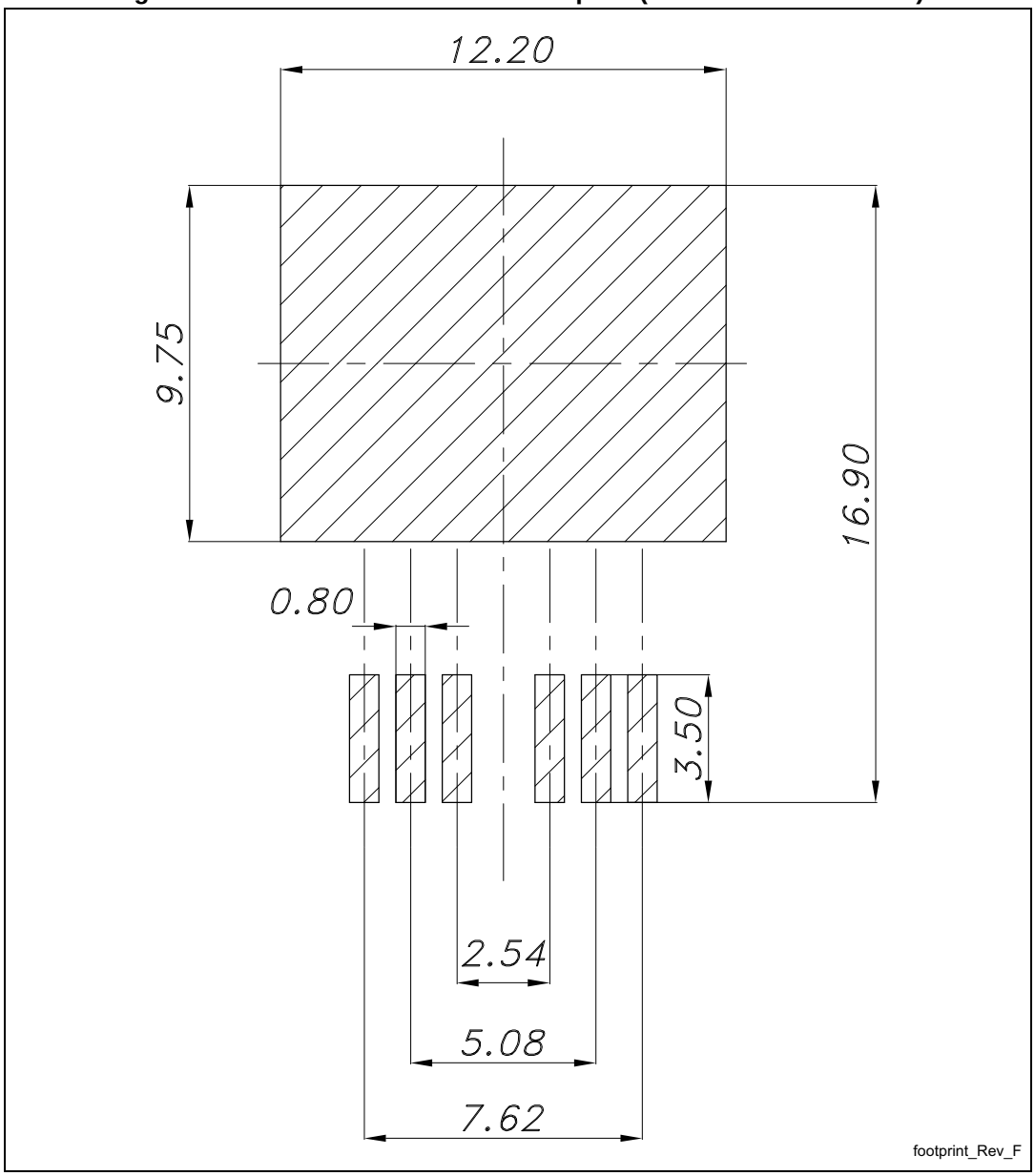


Table 8. H²PAK-6 package mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.30		4.80
A1	0.03		0.20
C	1.17		1.37
e	2.34		2.74
e1	4.88		5.28
e2	7.42		7.82
E	0.45		0.60
F	0.50		0.70
H	10.00	-	10.40
H1	7.40		7.80
L	14.75		15.25
L1	1.27		1.40
L2	4.35		4.95
L3	6.85		7.25
L4	1.5		1.75
M	1.90		2.50
R	0.20		0.60
V	0°		8°

Figure 20. H²PAK-6 recommended footprint (dimensions are in mm)



5 Packing information

Figure 21. Tape

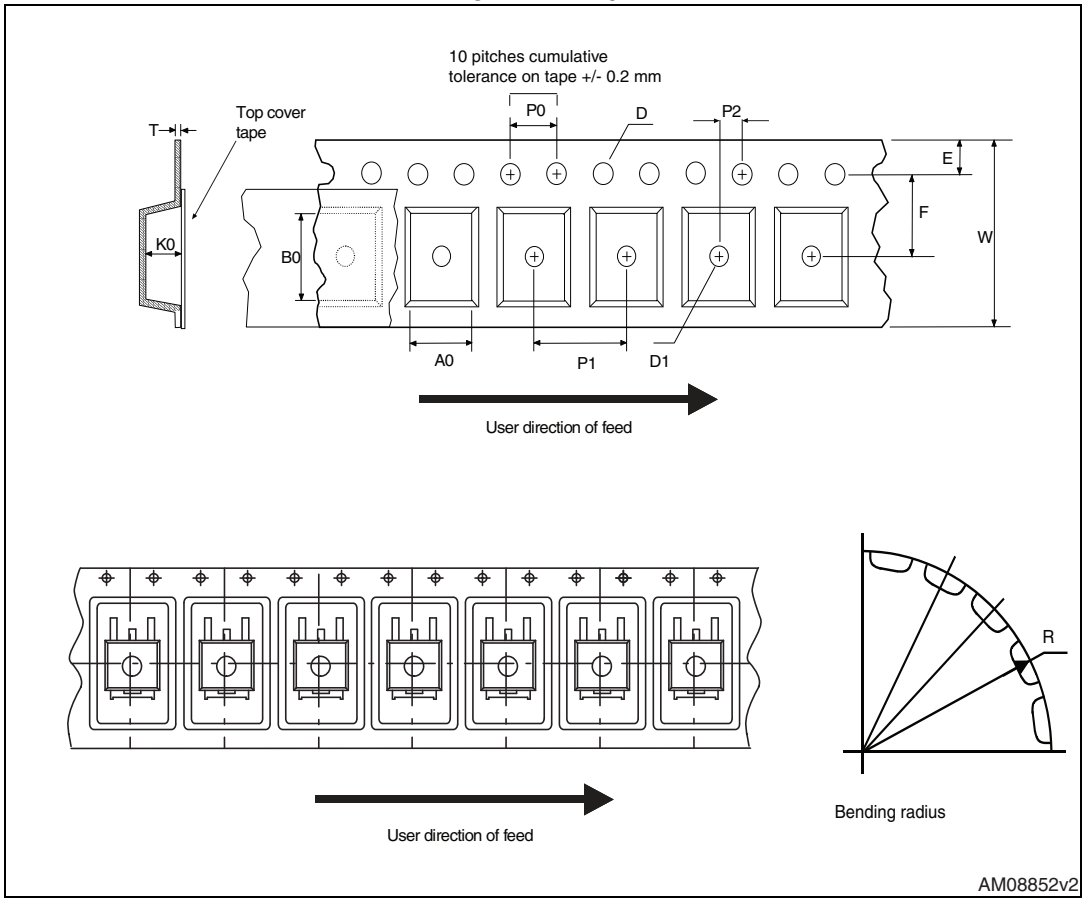


Figure 22. Reel

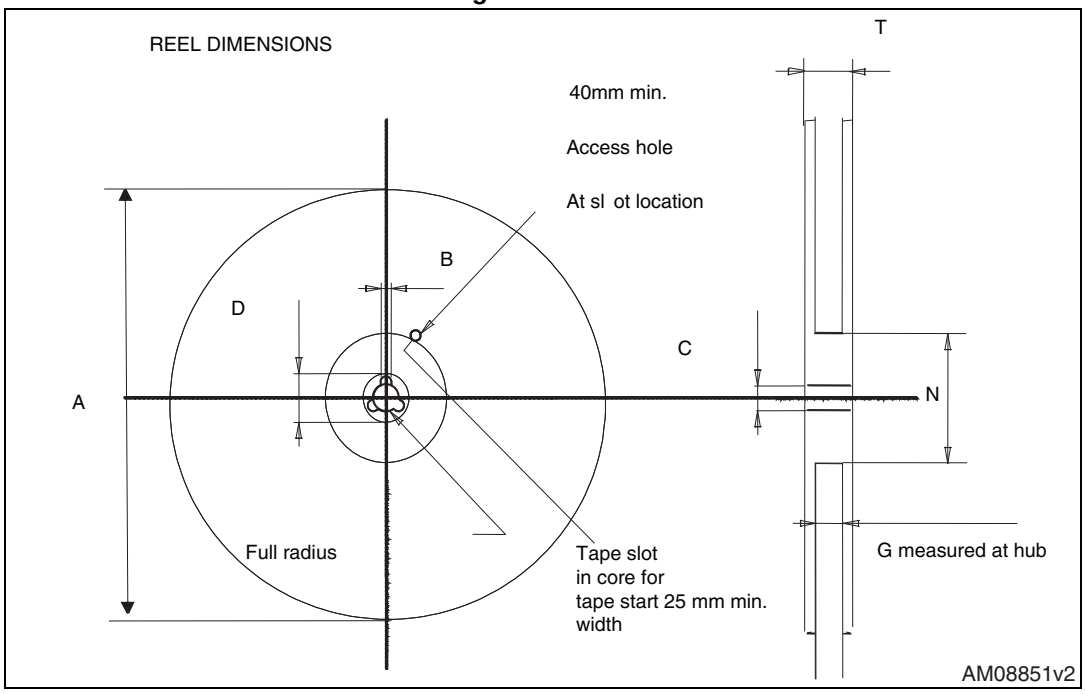


Table 9. H²PAK-2 and H²PAK-6 tape and reel mechanical data

Tape			Reel		
Dim.	mm		Dim.	mm	
	Min.	Max.		Min.	Max.
A0	10.5	10.7	A		330
B0	15.7	15.9	B	1.5	
D	1.5	1.6	C	12.8	13.2
D1	1.59	1.61	D	20.2	
E	1.65	1.85	G	24.4	26.4
F	11.4	11.6	N	100	
K0	4.8	5.0	T		30.4
P0	3.9	4.1			
P1	11.9	12.1	Base qty		1000
P2	1.9	2.1	Bulk qty		1000
R	50				
T	0.25	0.35			
W	23.7	24.3			

6 Revision history

Table 10. Document revision history

Date	Revision	Changes
22-May-2015	1	First release. Part number previously included in datasheet DocID16957.