

N-channel 100 V, 1.9 mΩ typ., 180 A, STripFET™ F7
Power MOSFETs in H²PAK-2 and H²PAK-6 packages

Datasheet - production data

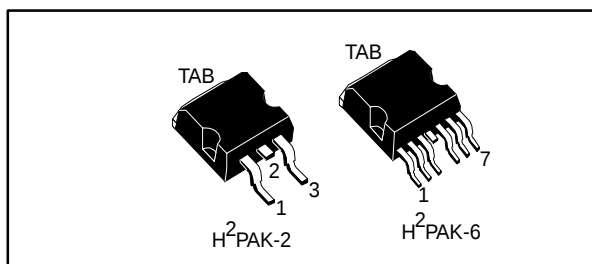
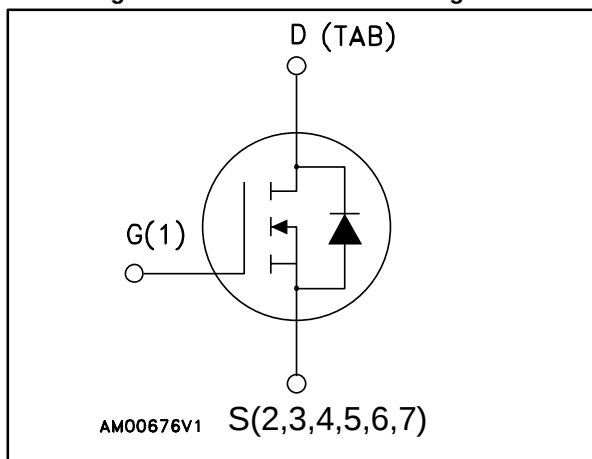


Figure 1: Internal schematic diagram



Features

Order code	V _{DS}	R _{DS(on)} max.	I _D
STH310N10F7-2	100 V	2.3 mΩ	180 A
STH310N10F7-6			

- Among the lowest R_{DS(on)} on the market
- Excellent figure of merit (FoM)
- Low C_{rss}/C_{iss} ratio for EMI immunity
- High avalanche ruggedness

Applications

- Switching applications

Description

These N-channel Power MOSFETs utilize STripFET™ F7 technology with an enhanced trench gate structure that results in very low on-resistance, while also reducing internal capacitance and gate charge for faster and more efficient switching.

Table 1: Device summary

Order code	Marking	Package	Packing
STH310N10F7-2	310N10F7	H ² PAK-2	Tape and reel
STH310N10F7-6		H ² PAK-6	

Contents

1	Electrical ratings	3
2	Electrical characteristics	4
	2.1 Electrical characteristics (curves).....	6
3	Test circuits	8
4	Package information	9
	4.1 H2PAK-2 package information	10
	4.2 H2PAK-6 package information	13
	4.3 Packing information.....	16
5	Revision history	18

1 Electrical ratings

Table 2: Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage	100	V
V_{GS}	Gate-source voltage	± 20	V
$I_D^{(1)}$	Drain current (continuous) at $T_C = 25\text{ }^\circ\text{C}$	180	A
	Drain current (continuous) at $T_C = 100\text{ }^\circ\text{C}$	180	A
$I_D^{(2)}$	Drain current (pulsed)	720	A
P_{TOT}	Total dissipation at $T_C = 25\text{ }^\circ\text{C}$	315	W
$E_{AS}^{(3)}$	Single pulse avalanche energy ($T_J = 25\text{ }^\circ\text{C}$ L = 0.55 mH, $I_{AS} = 65\text{ A}$)	1	J
T_J	Operating junction temperature	-55 to 175	$^\circ\text{C}$
T_{stg}	Storage temperature		$^\circ\text{C}$

Notes:

⁽¹⁾Current limited by package

⁽²⁾Pulse width limited by safe operating area

⁽³⁾Starting $T_J = 25\text{ }^\circ\text{C}$, $I_D = 60\text{ A}$, $V_{DD} = 50\text{ V}$

Table 3: Thermal data

Symbol	Parameter	Value	Unit
$R_{thj-case}$	Thermal resistance junction-case	0.48	$^\circ\text{C/W}$
$R_{thj-pcb}^{(1)}$	Thermal resistance junction-pcb	35	$^\circ\text{C/W}$

Notes:

⁽¹⁾When mounted on FR-4 board of 1 inch², 2 oz Cu

2 Electrical characteristics

(T_{CASE} = 25 °C unless otherwise specified)

Table 4: On/off-state

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V _{(BR)DSS}	Drain-source breakdown voltage (V _{GS} = 0)	I _D = 250 μA	100			V
I _{DSS}	Zero gate voltage drain current (V _{GS} = 0)	V _{DS} = 100 V			1	μA
		V _{DS} = 100 V; T _C = 125 °C			100	μA
I _{GSS}	Gate body leakage current (V _{DS} = 0)	V _{GS} = 20 V			100	nA
V _{GS(th)}	Gate threshold voltage	V _{DS} = V _{GS} , I _D = 250 μA	2.5	3.5	4.5	V
R _{DS(on)}	Static drain-source on-resistance	V _{GS} = 10 V, I _D = 60 A		1.9	2.3	mΩ

Table 5: Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C _{iss}	Input capacitance	V _{DS} = 25 V, f = 1 MHz, V _{GS} = 0	-	12800	-	pF
C _{oss}	Output capacitance			3500		pF
C _{rss}	Reverse transfer capacitance			170		pF
Q _g	Total gate charge	V _{DD} = 50 V, I _D = 180 A		180		nC
Q _{gs}	Gate-source charge	V _{GS} = 10 V		78		nC
Q _{gd}	Gate-drain charge	See Figure 14: "Gate charge test circuit"		34		nC

Table 6: Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
t _{d(on)}	Turn-on delay time	V _{DD} = 50 V, I _D = 90 A, R _G = 4.7 Ω, V _{GS} = 10 V See Figure 13: "Switching times test circuit for resistive load"	-	62	-	ns
t _r	Rise time			108		ns
t _{d(off)}	Turn-off delay time			148		ns
t _f	Fall time			40		ns

Table 7: Source-drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I _{SD}	Source-drain current		-		180	A
I _{SDM} ⁽¹⁾	Source-drain current (pulsed)				720	A
V _{SD} ⁽²⁾	Forward on voltage	I _{SD} = 60 A, V _{GS} = 0			1.5	V
t _{rr}	Reverse recovery time	I _{SD} = 180 A, di/dt = 100 A/μs, V _{DD} = 80 V, T _J = 150 °C		85		ns
Q _{rr}	Reverse recovery charge			200		nC
I _{RRM}	Reverse recovery current			4.7		A

Notes:

⁽¹⁾Pulse width limited by safe operating area

⁽²⁾Pulsed: pulse duration = 300 μs , duty cycle 1.5%

2.1 Electrical characteristics (curves)

Figure 2: Safe operating area

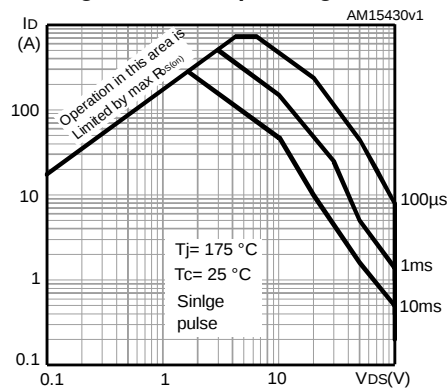


Figure 3: Thermal impedance

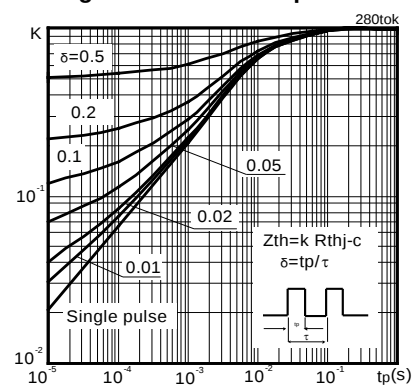


Figure 4: Output characteristics

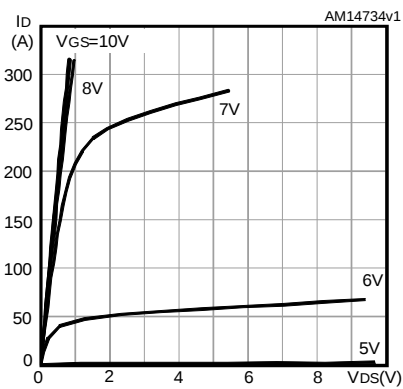


Figure 5: Transfer characteristics

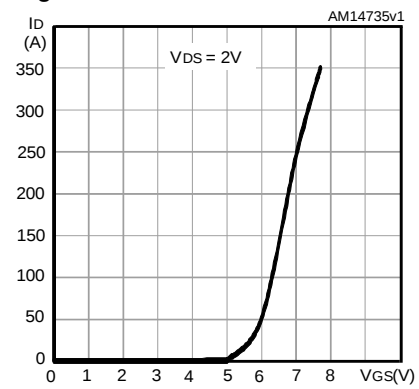


Figure 6: Gate charge vs gate-source voltage

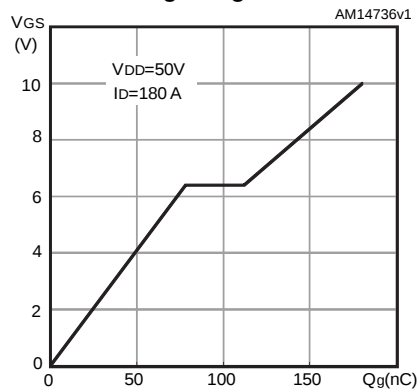


Figure 7: Static drain-source on-resistance

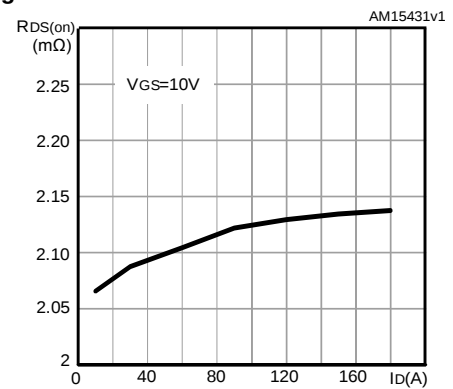


Figure 8: Normalized $V_{(BR)DSS}$ vs temperature

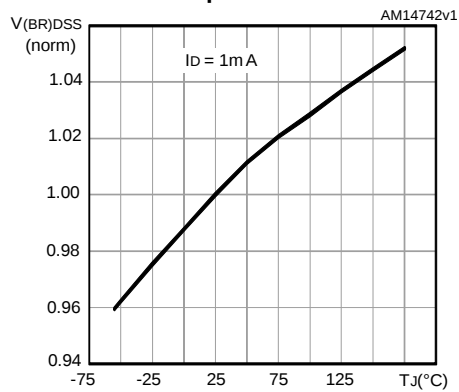


Figure 9: Capacitance variations

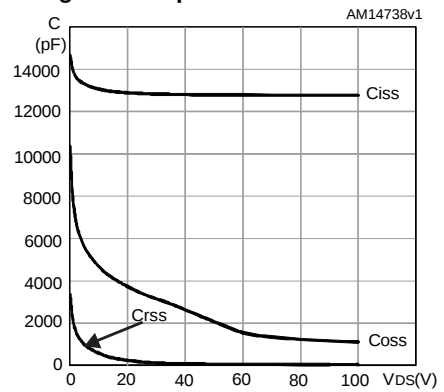


Figure 10: Source-drain diode forward characteristics

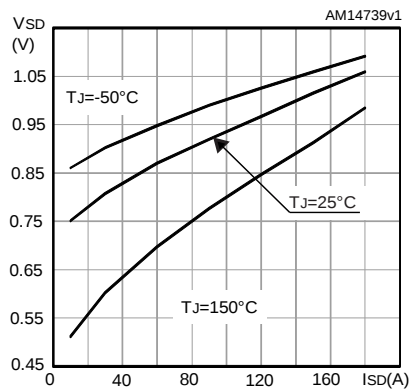


Figure 11: Normalized gate threshold voltage vs temperature

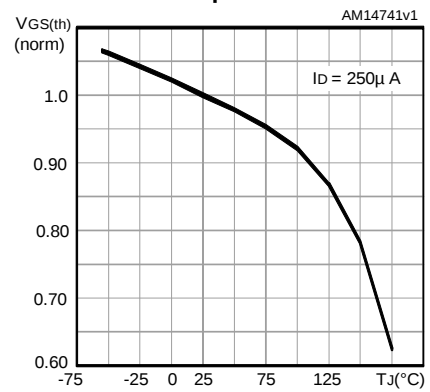
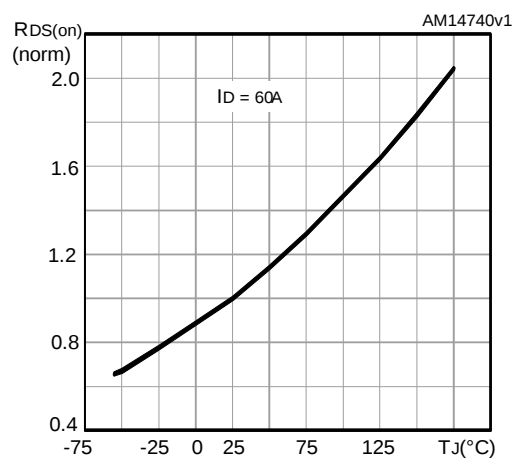
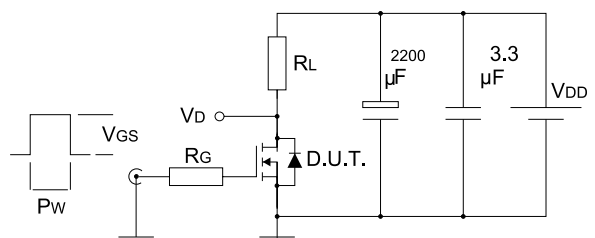


Figure 12: Normalized on-resistance vs temperature



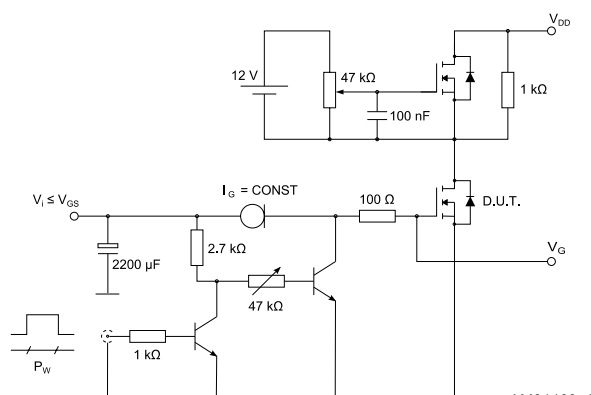
3 Test circuits

Figure 13: Switching times test circuit for resistive load



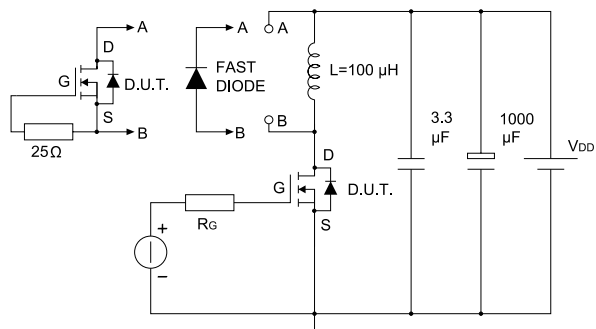
AM01468v1

Figure 14: Gate charge test circuit



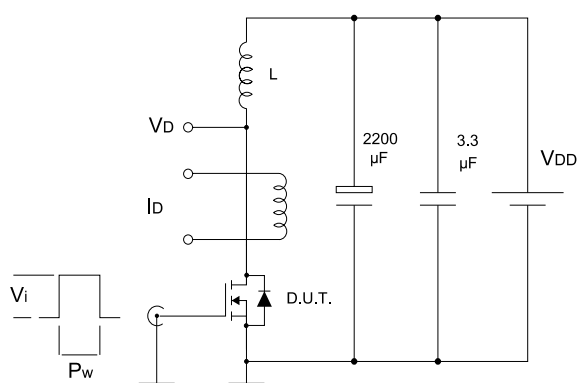
AM01469v1

Figure 15: Test circuit for inductive load switching and diode recovery times



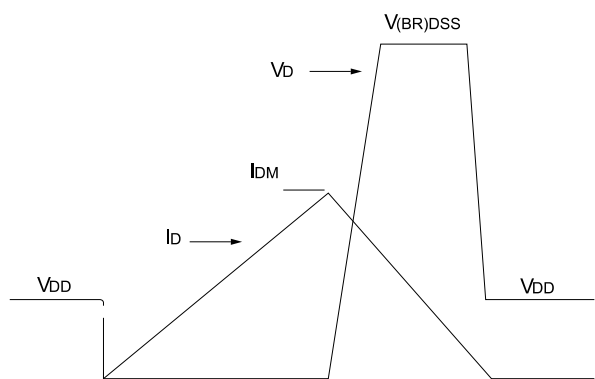
AM01470v1

Figure 16: Unclamped inductive load test circuit



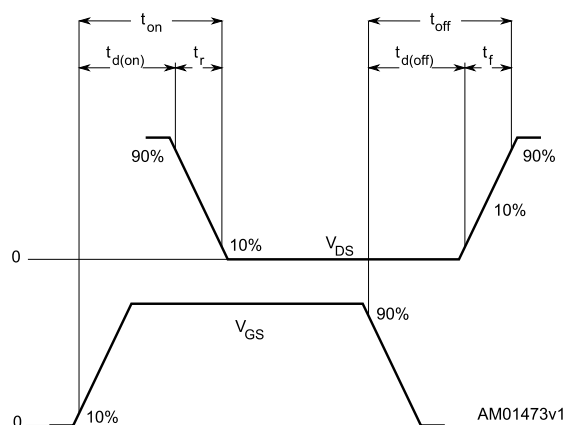
AM01471v1

Figure 17: Unclamped inductive waveform



AM01472v1

Figure 18: Switching time waveform



AM01473v1

4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: **www.st.com**. ECOPACK® is an ST trademark.

4.1 H2PAK-2 package information

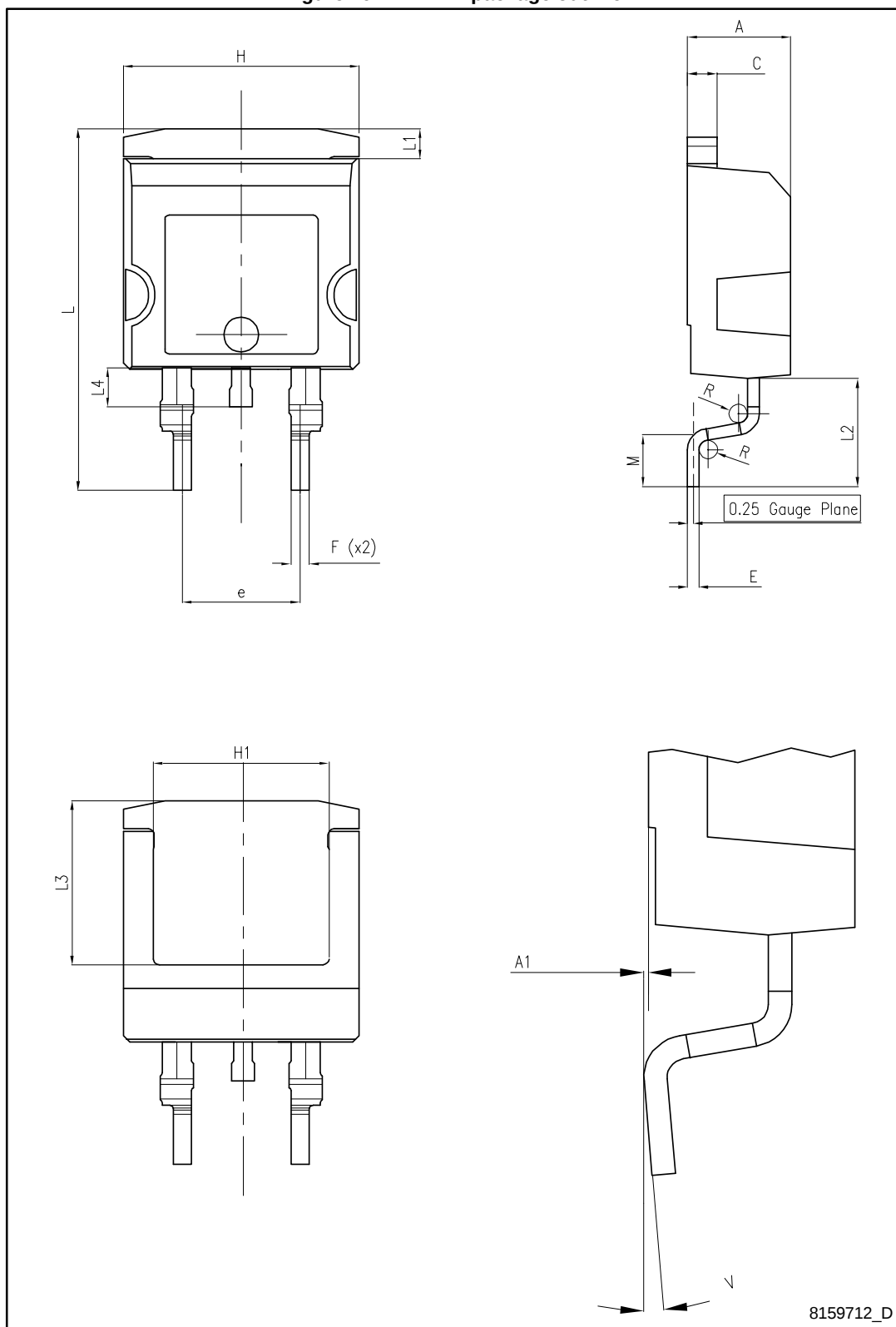
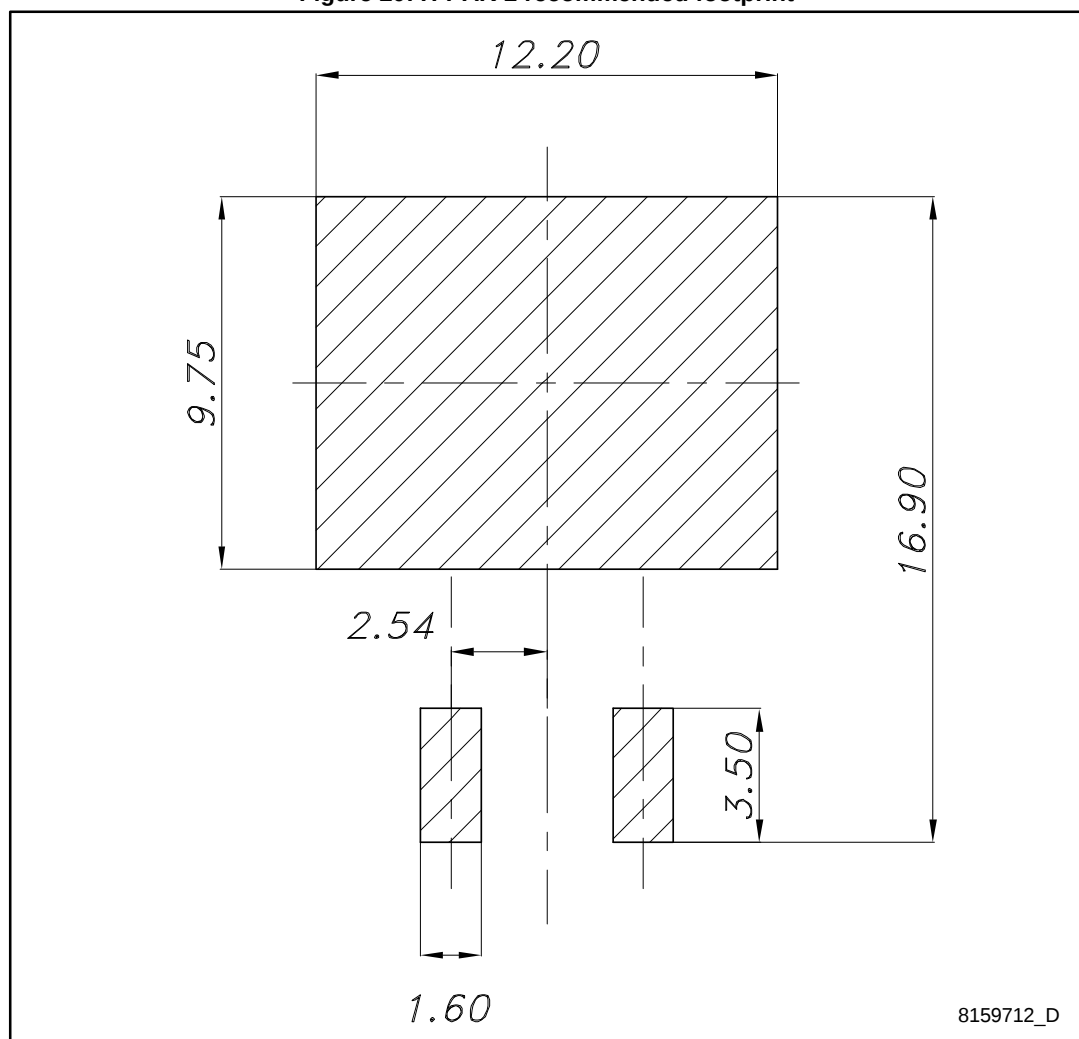
Figure 19: H²PAK-2 package outline

Table 8: H²PAK-2 package mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.30	-	4.80
A1	0.03		0.20
C	1.17		1.37
e	4.98		5.18
E	0.50		0.90
F	0.78		0.85
H	10.00		10.40
H1	7.40		7.80
L	15.30		15.80
L1	1.27		1.40
L2	4.93		5.23
L3	6.85		7.25
L4	1.5		1.7
M	2.6		2.9
R	0.20		0.60
V	0°		8°

Figure 20: H²PAK-2 recommended footprint

4.2 H2PAK-6 package information

Figure 21: H²PAK-6 package outline

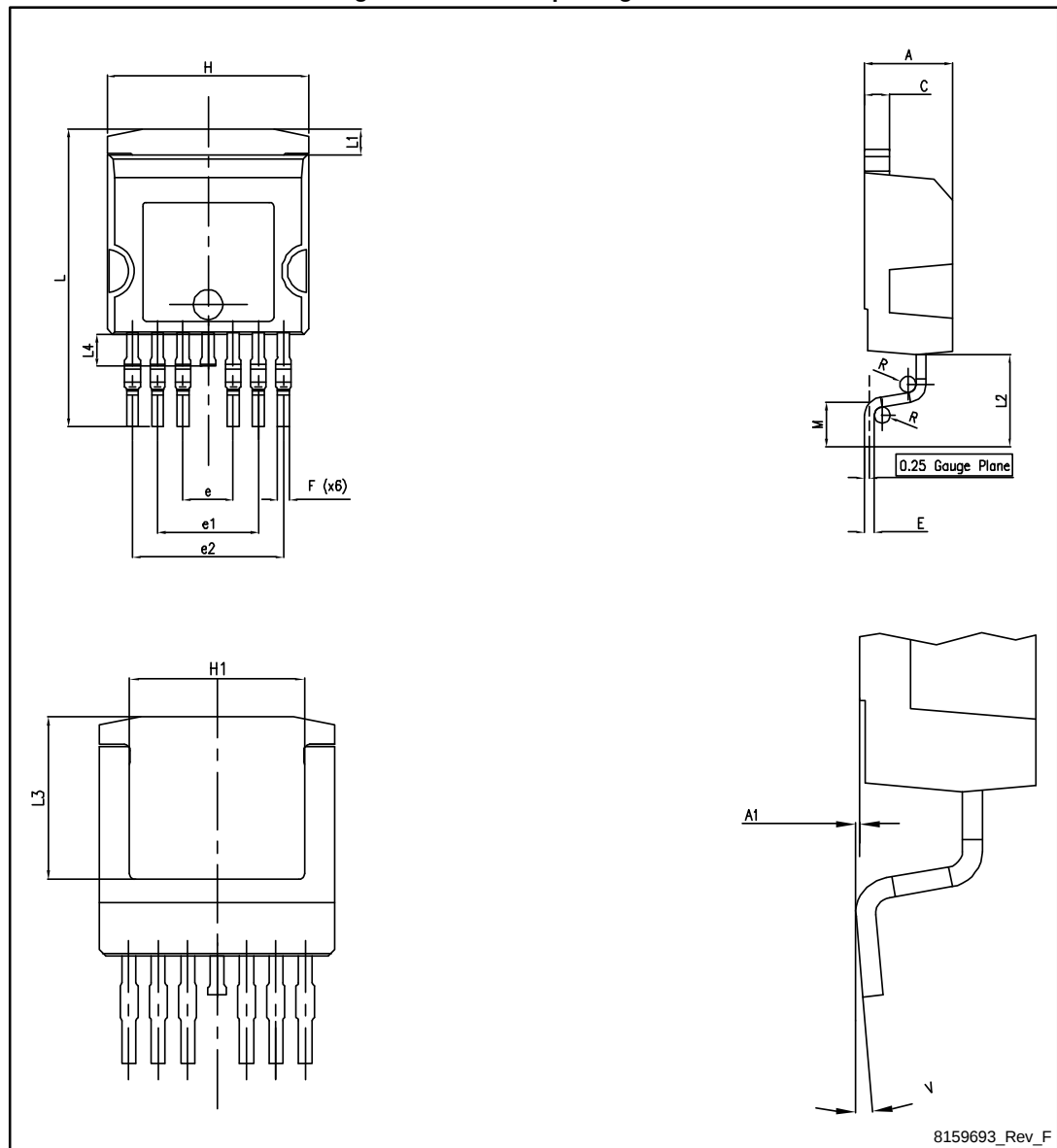
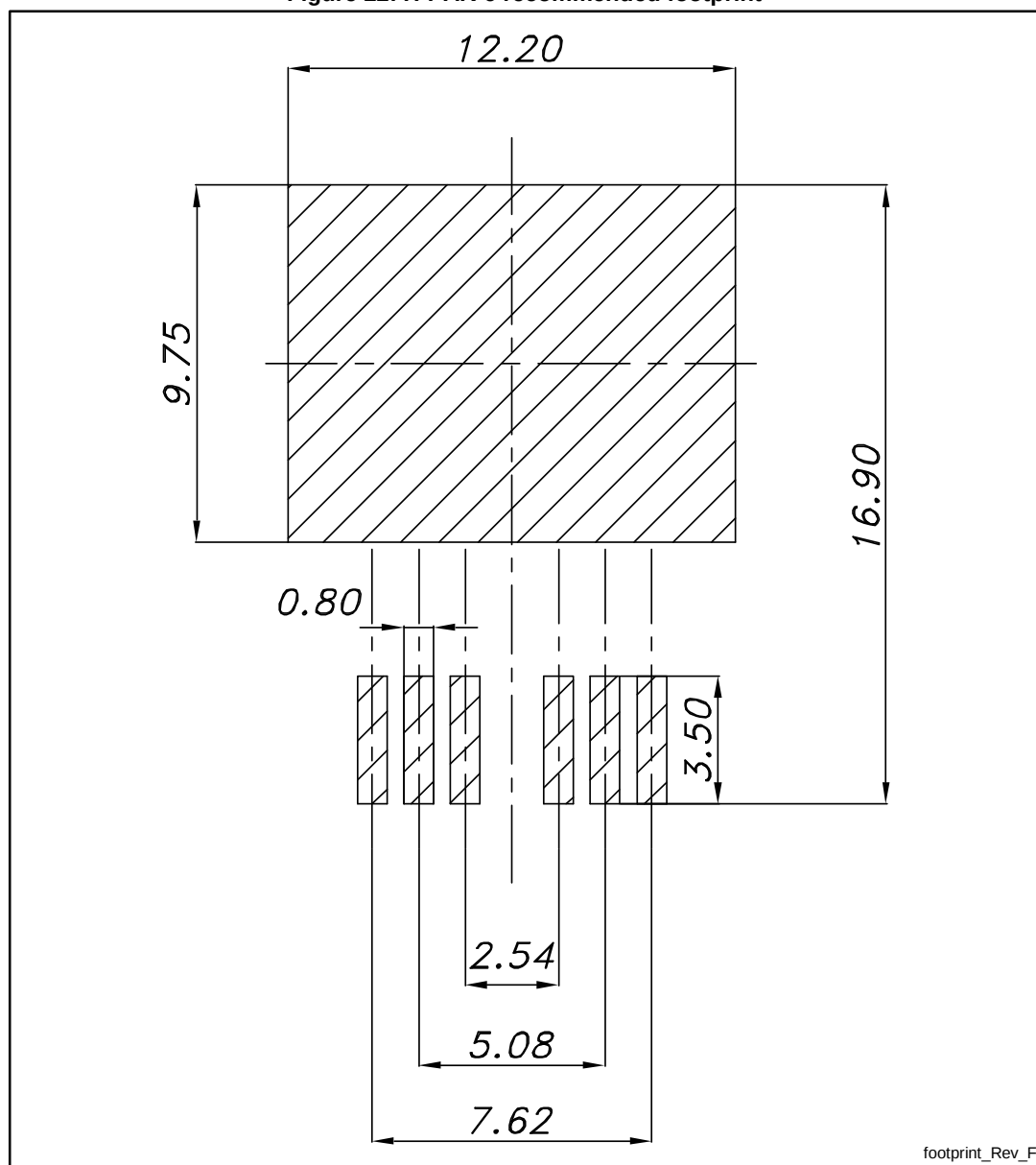


Table 9: H²PAK-6 package mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.30	-	4.80
A1	0.03		0.20
C	1.17		1.37
e	2.34		2.74
e1	4.88		5.28
e2	7.42		7.82
E	0.45		0.60
F	0.50		0.70
H	10.00		10.40
H1	7.40		7.80
L	14.75		15.25
L1	1.27		1.40
L2	4.35		4.95
L3	6.85		7.25
L4	1.5		1.75
M	1.90		2.50
R	0.20		0.60
V	0°		8°

Figure 22: H²PAK-6 recommended footprint



Dimensions are in mm.

4.3 Packing information

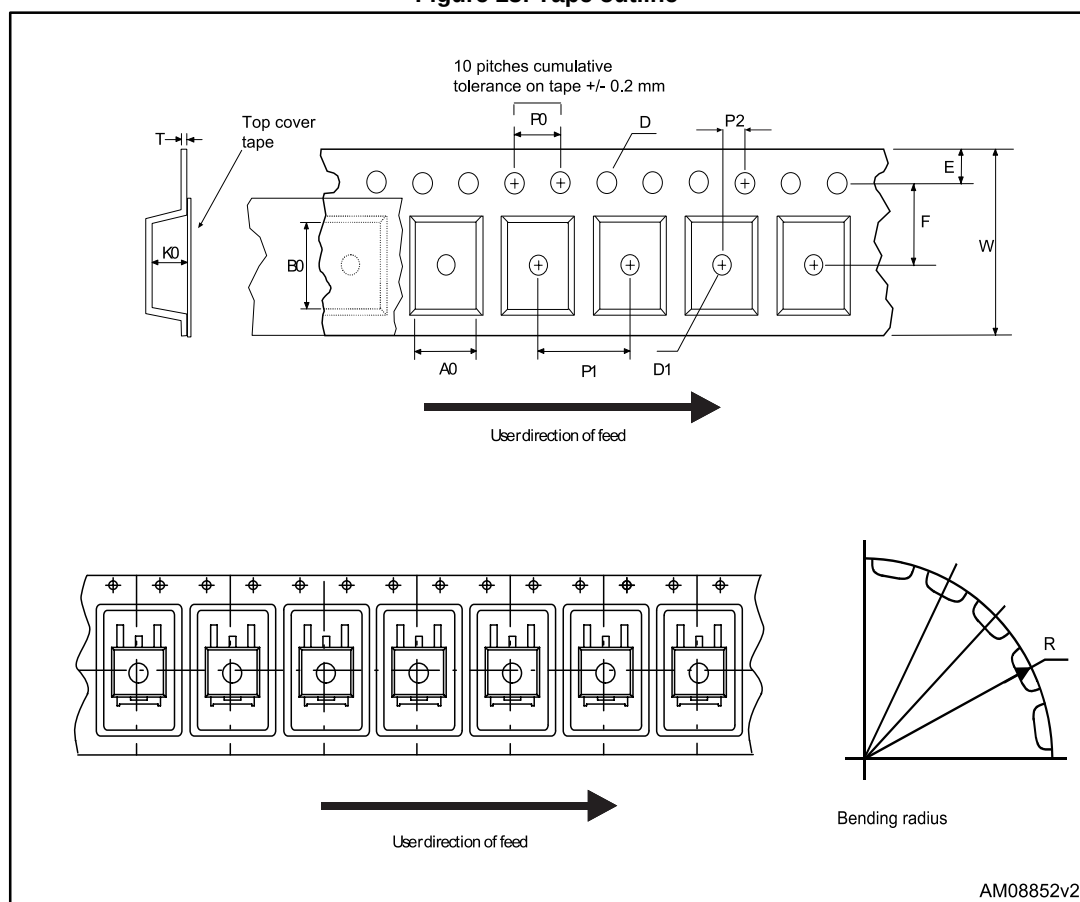
Figure 23: Tape outline

Figure 24: Reel outline

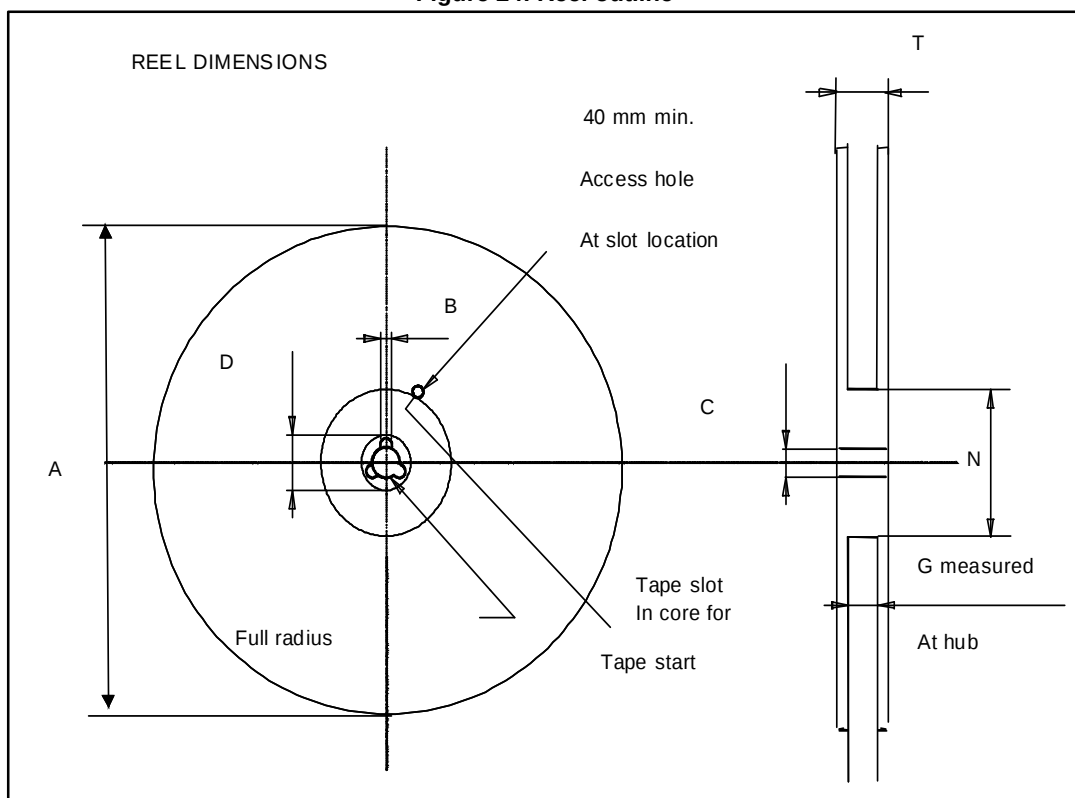


Table 10: Tape and reel mechanical data

Tape			Reel		
Dim.	mm		Dim.	mm	
	Min.	Max.		Min.	Max.
A0	10.5	10.7	A		330
B0	15.7	15.9	B	1.5	
D	1.5	1.6	C	12.8	13.2
D1	1.59	1.61	D	20.2	
E	1.65	1.85	G	24.4	26.4
F	11.4	11.6	N	100	
K0	4.8	5.0	T		30.4
P0	3.9	4.1			
P1	11.9	12.1	Base quantity		1000
P2	1.9	2.1	Bulk quantity		1000
R	50				
T	0.25	0.35			
W	23.7	24.3			

5 Revision history

Table 11: Document revision history

Date	Revision	Changes
10-Dec-2012	1	Initial release. Part number(s) previously included in datasheet ID02287
23-Jul-2013	2	• Document status promoted from preliminary to production data • Modified: I_{DSS} and V_{GS} value in table 4 • Added: E_{AS} value in table 2 • Minor text changes
27-Nov-2014	3	• Updated: H²PAK-6 package information. • Updated the title, features and description. • Minor text changes.
29-Jul-2015	4	Updated Table 2: "Absolute maximum ratings" .

IMPORTANT NOTICE – PLEASE READ CAREFULLY

STMicroelectronics NV and its subsidiaries ("ST") reserve the right to make changes, corrections, enhancements, modifications, and improvements to ST products and/or to this document at any time without notice. Purchasers should obtain the latest relevant information on ST products before placing orders. ST products are sold pursuant to ST's terms and conditions of sale in place at the time of order acknowledgement.

Purchasers are solely responsible for the choice, selection, and use of ST products and ST assumes no liability for application assistance or the design of Purchasers' products.

No license, express or implied, to any intellectual property right is granted by ST herein.

Resale of ST products with provisions different from the information set forth herein shall void any warranty granted by ST for such product.

ST and the ST logo are trademarks of ST. All other product or service names are the property of their respective owners.

Information in this document supersedes and replaces information previously supplied in any prior versions of this document.

© 2015 STMicroelectronics – All rights reserved