

260-745

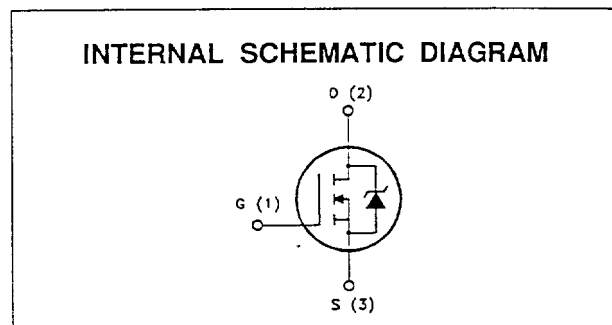
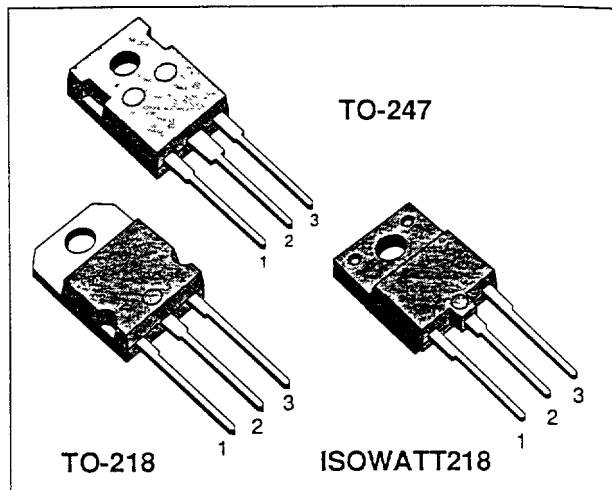
**N - CHANNEL ENHANCEMENT MODE
POWER MOS TRANSISTOR**

TYPE	V _{DSS}	R _{DS(on)}	I _D
STH33N20	200 V	< 0.085 Ω	33 A
STH33N20FI	200 V	< 0.085 Ω	20 A
STW33N20	200 V	< 0.085 Ω	33 A

- TYPICAL R_{DS(on)} = 0.073 Ω
- AVALANCHE RUGGED TECHNOLOGY
- 100% AVALANCHE TESTED
- REPETITIVE AVALANCHE DATA AT 100°C
- APPLICATION ORIENTED CHARACTERIZATION

APPLICATIONS

- HIGH CURRENT, HIGH SPEED SWITCHING
- UNINTERRUPTIBLE POWER SUPPLY (UPS)
- MOTOR CONTROL, AUDIO AMPLIFIERS
- INDUSTRIAL ACTUATORS
- DC-DC & DC-AC CONVERTERS FOR TELECOM, INDUSTRIAL AND CONSUMER ENVIRONMENT



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value		Unit
		STH/STW33N20	STH33N20FI	
V _{DS}	Drain-source Voltage (V _{GS} = 0)	200		V
V _{DGR}	Drain- gate Voltage (R _{GS} = 20 kΩ)	200		V
V _{GS}	Gate-source Voltage	± 20		V
I _D	Drain Current (continuous) at T _c = 25 °C	33	20	A
I _D	Drain Current (continuous) at T _c = 100 °C	20	12	A
I _{DM} (*)	Drain Current (pulsed)	132	132	A
P _{tot}	Total Dissipation at T _c = 25 °C	180	70	W
	Derating Factor	1.44	0.56	W/°C
V _{ISO}	Insulation Withstand Voltage (DC)	—	4000	V
T _{stg}	Storage Temperature	-65 to 150		°C
T _J	Max. Operating Junction Temperature	150		°C

(*) Pulse width limited by safe operating area

STH33N20/FI - STW33N20

THERMAL DATA

			TO-218/TO-247	ISOWATT218	
$R_{thj-case}$	Thermal Resistance Junction-case	Max	0.69	1.79	°C/W
$R_{thj-amb}$	Thermal Resistance Junction-ambient	Max	30		°C/W
$R_{thc-sink}$	Thermal Resistance Case-sink	Typ	0.1		°C/W
T_l	Maximum Lead Temperature For Soldering Purpose		300		°C

AVALANCHE CHARACTERISTICS

Symbol	Parameter	Max Value	Unit
I_{AR}	Avalanche Current, Repetitive or Not-Repetitive (pulse width limited by T_j max, $\delta < 1\%$)	33	A
E_{AS}	Single Pulse Avalanche Energy (starting $T_j = 25\text{ }^\circ\text{C}$, $I_D = I_{AR}$, $V_{DD} = 50\text{ V}$)	150	mJ
E_{AR}	Repetitive Avalanche Energy (pulse width limited by T_j max, $\delta < 1\%$)	40	mJ
I_{AR}	Avalanche Current, Repetitive or Not-Repetitive ($T_c = 100\text{ }^\circ\text{C}$, pulse width limited by T_j max, $\delta < 1\%$)	20	A

ELECTRICAL CHARACTERISTICS ($T_{case} = 25\text{ }^\circ\text{C}$ unless otherwise specified)

OFF

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source Breakdown Voltage	$I_D = 250\text{ }\mu\text{A}$ $V_{GS} = 0$	200			V
I_{DSS}	Zero Gate Voltage Drain Current ($V_{GS} = 0$)	$V_{DS} = \text{Max Rating}$ $V_{DS} = \text{Max Rating} \times 0.8$ $T_c = 125\text{ }^\circ\text{C}$			250 1000	μA μA
I_{GSS}	Gate-body Leakage Current ($V_{DS} = 0$)	$V_{GS} = \pm 20\text{ V}$			± 100	nA

ON (*)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}$ $I_D = 250\text{ }\mu\text{A}$	2	3	4	V
$R_{DS(on)}$	Static Drain-source On Resistance	$V_{GS} = 10\text{ V}$ $I_D = 16\text{ A}$ $V_{GS} = 10\text{ V}$ $I_D = 16\text{ A}$ $T_c = 100\text{ }^\circ\text{C}$		0.073	0.085 0.170	Ω Ω
$I_{D(on)}$	On State Drain Current	$V_{DS} > I_{D(on)} \times R_{DS(on)max}$ $V_{GS} = 10\text{ V}$	33			A

DYNAMIC

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
g_{fs} (*)	Forward Transconductance	$V_{DS} > I_{D(on)} \times R_{DS(on)max}$ $I_D = 16\text{ A}$	10	22		S
C_{iss}	Input Capacitance	$V_{DS} = 25\text{ V}$ $f = 1\text{ MHz}$ $V_{GS} = 0$		2800	3600	pF
C_{oss}	Output Capacitance			600	800	pF
C_{rss}	Reverse Transfer Capacitance			190	250	pF

ELECTRICAL CHARACTERISTICS (continued)

SWITCHING ON

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on Time	$V_{DD} = 95\text{ V}$ $I_D = 16\text{ A}$		25	40	ns
t_r	Rise Time	$R_G = 4.7\ \Omega$ $V_{GS} = 10\text{ V}$ (see test circuit, figure 3)		65	95	ns
$(di/dt)_{on}$	Turn-on Current Slope	$V_{DD} = 160\text{ V}$ $I_D = 33\text{ A}$ $R_G = 50\ \Omega$ $V_{GS} = 10\text{ V}$ (see test circuit, figure 5)		200		A/ μs
Q_g	Total Gate Charge	$V_{DD} = 160\text{ V}$ $I_D = 33\text{ A}$ $V_{GS} = 10\text{ V}$		125	180	nC
Q_{gs}	Gate-Source Charge			15		nC
Q_{gd}	Gate-Drain Charge			62		nC

SWITCHING OFF

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{r(Voff)}$	Off-voltage Rise Time	$V_{DD} = 160\text{ V}$ $I_D = 33\text{ A}$		180	250	ns
t_f	Fall Time	$R_G = 50\ \Omega$ $V_{GS} = 10\text{ V}$ (see test circuit, figure 5)		105	150	ns
t_c	Cross-over Time			285	400	ns

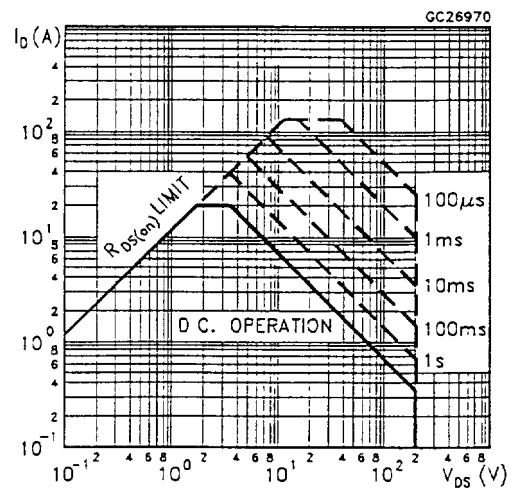
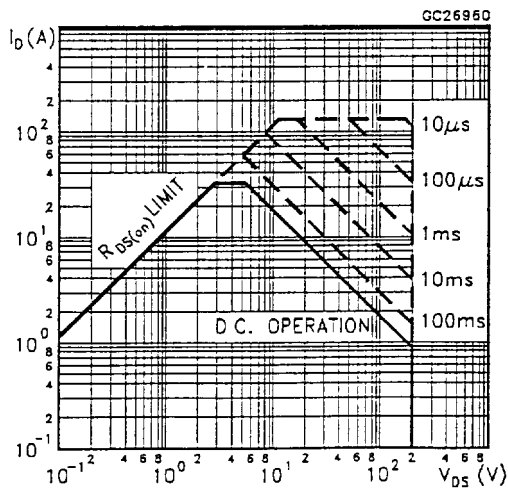
SOURCE DRAIN DIODE

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain Current				33	A
$I_{SDM}(\bullet)$	Source-drain Current (pulsed)				132	A
$V_{SD}(\ast)$	Forward On Voltage	$I_{SD} = 33\text{ A}$ $V_{GS} = 0$			1.6	V
t_{rr}	Reverse Recovery Time	$I_{SD} = 33\text{ A}$ $di/dt = 100\text{ A}/\mu\text{s}$ $V_{DD} = 30\text{ V}$ $T_J = 150\text{ }^\circ\text{C}$ (see test circuit, figure 5)		450		ns
Q_{rr}	Reverse Recovery Charge			5		μC
I_{RRM}	Reverse Recovery Current			22		A

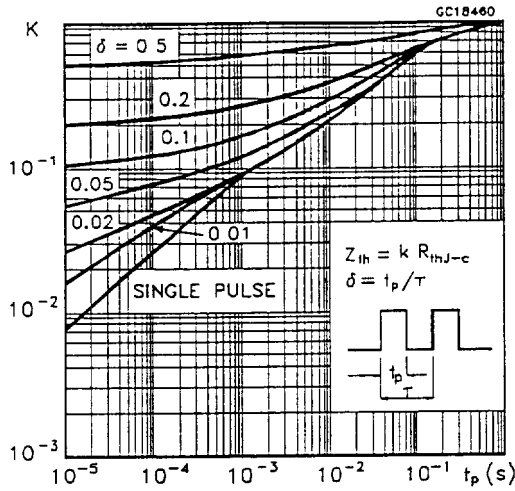
(\ast) Pulsed Pulse duration = 300 μs , duty cycle 1.5 %
 (\bullet) Pulse width limited by safe operating area

Safe Operating Areas For TO-218 and TO-247

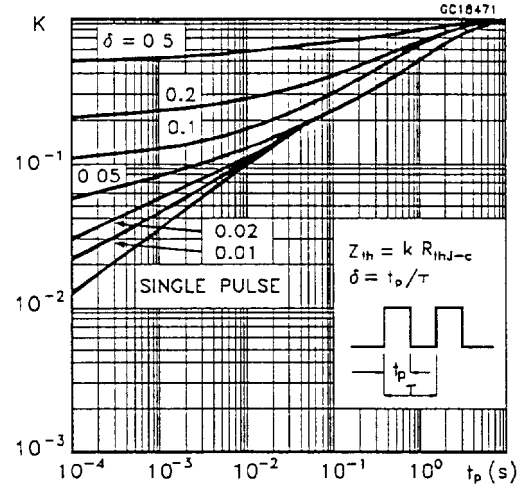
Safe Operating Areas For ISOWATT218



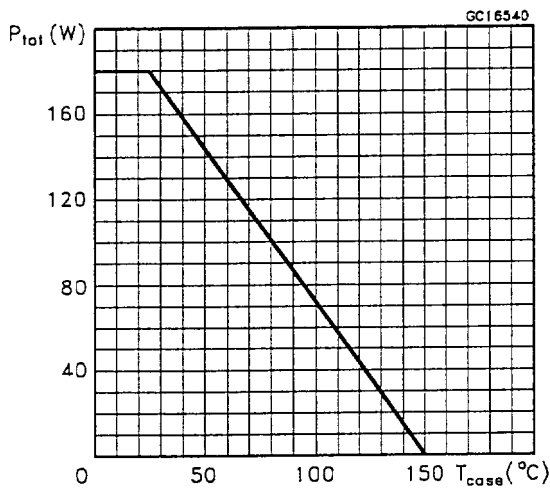
Thermal Impedance For TO-218 and TO-247



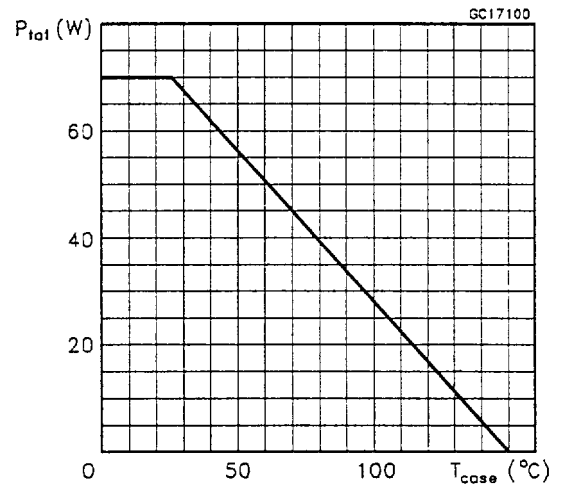
Thermal Impedance For ISOWATT218



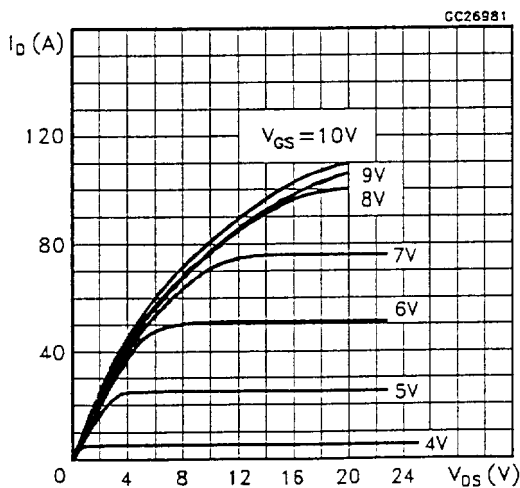
Derating Curve For TO-218 and TO-247



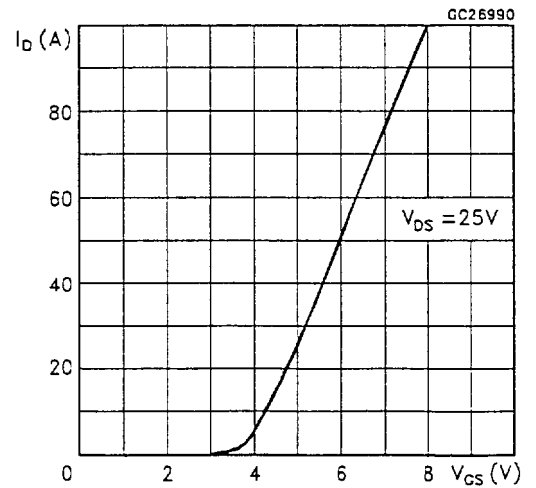
Derating Curve For ISOWATT218



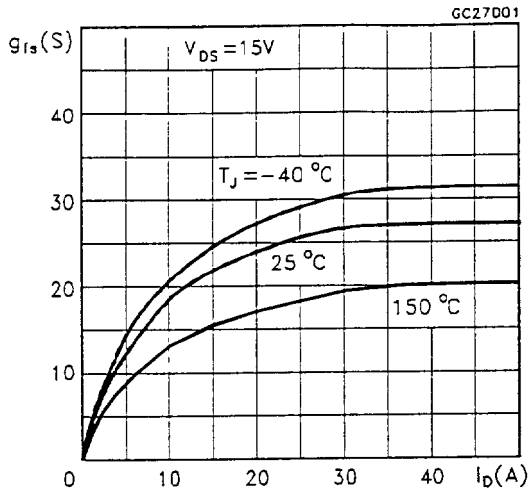
Output Characteristics



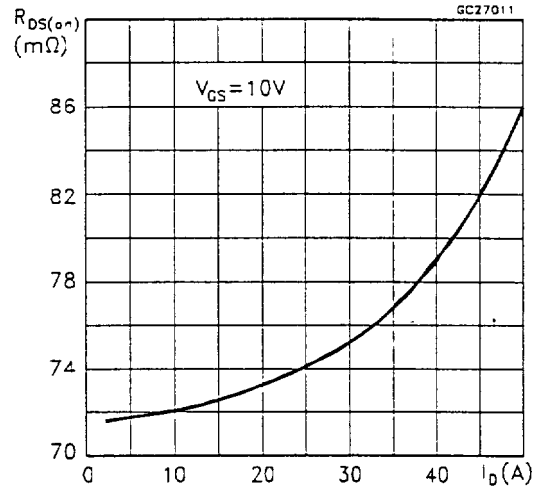
Transfer Characteristics



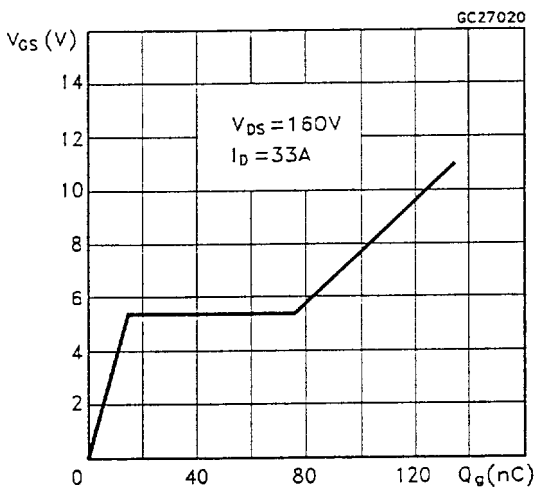
Transconductance



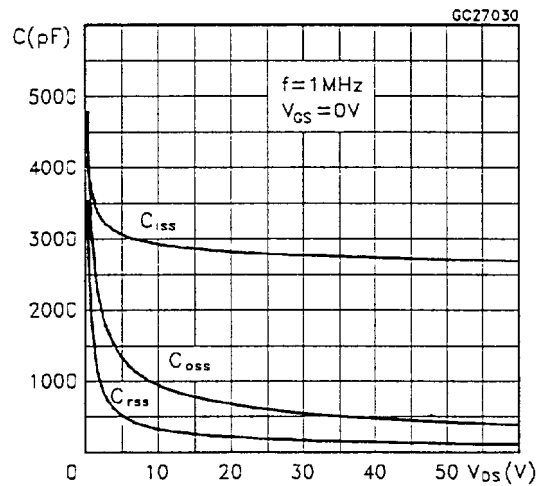
Static Drain-source On Resistance



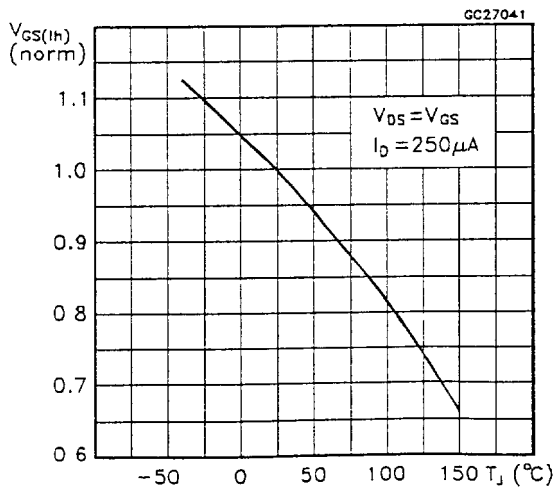
Gate Charge vs Gate-source Voltage



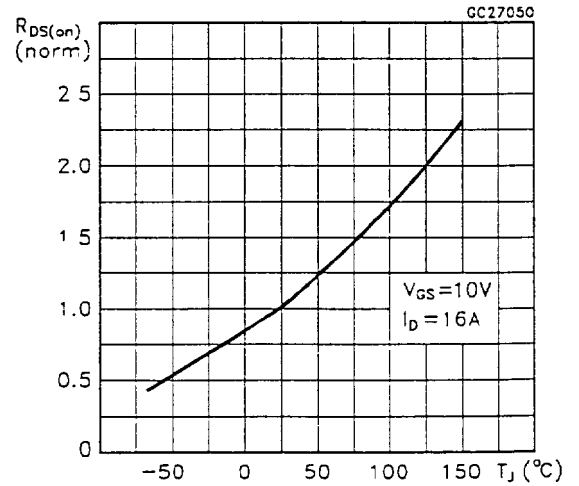
Capacitance Variations



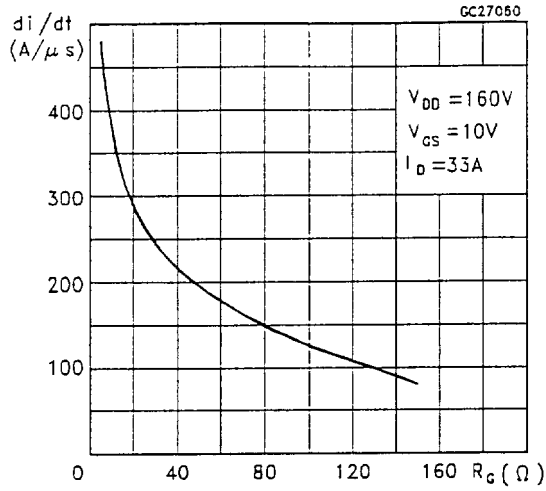
Normalized Gate Threshold Voltage vs Temperature



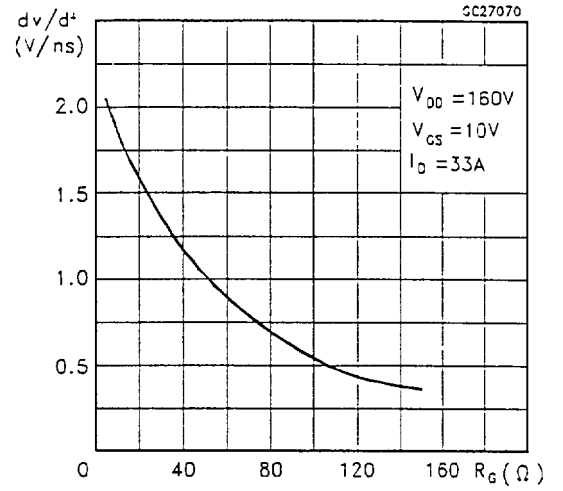
Normalized On Resistance vs Temperature



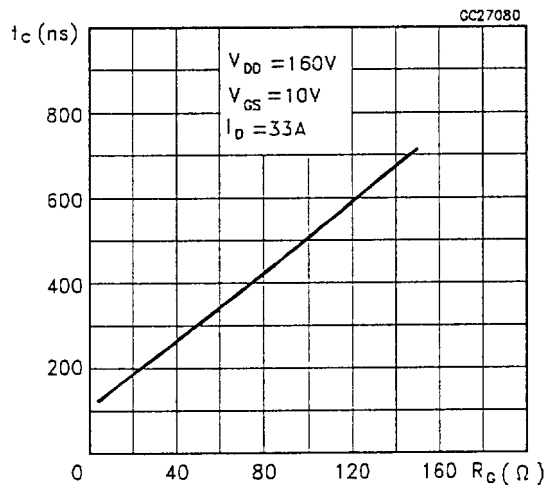
Turn-on Current Slope



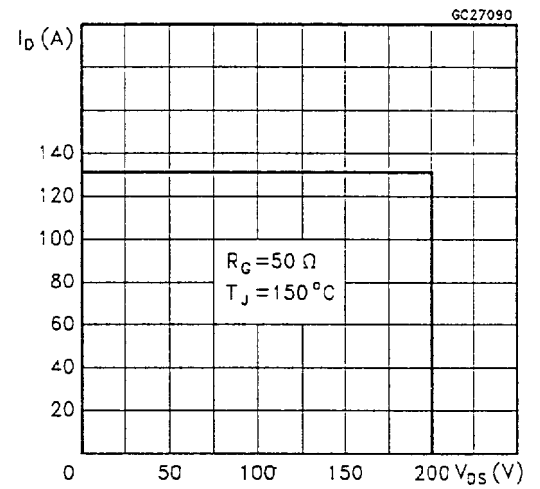
Turn-off Drain-source Voltage Slope



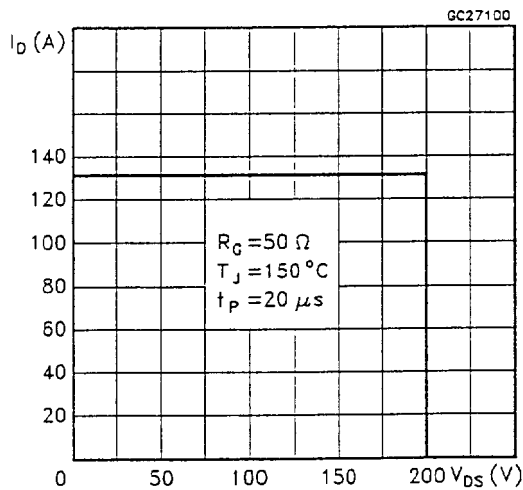
Cross-over Time



Switching Safe Operating Area



Accidental Overload Area



Source-drain Diode Forward Characteristics

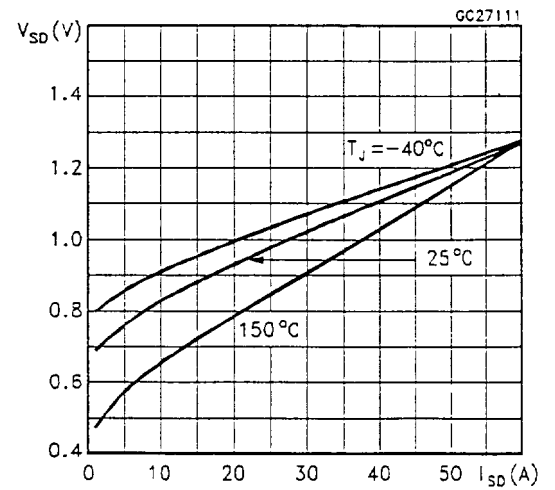


Fig. 1: Unclamped Inductive Load Test Circuits

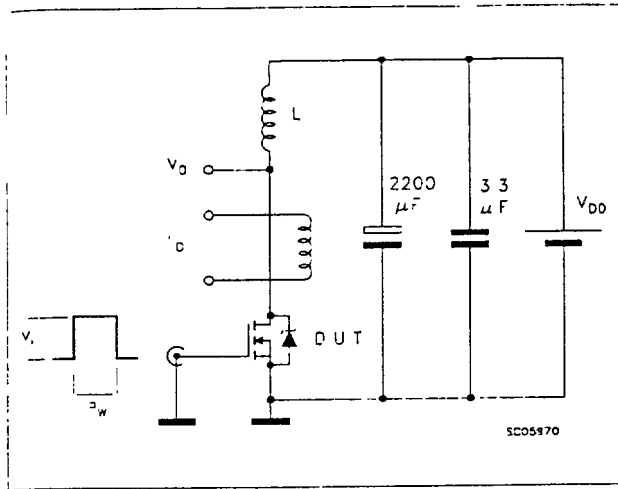


Fig. 2: Unclamped Inductive Waveforms

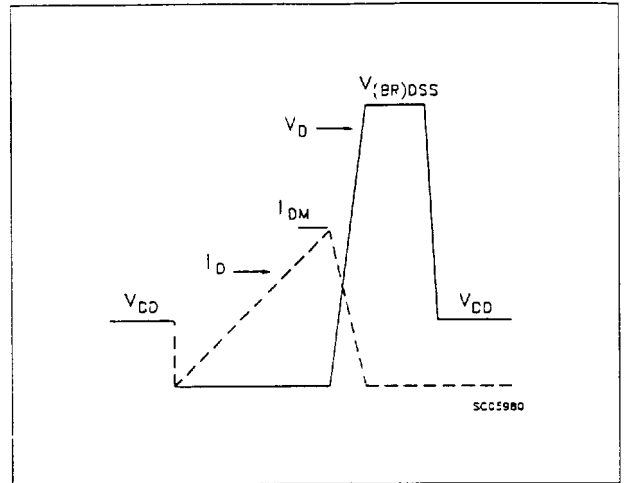


Fig. 3: Switching Times Test Circuits For Resistive Load

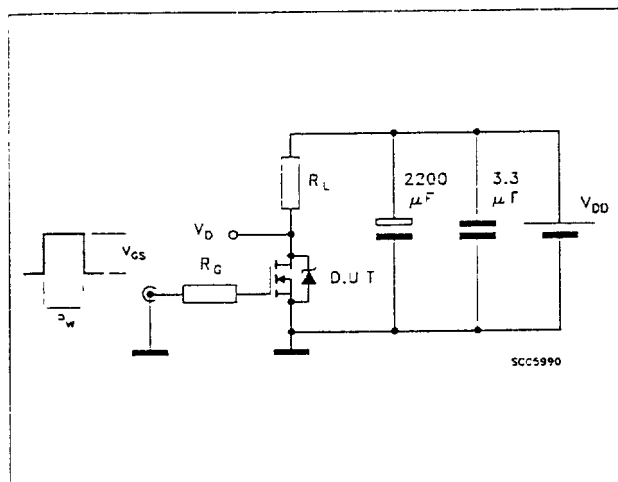


Fig. 4: Gate Charge Test Circuit

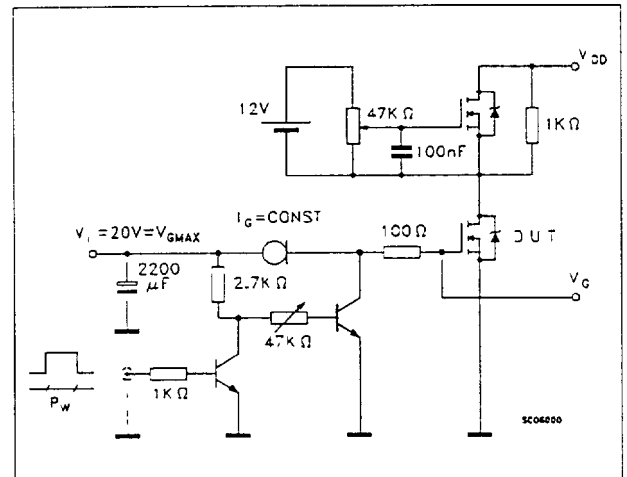


Fig. 5: Test Circuit For Inductive Load Switching And Diode Reverse Recovery Time

