Automotive-grade N-channel 600 V, 0.084 Ω typ., 29 A MDmesh™ DM6 Power MOSFET in an H²PAK-7 package
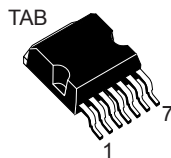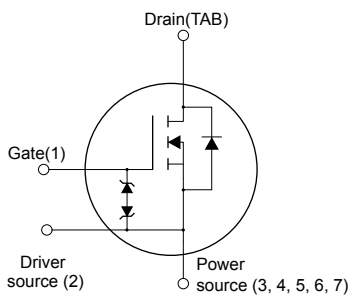

TAB

7

1

H²PAK-7

Order code	V_{DS}	$R_{DS(on)}$ max.	I_D
STH36N60DM6-7AG	600 V	0.099 Ω	29 A

- AEC-Q101 qualified
- Fast-recovery body diode
- Lower $R_{DS(on)}$ x area vs previous generation
- Low gate charge, input capacitance and resistance
- 100% avalanche tested
- Extremely dv/dt ruggedness
- Zener-protected
- Tab-leads creepage distance 4.5 mm typ.
- Excellent switching performance thanks to the extra driving source pin

Drain(TAB)

Gate(1)

Driver
source (2)

Power
source (3, 4, 5, 6, 7)

N-chG1DS2PS34567DTABZ

Applications

- Switching applications

Description

This high-voltage N-channel Power MOSFET is part of the MDmesh™ DM6 fast-recovery diode series. Compared with the previous MDmesh fast generation, DM6 combines very low recovery charge (Q_{rr}), recovery time (t_{rr}) and excellent improvement in $R_{DS(on)}$ per area with one of the most effective switching behaviors available in the market for the most demanding high-efficiency bridge topologies and ZVS phase-shift converters.

Product status link
STH36N60DM6-7AG

Product summary	
Order code	STH36N60DM6-7AG
Marking	36N60DM6
Package	H²PAK-7
Packing	Tape and reel

Prerelease product(s)

DS11713 - **Rev 3** - September 2018
For further information contact your local STMicroelectronics sales office.

www.st.com

1 Electrical ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{GS}	Gate-source voltage	±25	V
I_D	Drain current (continuous) at T_C = 25 °C	29	A
I_D	Drain current (continuous) at T_C = 100 °C	18	A
I_D [1]	Drain current (pulsed)	103	A
P_{TOT}	Total dissipation at T_C = 25 °C	210	W
dv/dt[2]	Peak diode recovery voltage slope	50	V/ns
dv/dt[3]	MOSFET dv/dt ruggedness	100	
T_J	Operating junction temperature range	-55 to 150	°C
T_{stg}	Storage temperature range		

1. Pulse width limited by safe operating area.

2. $I_{SD} \leq 29$ A, di/dt ≤ 800 A/µs; $V_{DS\ peak} < V_{(BR)DSS}$, V_{DD} = 480 V

3. $V_{DS} \leq 480$ V

Table 2. Thermal data

Symbol	Parameter	Value	Unit
$R_{thj-case}$	Thermal resistance junction-case	0.6	°C/W
$R_{thj-pcb}$	Thermal resistance junction-pcb[1]	30	

1. When mounted on 1 inch² FR-4, 2 Oz copper board.

Table 3. Avalanche characteristics

Symbol	Parameter	Value	Unit
I_{AR}	Avalanche current, repetitive or not repetitive (pulse width limited by T_{jmax})	6	A
E_{AS}	Single pulse avalanche energy (starting T_j = 25 °C, I_D = I_{AR}, V_{DD} = 100 V)	630	mJ

2 Electrical characteristics

T_C = 25 °C unless otherwise specified.

Table 4. On/off-state

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V, I_D = 1 mA	600			V
I_{DSS}	Zero gate voltage drain current	V_{GS} = 0 V, V_{DS} = 600 V			5	µA
		V_{GS} = 0 V, V_{DS} = 600 V; T_C = 125 °C[1]			100	µA
I_{GSS}	Gate body leakage current	V_{DS} = 0 V, V_{GS} = ±25 V			±5	µA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 250 µA	3	4	5	V
$R_{DS(on)}$	Static drain-source on-resistance	V_{GS} = 10 V, I_D = 14.5 A		0.084	0.099	Ω

1. Defined by design, not subject to production test.

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	V_{DS} = 100 V, f = 1 MHz, V_{GS} = 0 V	-	1960	-	pF
C_{oss}	Output capacitance		-	140	-	pF
C_{rss}	Reverse transfer capacitance		-	2	-	pF
$C_{oss\ eq.}$ [1]	Equivalent output capacitance	V_{DS} = 0 to 480 V, V_{GS} = 0 V	-	335	-	pF
R_G	Intrinsic gate resistance	f = 1 MHz open drain	-	1.5	-	Ω
Q_g	Total gate charge	V_{DD} = 480 V, I_D = 29 A, V_{GS}= 0 to 10 V, (see Figure 13. Test circuit for gate charge behavior)	-	46	-	nC
Q_{gs}	Gate-source charge		-	13	-	nC
Q_{gd}	Gate-drain charge		-	22	-	nC

1. $C_{oss\ eq.}$ is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}.

Table 6. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	V_{DD}= 300 V, I_D = 14.5 A, R_G = 4.7 Ω, V_{GS} = 10 V (See Figure 12. Test circuit for resistive load switching times and Figure 17. Switching time waveform)	-	16	-	ns
t_r	Rise time		-	5.3	-	ns
$t_{d(off)}$	Turn-off delay time		-	50	-	ns
t_f	Fall time		-	7	-	ns

Table 7. Source-drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		29	A
I_{SDM} [1]	Source-drain current (pulsed)		-		103	A
V_{SD} [2]	Forward on voltage	I_{SD} = 29 A, V_{GS} = 0 V	-		1.6	V
t_{rr}	Reverse recovery time	I_{SD} = 29 A, di/dt = 100 A/µs, V_{DD} = 60 V, (see Figure 14. Test circuit for inductive load switching and diode recovery times)	-	110		ns
Q_{rr}	Reverse recovery charge		-	0.5		µC
I_{RRM}	Reverse recovery current		-	9		A
t_{rr}	Reverse recovery time	I_{SD} = 29 A, di/dt = 100 A/µs, V_{DD} = 60 V, T_j = 150 °C (see Figure 14. Test circuit for inductive load switching and diode recovery times)	-	215		ns
Q_{rr}	Reverse recovery charge		-	2		µC
I_{RRM}	Reverse recovery current		-	17		A

1. *Pulse width limited by safe operating area.*

2. *Pulsed: pulse duration = 300 µs, duty cycle 1.5%.*

Table 8. Gate-source Zener diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)GSO}$	Gate-source breakdown voltage	I_{GS} = ±1 mA, I_D = 0 A	±30	-	-	V

The built-in back-to-back Zener diodes are specifically designed to enhance the ESD performance of the device. The Zener voltage facilitates efficient and cost-effective device integrity protection, thus eliminating the need for additional external componentry.

Prerelease product(s)

2.1 Electrical characteristics (curves)

Figure 1. Safe operating area
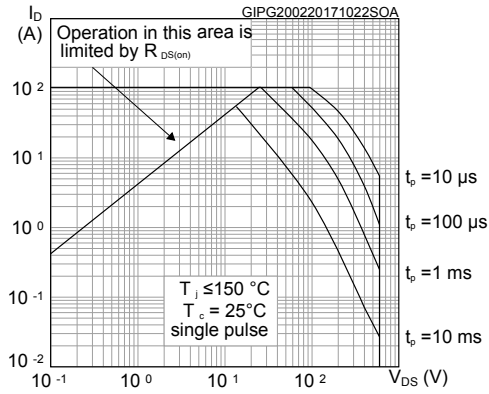
Figure 2. Thermal impedance
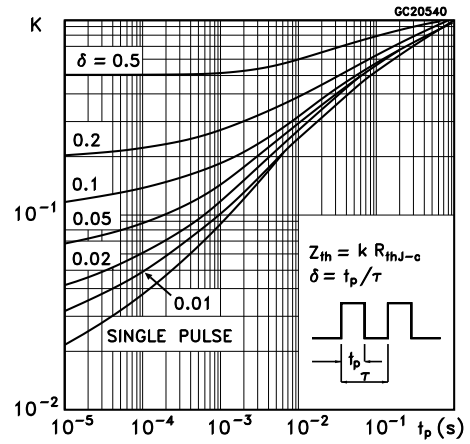
Figure 3. Output characteristics
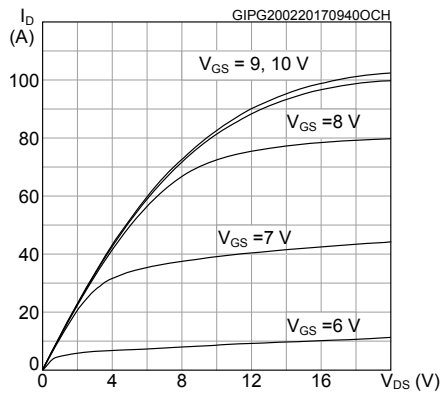
Figure 4. Transfer characteristics

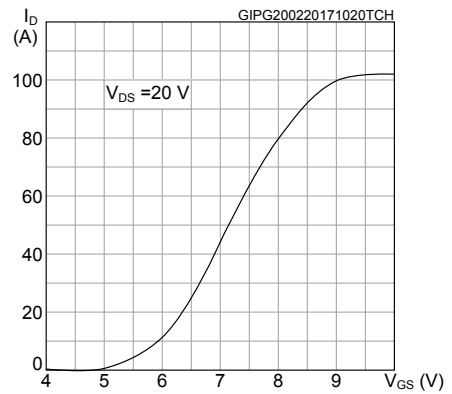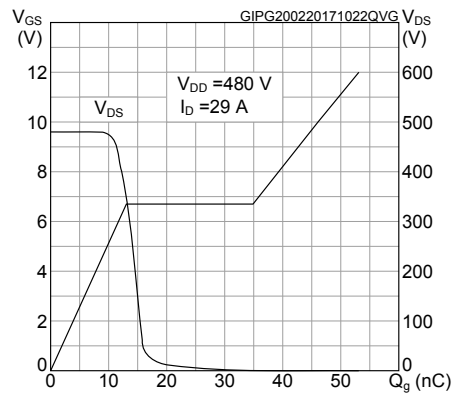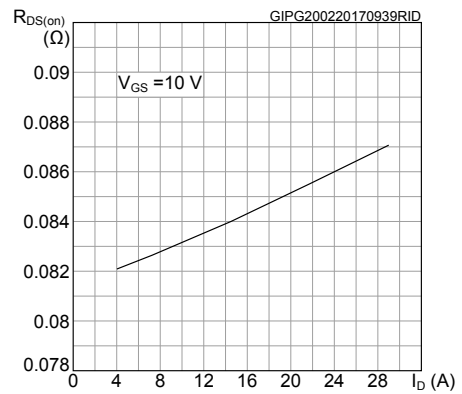**Figure 5. Gate charge vs gate-source voltage**

Figure 6. Static drain-source on-resistance

Figure 7. Capacitance variations

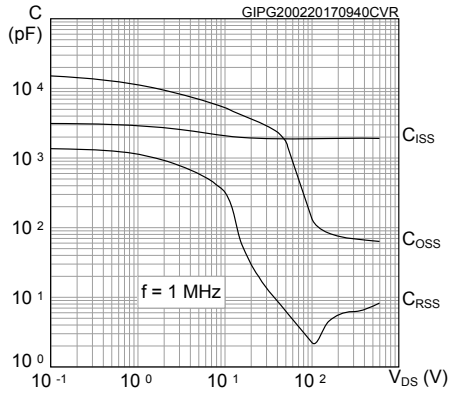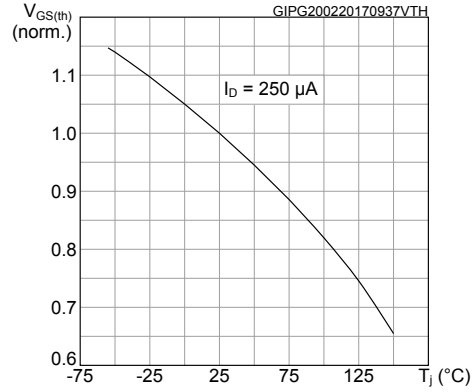### Figure 8. Normalized gate threshold voltage vs temperature
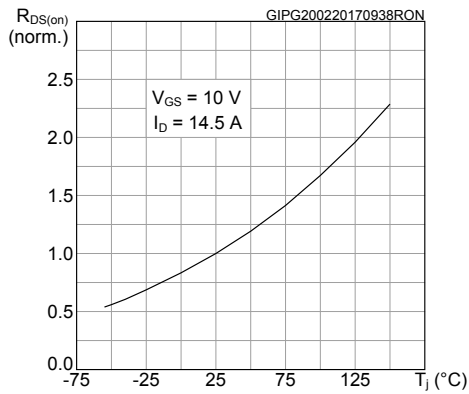

Figure 9. Normalized on-resistance vs temperature

Figure 10. Normalized $V_{(BR)DSS}$ vs temperature
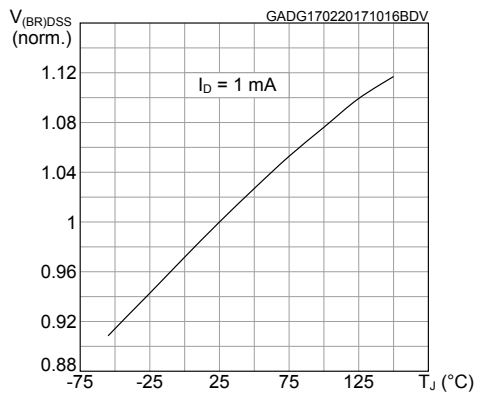
Figure 11. Source-drain diode forward characteristics
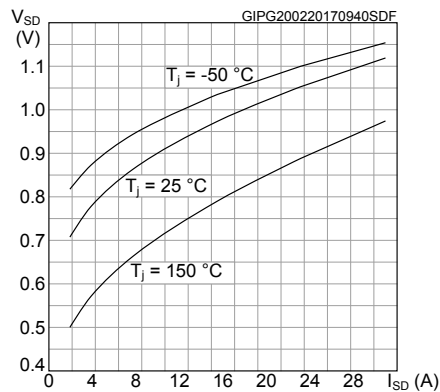
3 Test circuits

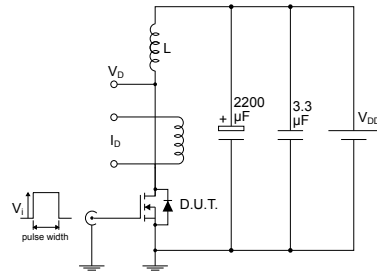**Figure 12. Test circuit for resistive load switching times**
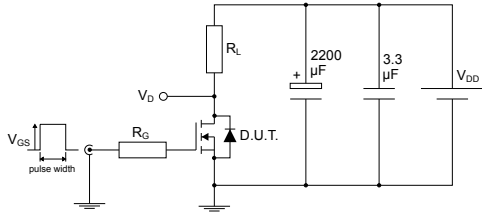
AM01468v1

Figure 13. Test circuit for gate charge behavior

AM01469v1

Figure 14. Test circuit for inductive load switching and diode recovery times

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Figure 15. Unclamped inductive load test circuit

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Figure 16. Unclamped inductive waveform

AM01472v1

Figure 17. Switching time waveform
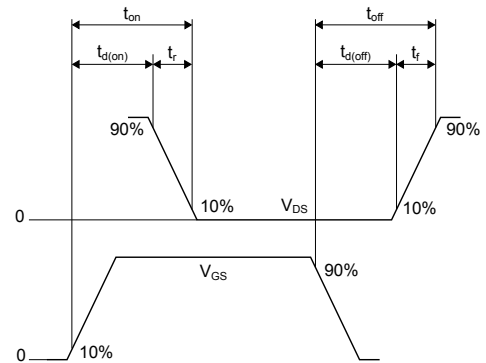
AM01473v1

4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

4.1 H²PAK-7 package information
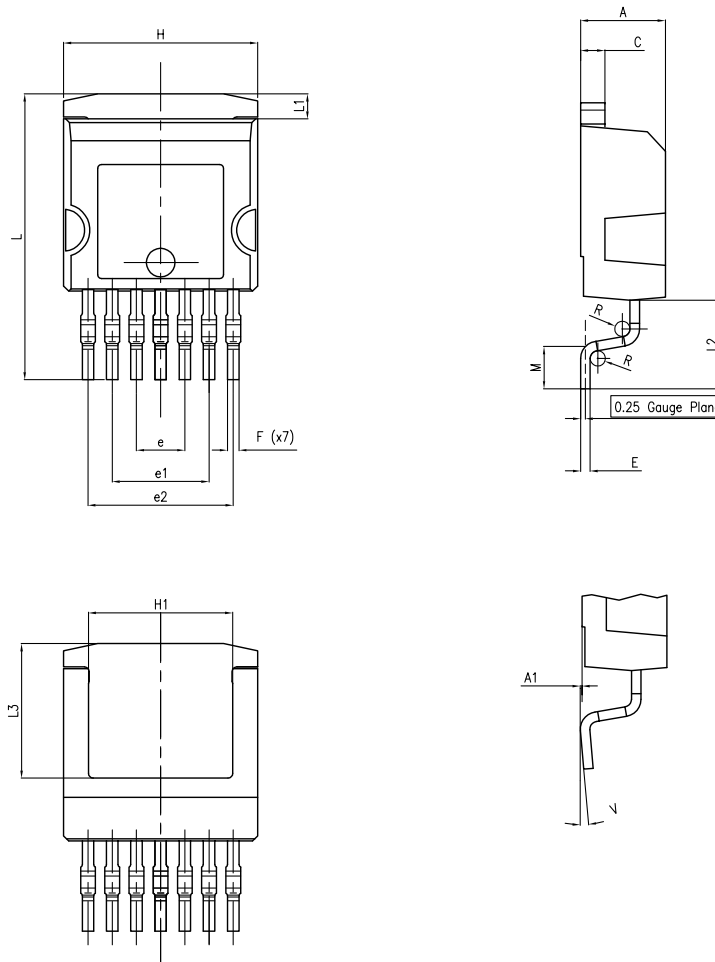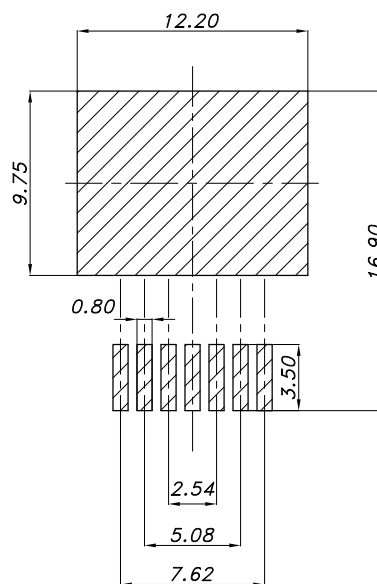
Figure 18. H²PAK-7 package outline

DM00249216_4

Table 9. H²PAK-7 package mechanical data

Dim.	mm	
	Min.	Max.
A	4.30	4.80
A1	0.03	0.20
C	1.17	1.37
e	2.34	2.74
e1	4.88	5.28
e2	7.42	7.82
E	0.45	0.60
F	0.50	0.70
H	10.00	10.40
H1	7.40	7.60
L	14.75	15.25
L1	1.27	1.40
L2	4.35	4.95
L3	6.85	7.25
M	1.90	2.50
R	0.20	0.60
V	0°	8°

Figure 19. H²PAK-7 recommended footprint

footprint_DM00249216_4

Note: *Dimensions are in mm.*

4.2 H²PAK-7 packing information

Figure 20. Tape outline

10 pitches cumulative
tolerance on tape +/- 0.2 mm

User direction of feed

User direction of feed

Bending radius
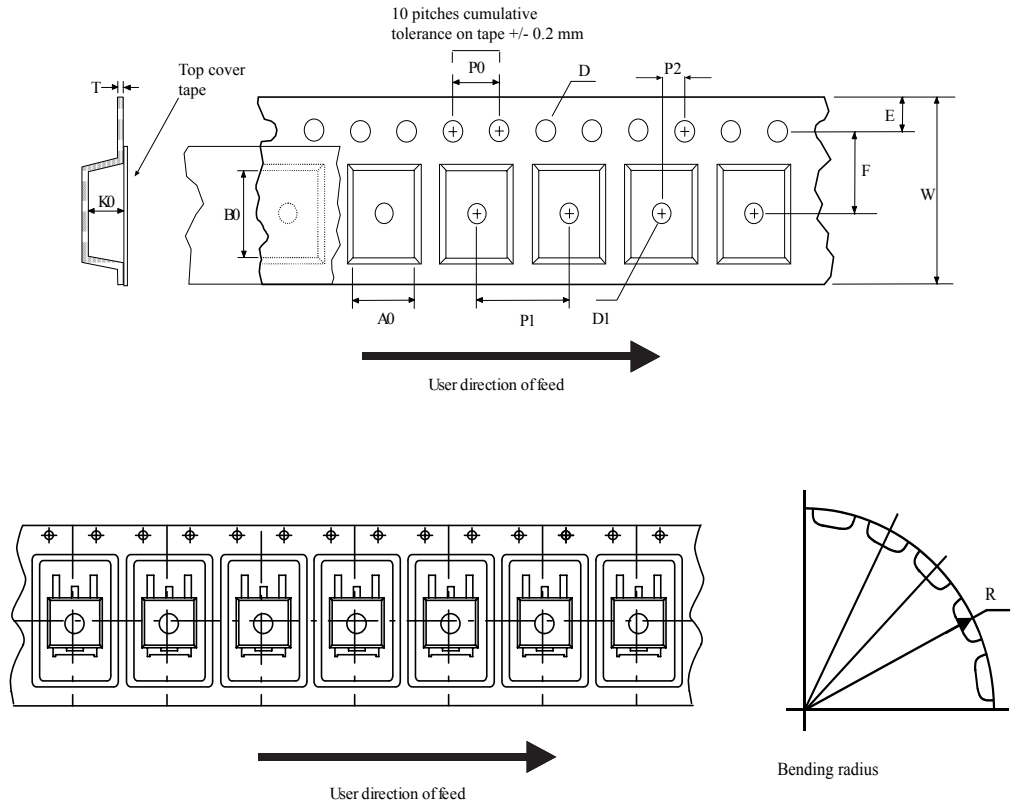
AM08852v2

Prerelease product(s)

Figure 21. Reel outline
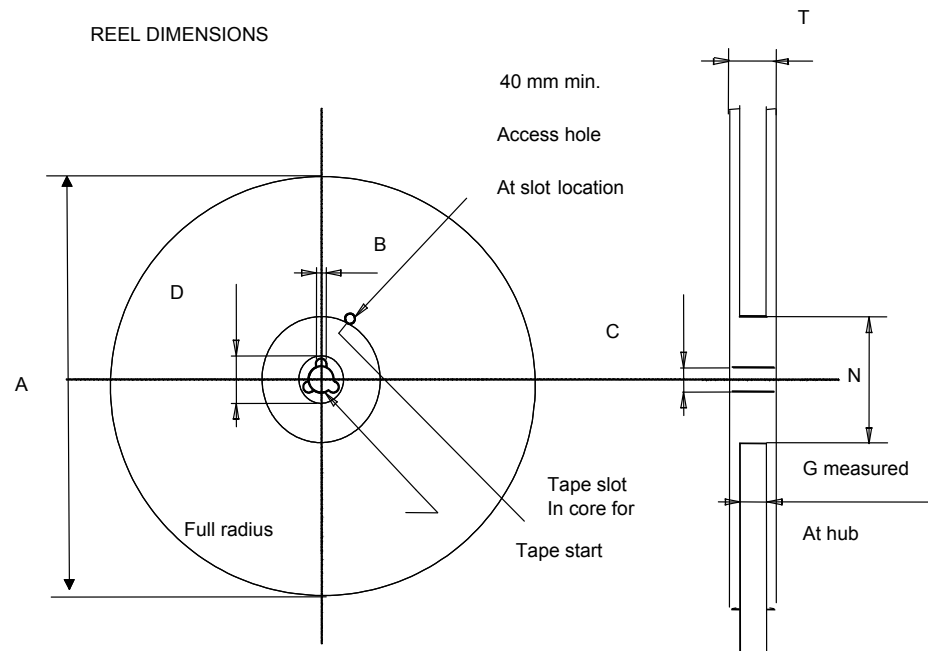
Table 10. Tape and reel mechanical data

Tape			Reel		
Dim.	mm		Dim.	mm	
	Min.	Max.		Min.	Max.
A0	10.5	10.7	A		330
B0	15.7	15.9	B	1.5	
D	1.5	1.6	C	12.8	13.2
D1	1.59	1.61	D	20.2	
E	1.65	1.85	G	24.4	26.4
F	11.4	11.6	N	100	
K0	4.8	5.0	T		30.4
P0	3.9	4.1			
P1	11.9	12.1	Base quantity		1000
P2	1.9	2.1	Bulk quantity		1000
R	50				
T	0.25	0.35			
W	23.7	24.3			

Revision history

Table 11. Document revision history

Date	Revision	Changes
16-Jun-2016	1	Initial release.
03-Nov-2017	2	Modified *Table 2: "Absolute maximum ratings"*, *Table 3: "Thermal data"*, *Table 5: "On/off-state"*, *Table 6: "Dynamic"*, *Table 7: "Switching times"* and *Table 8: "Source-drain diode"*. Added *Table 9: "Gate-source Zener diode "*. Added *Section 2.1: "Electrical characteristics (curves)"*. Minor text changes.
26-Sep-2018	3	Removed maturity status indication from cover page. The document status is production data. Updated title and features in cover page. Minor text changes.

Prerelease product(s)

Contents

Prerelease product(s)

IMPORTANT NOTICE – PLEASE READ CAREFULLY

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