

N - CHANNEL ENHANCEMENT MODE POWER MOS TRANSISTOR

PRELIMINARY DATA

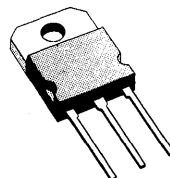
TYPE	V _{DSS}	R _{DS(on)}	I _D
STHV102	1000 V	3.5 Ω	4.2 A

- 1000 V - VERY HIGH VOLTAGE FOR SMPS
- EASY DRIVE - REDUCED COST AND SIZE
- ULTRA FAST SWITCHING
- HIGH RESOLUTION CTV DEFLECTION

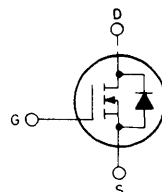
INDUSTRIAL APPLICATIONS:

- SINGLE TRANSISTOR HIGH VOLTAGE SWITCH
- SWITCHING POWER SUPPLIES

N - channel enhancement mode POWER MOS field effect transistor. Easy drive and very fast switching times make these POWER MOS transistors ideal for high speed switching applications. Typical uses include single transistor forward and flyback converters and lamp ballast. They are also used in high voltage CTV EHT supplies, interfaces to thyristor and power transistors operating from 380V and 440V A.C. supplies and resonant converters operating up to 500kHz.



TO-218

**INTERNAL SCHEMATIC
DIAGRAM**

ABSOLUTE MAXIMUM RATINGS

V _{DS}	Drain-source voltage (V _{GS} = 0)	1000	V
V _{GS}	Gate-source voltage	±20	V
I _D	Drain current (cont.) at T _c = 25°C	4.2	A
I _D	Drain current (cont.) at T _c = 100°C	2.6	A
I _{DM} (*)	Drain current (pulsed)	16	A
P _{tot}	Total dissipation at T _c < 25°C	125	W
	Derating factor	1	W/°C
T _{stg}	Storage temperature	- 65 to 150	°C
T _j	Max. operating junction temperature	150	°C

(*) Pulse width limited by safe operating area

THERMAL DATA

$R_{thj - case}$	Thermal resistance junction-case	max	1	°C/W
T_L	Maximum lead temperature for soldering purpose		275	°C

ELECTRICAL CHARACTERISTICS
($T_{case} = 25^{\circ}C$ unless otherwise specified)

Parameters	Test Conditions	Min.	Typ.	Max.	Unit
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OFF

$V_{(BR) DSS}$	Drain-source breakdown voltage	$I_D = 250 \mu A$	$V_{GS} = 0$	1000			V
I_{DSS}	Zero gate voltage drain current ($V_{GS} = 0$)	$V_{DS} = \text{Max Rating}$ $V_{DS} = \text{Max Rating} \times 0.8$	$T_c = 125^{\circ}C$			250 1000	μA μA
I_{GSS}	Gate-body leakage current ($V_{DS} = 0$)	$V_{GS} = \pm 20 V$				100	nA

ON (*)

$V_{GS (th)}$	Gate threshold voltage	$V_{DS} = V_{GS}$	$I_D = 250 \mu A$	2		4	V
$R_{DS (on)}$	Static drain-source on resistance	$V_{GS} = 10 V$	$I_D = 2 A$			3.5	Ω

DYNAMIC

g_{fs}	Forward transconductance	$V_{DS} = 25 V$	$I_D = 2 A$	2			mho
C_{iss}	Input capacitance	$V_{DS} = 25 V$	$f = 1 MHz$		900	1200	pF
C_{oss}	Output capacitance	$V_{GS} = 0$			150	250	pF
C_{rss}	Reverse transfer capacitance				90	110	pF

SWITCHING

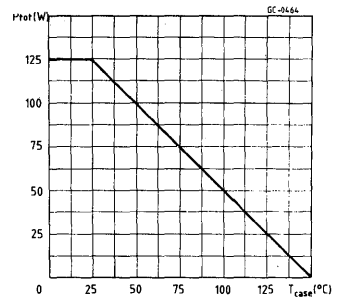
$t_{d (on)}$	Turn-on time	$V_{DD} = 400 V$	$I_D = 2 A$		40		ns
t_r	Rise time	$V_i = 10 V$	$R_i = 50 \Omega$		100		ns
$t_{d (off)}$	Turn-off delay time	(see test circuit)			300		ns
t_f	Fall time				100		ns
Q_g	Total gate Charge	$V_{DD} = 500 V$ $V_{GS} = 10 V$	$I_D = 6 A$			70	nC

Parameters	Test Conditions	Min.	Typ.	Max.	Unit
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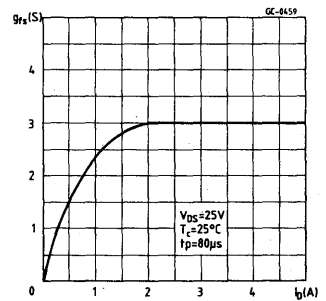
I_{SD}	Source-drain current				4.2	A
I_{SDM}^*	Source-drain current (pulsed)				16	A
V_{SD}	Forward on voltage	$I_{SD} = 4.2 \text{ A}$	$V_{GS} = 0$		2.5	V
t_{rr}	Reverse recovery time	$I_{SD} = 4.2 \text{ A}$	$V_{GS} = 0$		1000	ns
Q_{rr}	Reverse recovery charge	$di/dt = 100 \text{ A}/\mu\text{s}$			15	μC

(*) Pulse width limited by safe operating area

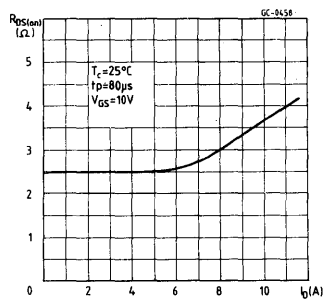
Derating curve



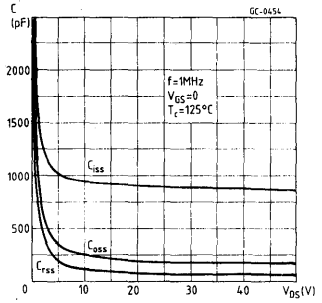
Transconductance



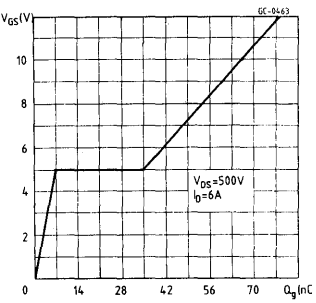
Static drain-source on resistance



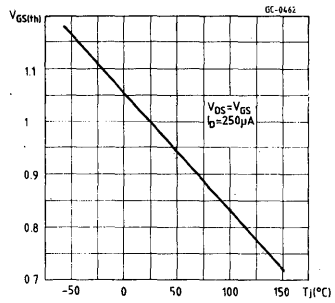
Capacitance variation



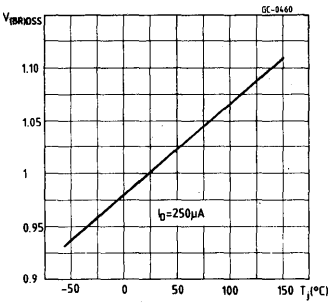
Gate charge vs gate-source voltage



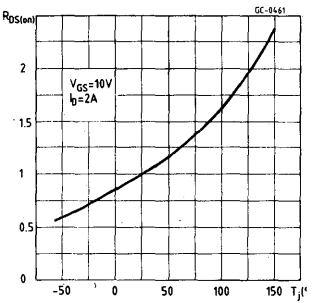
Normalized gate threshold voltage vs temperature



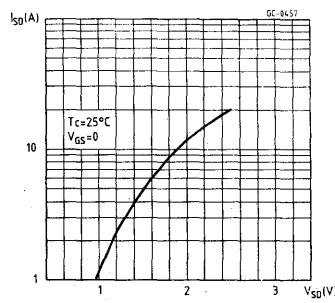
Normalized breakdown voltage vs temperature



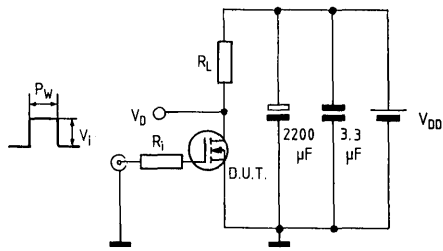
Normalized on resistance vs temperature



Static drain diode forward characteristic

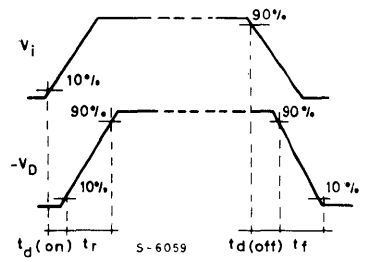


Switching times test circuit for resistive load

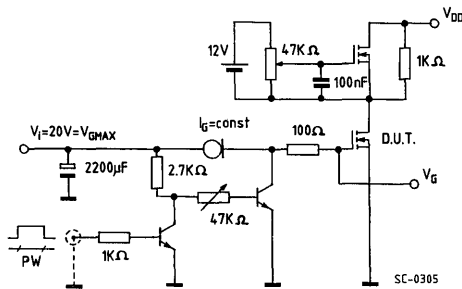
Pulse width $\leq 100 \mu\text{s}$ Duty cycle $\leq 2\%$

SC-0008/1

Switching time waveforms for resistive load



Gate charge test circuit

PW adjusted to obtain required V_G Body-drain diode t_{rr} measurement
Jedec test circuit