

## N-channel 600 V, 0.53 $\Omega$ typ., 10 A MDmesh™ II Power MOSFET in I<sup>2</sup>PAK package

Datasheet - obsolete product

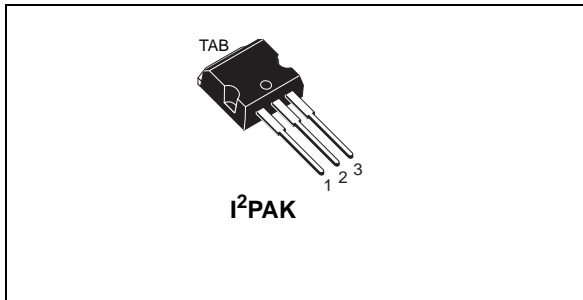
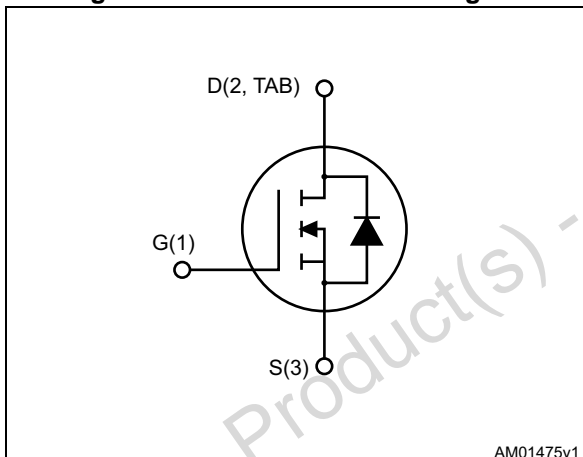


Figure 1. Internal schematic diagram



### Features

Order code	$V_{DS}$ @ $T_{Jmax}$	$R_{DS(on)}$ max.	$I_D$	$P_{TOT}$
STI10NM60N	650 V	< 0.53 $\Omega$	10 A	70 W

- 100% avalanche tested
- Low input capacitance and gate charge
- Low gate input resistance

### Applications

- Switching applications

### Description

This device is an N-channel Power MOSFET developed using the second generation of MDmesh™ technology. This revolutionary Power MOSFET associates a vertical structure to the company's strip layout to yield one of the world's lowest on-resistance and gate charge. It is therefore suitable for the most demanding high efficiency converters.

Table 1. Device summary

Order code	Marking	Package	Packing
STI10NM60N	10NM60N	I <sup>2</sup> PAK	Tube

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Obsolete Product(s) - Obsolete Product(s)



# 1 Electrical ratings

**Table 2. Absolute maximum ratings**

Symbol	Parameter	Value	
		I <sup>2</sup> PAK	Unit
V <sub>GS</sub>	Gate- source voltage	± 25	V
I <sub>D</sub>	Drain current (continuous) at T <sub>C</sub> = 25 °C	10	A
I <sub>D</sub>	Drain current (continuous) at T <sub>C</sub> = 100 °C	5	A
I <sub>DM</sub> <sup>(1)</sup>	Drain current (pulsed)	32	A
P <sub>TOT</sub>	Total dissipation at T <sub>C</sub> = 25 °C	70	W
dv/dt <sup>(2)</sup>	Peak diode recovery voltage slope	15	V/ns
V <sub>ISO</sub>	Insulation withstand voltage (RMS) from all three leads to external heat sink (t = 1 s; T <sub>C</sub> = 25 °C)		V
T <sub>J</sub> T <sub>stg</sub>	Operating junction temperature Storage temperature	- 55 to 150	°C

1. Pulse width limited by safe operating area.
2. I<sub>SD</sub> ≤ 10 A, di/dt ≤ 400 A/μs, V<sub>DS peak</sub> ≤ V<sub>(BR)DSS</sub>, V<sub>DD</sub> = 80% V<sub>(BR)DSS</sub>.

**Table 3. Thermal data**

Symbol	Parameter	Value	
		I <sup>2</sup> PAK	Unit
R <sub>thj-case</sub>	Thermal resistance junction-case max.	1.79	°C/W
R <sub>thj-amb</sub>	Thermal resistance junction-ambient max.	62.50	°C/W
R <sub>thj-pcb</sub>	Thermal resistance junction-pcb max.		°C/W

**Table 4. Avalanche characteristics**

Symbol	Parameter	Value	Unit
I <sub>AS</sub>	Avalanche current, repetitive or not-repetitive (pulse width limited by T <sub>J</sub> max.)	4	A
E <sub>AS</sub>	Single pulse avalanche energy (starting T <sub>J</sub> = 25 °C, I <sub>D</sub> = I <sub>AS</sub> , V <sub>DD</sub> = 50 V)	200	mJ

## 2 Electrical characteristics

( $T_{\text{case}} = 25\text{ °C}$  unless otherwise specified)

**Table 5. On /off states**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$I_D = 1\text{ mA}$ , $V_{GS} = 0$ $I_D = 1\text{ mA}$ , $V_{GS} = 0$ , $T_C = 150\text{ °C}$	600	650		V
$I_{DSS}$	Zero-gate voltage drain current ( $V_{GS} = 0$ )	$V_{DS} = 600\text{ V}$ $V_{DS} = 600\text{ V}$ , $T_C = 125\text{ °C}$			1 100	$\mu\text{A}$ $\mu\text{A}$
$I_{GSS}$	Gate-body leakage current ( $V_{DS} = 0$ )	$V_{GS} = \pm 25\text{ V}$			$\pm 100$	nA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}$ , $I_D = 250\text{ }\mu\text{A}$	2	3	4	V
$R_{DS(on)}$	Static drain-source on-resistance	$V_{GS} = 10\text{ V}$ , $I_D = 4\text{ A}$		0.53	0.55	$\Omega$

**Table 6. Dynamic**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$C_{iss}$	Input capacitance	$V_{DS} = 50\text{ V}$ , $f = 1\text{ MHz}$ , $V_{GS} = 0$	-	540	-	pF
$C_{oss}$	Output capacitance		-	44	-	pF
$C_{riss}$	Reverse transfer capacitance		-	1.2	-	pF
$C_{oss\text{ eq}}^{(1)}$	Equivalent capacitance time related	$V_{DS} = 0\text{ to }480\text{ V}$ , $V_{GS} = 0$	-	110	-	pF
$R_g$	Gate input resistance	$f = 1\text{ MHz}$ open drain	-	6	-	$\Omega$
$Q_g$	Total gate charge	$V_{DD} = 480\text{ V}$ , $I_D = 8\text{ A}$ , $V_{GS} = 10\text{ V}$	-	19	-	nC
$Q_{gs}$	Gate-source charge		-	3	-	nC
$Q_{gd}$	Gate-drain charge		-	10	-	nC

1.  $C_{oss\text{ eq}}$  time related is defined as a constant equivalent capacitance giving the same charging time as  $C_{oss}$  when  $V_{DS}$  increases from 0 to 80%  $V_{DSS}$ .

Table 7. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 300\text{ V}$ , $I_D = 4\text{ A}$ , $R_G = 4.7\ \Omega$ , $V_{GS} = 10\text{ V}$	-	10	-	ns
$t_r$	Rise time		-	12	-	ns
$t_{d(off)}$	Turn-off-delay time		-	32	-	ns
$t_f$	Fall time		-	15	-	ns

Table 8. Source-drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$I_{SD}$	Source-drain current		-		8	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)				32	A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD} = 8\text{ A}$ , $V_{GS} = 0$	-		1.3	V
$t_{rr}$	Reverse recovery time	$I_{SD} = 8\text{ A}$ , $di/dt = 100\text{ A}/\mu\text{s}$ $V_{DD} = 60\text{ V}$	-	250		ns
$Q_{rr}$	Reverse recovery charge		-	2.12		$\mu\text{C}$
$I_{RRM}$	Reverse recovery current				17	A
$t_{rr}$	Reverse recovery time	$I_{SD} = 8\text{ A}$ , $di/dt = 100\text{ A}/\mu\text{s}$ $V_{DD} = 60\text{ V}$ , $T_J = 150\text{ }^\circ\text{C}$	-	315		ns
$Q_{rr}$	Reverse recovery charge				2.6	$\mu\text{C}$
$I_{RRM}$	Reverse recovery current				16.5	A

1. Pulse width limited by safe operating area.
2. Pulsed: pulse duration = 300  $\mu\text{s}$ , duty cycle 1.5%

## 2.1 Electrical characteristics (curves)

Figure 2. Safe operating area for I<sup>2</sup>PAK

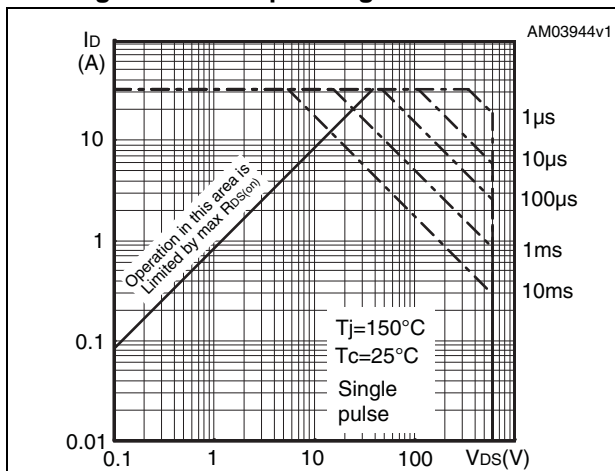


Figure 3. Thermal impedance for I<sup>2</sup>PAK

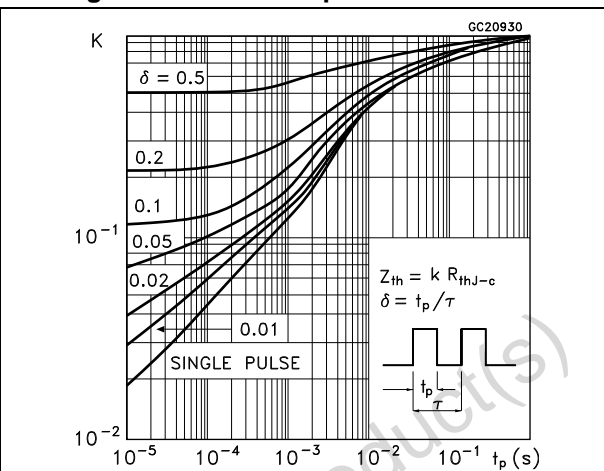


Figure 4. Output characteristics

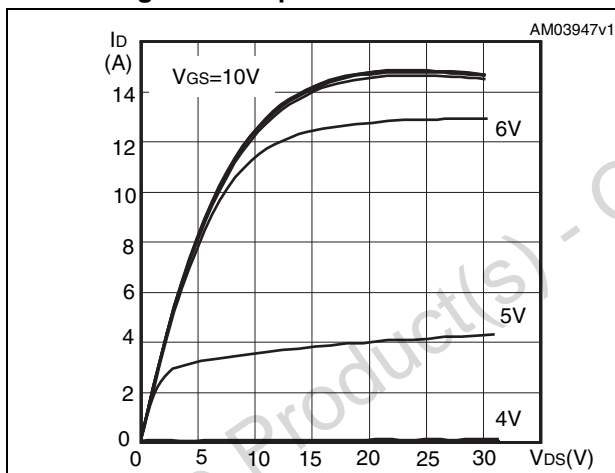


Figure 5. Transfer characteristics

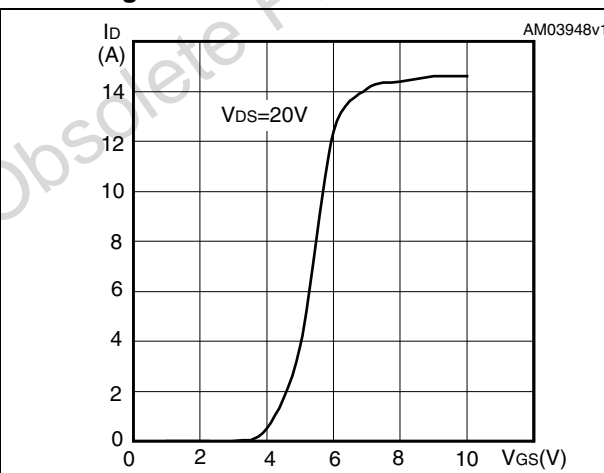


Figure 6. Normalized V<sub>DS</sub> vs. temperature

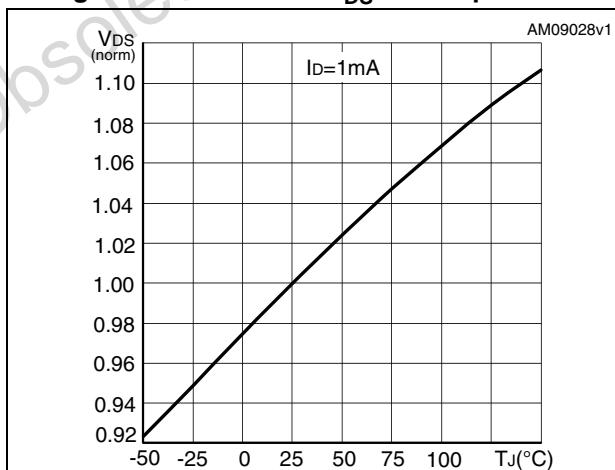


Figure 7. Static drain-source on-resistance

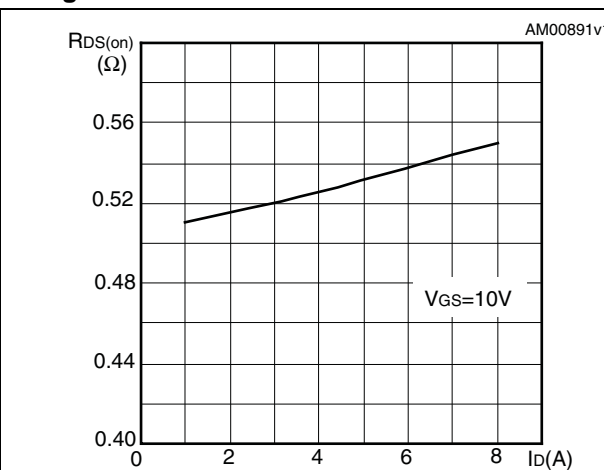


Figure 8. Gate charge vs. gate-source voltage

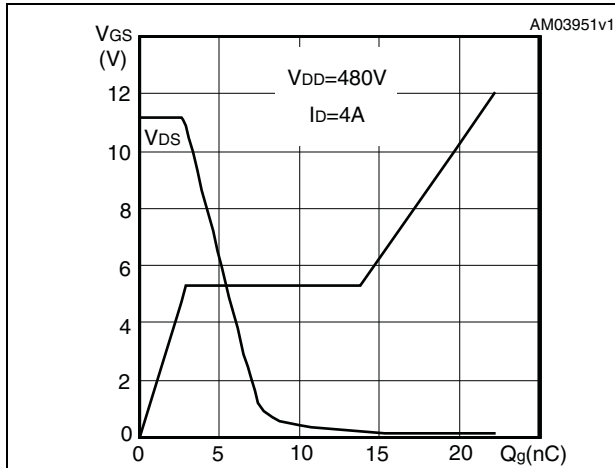


Figure 9. Capacitance variations

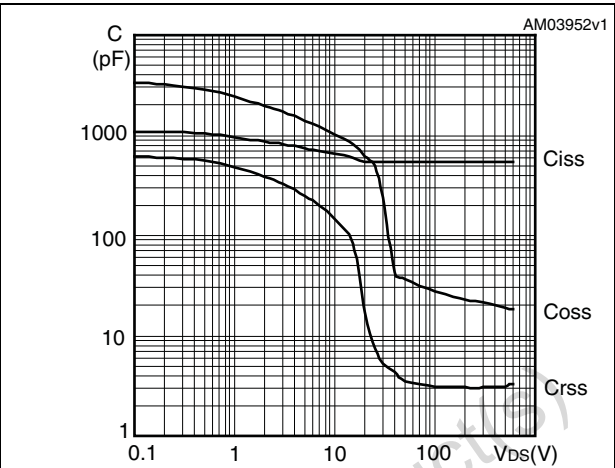


Figure 10. Normalized gate threshold voltage vs. temperature

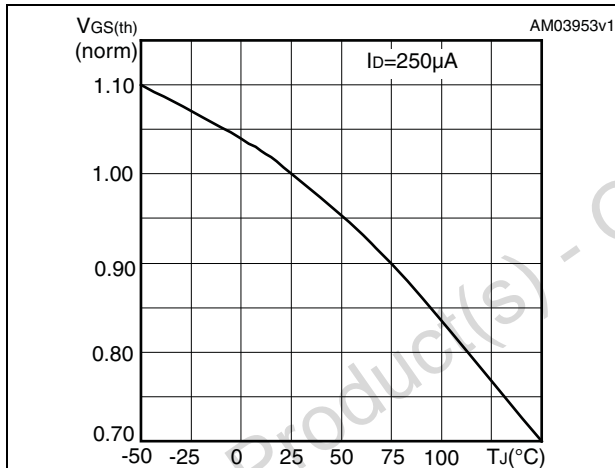
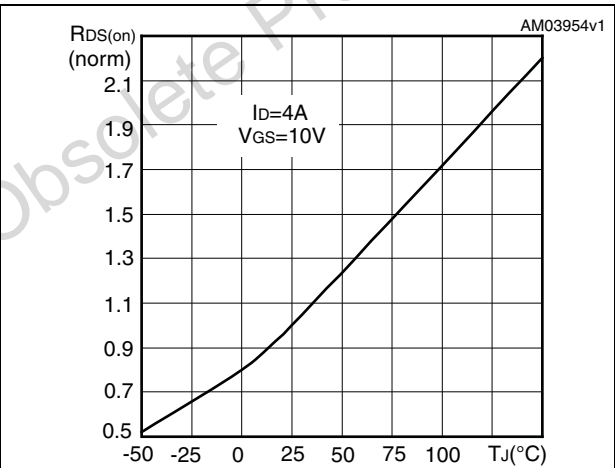


Figure 11. Normalized on-resistance vs. temperature



### 3 Test circuits

Figure 12. Switching times test circuit for resistive load



Figure 13. Gate charge test circuit

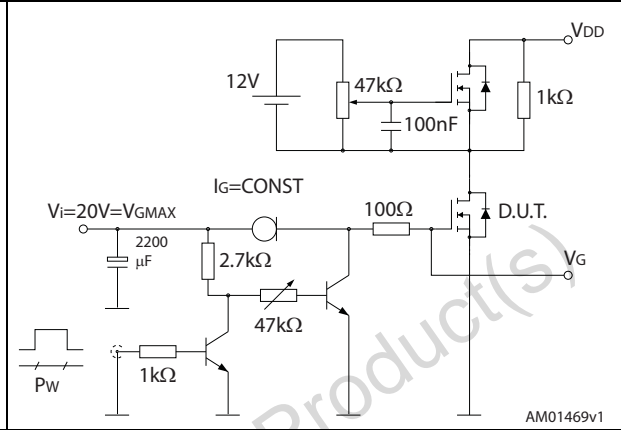


Figure 14. Test circuit for inductive load switching and diode recovery times

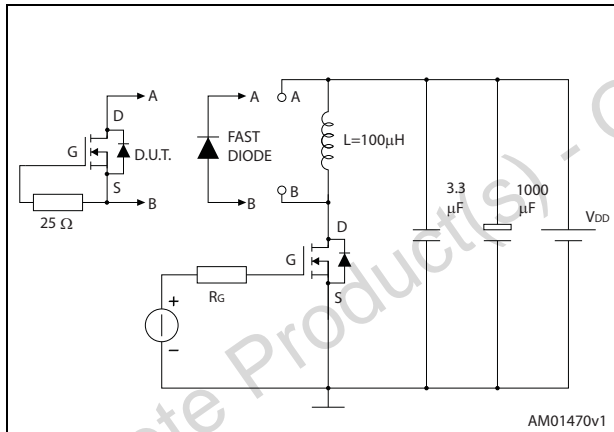


Figure 15. Unclamped inductive load test circuit

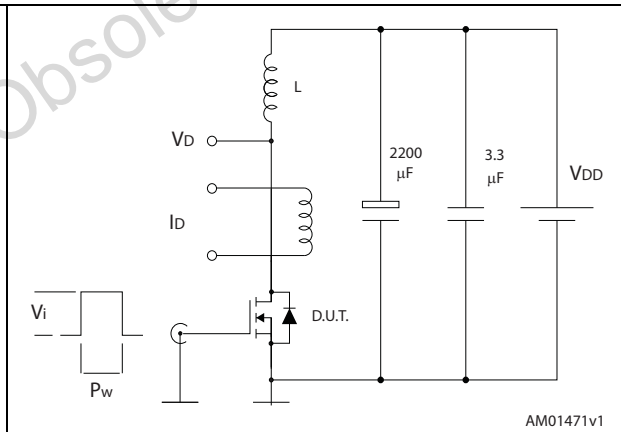


Figure 16. Unclamped inductive waveform

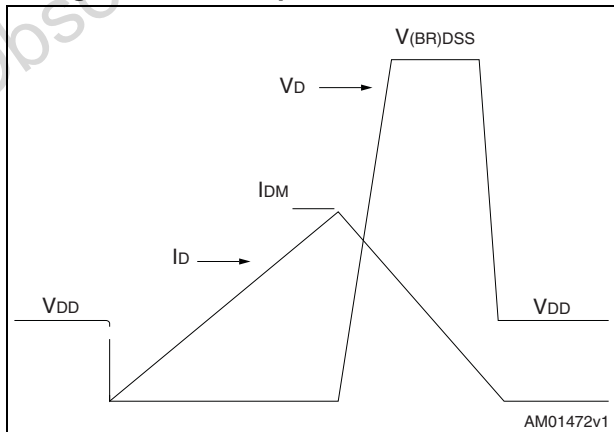
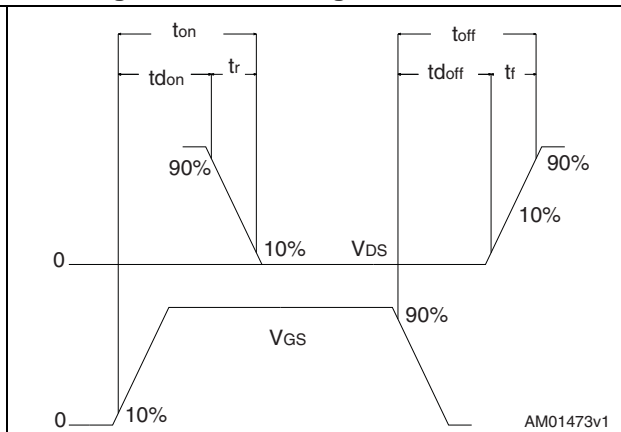


Figure 17. Switching time waveform





## 4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK<sup>®</sup> packages, depending on their level of environmental compliance. ECOPACK<sup>®</sup> specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com). ECOPACK is an ST trademark.

### 4.1 I<sup>2</sup>PAK package information

Figure 18. I<sup>2</sup>PAK (TO-262) package outline

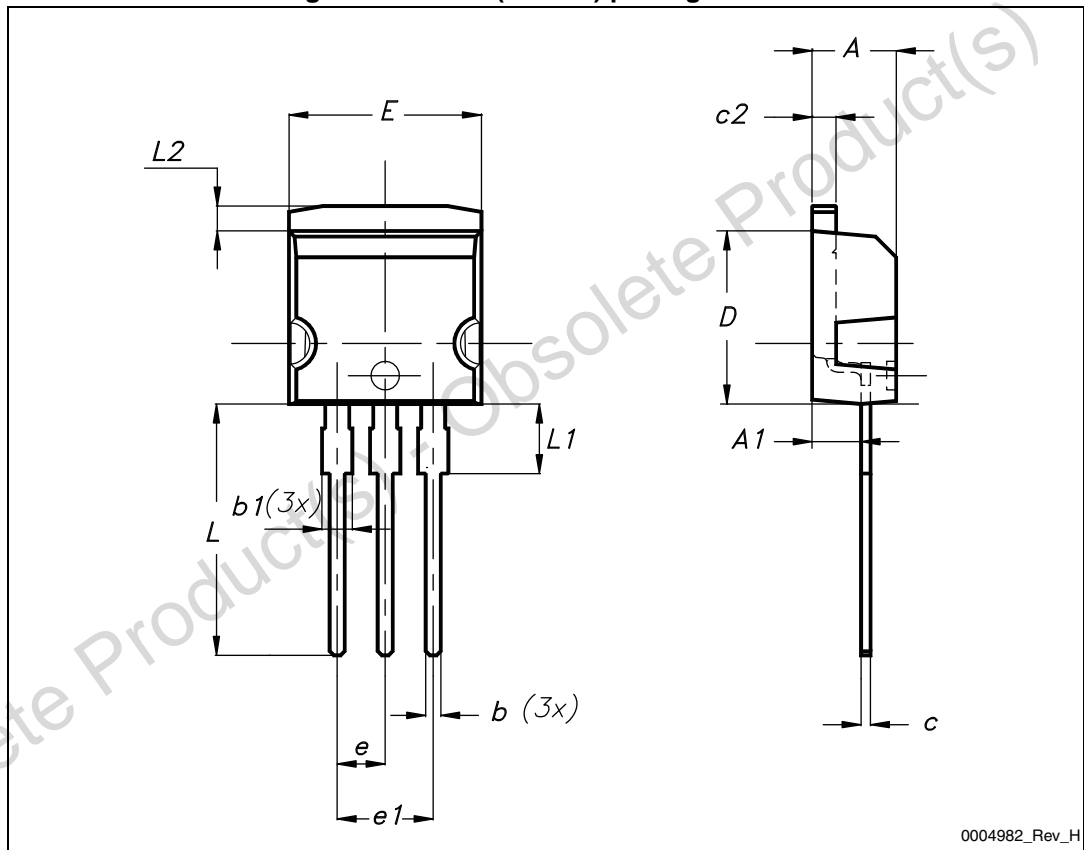


Table 9. I<sup>2</sup>PAK (TO-262) package mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.40		4.60
A1	2.40		2.72
b	0.61		0.88
b1	1.14		1.70
c	0.49		0.70
c2	1.23		1.32
D	8.95		9.35
e	2.40		2.70
e1	4.95		5.15
E	10		10.40
L	13		14
L1	3.50		3.93
L2	1.27		1.40

## 5 Revision history

Table 10. Document revision history

Date	Revision	Changes
10-Jun-2009	1	First release
12-Jan-2010	2	Figure 4: Safe operating area for TO-220FP has been corrected
31-Mar-2010	3	Features have been corrected
17-Sep-2010	4	Content reworked to improve readability
24-Nov-2010	5	Corrected $I_D$ value
16-Nov-2012	6	Inserted new package and mechanical data: I <sup>2</sup> PAK
18-Jul-2013	7	Updated Section 4: Package mechanical data. Minor text changes.
02-Dec-2015	8	Part numbers STD10NM60N, STF10NM60N, STP10NM60N, STU10NM60N have been moved to a separate datasheet.

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