

Automotive-grade N-channel 40 V, 2.1 mΩ typ., 120 A STripFET™ F6 Power MOSFET in an I²PAK package

Datasheet - production data

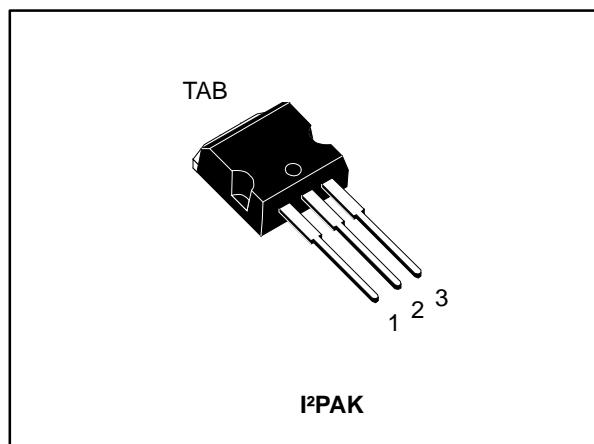


Figure 1: Internal schematic diagram

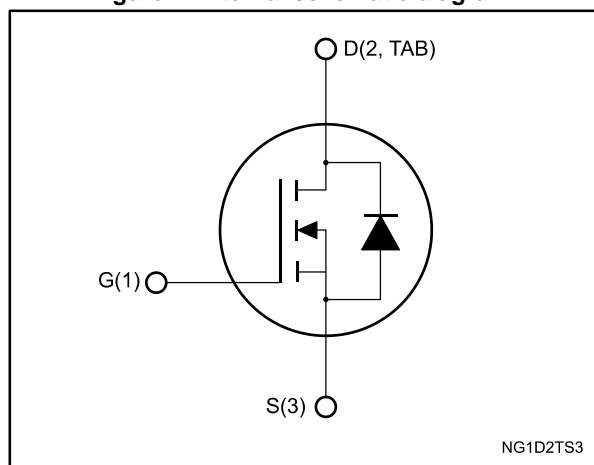


Table 1: Device summary

| Order code | Marking | Package | Packing |
|--------------|---------|--------------------|---------|
| STI175N4F6AG | 175N4F6 | I ² PAK | Tube |

Features

| Order code | V _{DS} | R _{DS(on)} max. | I _D | P _{TOT} |
|--------------|-----------------|--------------------------|----------------|------------------|
| STI175N4F6AG | 40 V | 2.7 mΩ | 120 A | 190 W |

- Designed for automotive applications and AEC-Q101 qualified
- Very low on-resistance
- Very low gate charge
- High avalanche ruggedness
- Low gate drive power loss

Applications

- Switching applications
- Power tools

Description

This device is an N-channel Power MOSFET developed using the STripFET™ F6 technology with a new trench gate structure. The resulting Power MOSFET exhibits very low R_{DS(on)} in all packages.

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1 Electrical ratings

Table 2: Absolute maximum ratings

| Symbol | Parameter | Value | Unit |
|----------------|--|------------|------------------|
| V_{DS} | Drain-source voltage | 40 | V |
| V_{GS} | Gate-source voltage | ± 20 | V |
| $I_D^{(1)}$ | Drain current (continuous) at $T_{case} = 25\text{ }^\circ\text{C}$ | 120 | A |
| | Drain current (continuous) at $T_{case} = 100\text{ }^\circ\text{C}$ | 120 | |
| $I_{DM}^{(2)}$ | Drain current (pulsed) | 480 | A |
| P_{TOT} | Total dissipation at $T_{case} = 25\text{ }^\circ\text{C}$ | 190 | W |
| T_{stg} | Storage temperature range | -55 to 175 | $^\circ\text{C}$ |
| T_j | Operating junction temperature range | | |

Notes:

(1) Limited by package

(2) Pulse width limited by safe operating area.

Table 3: Thermal data

| Symbol | Parameter | Value | Unit |
|----------------|----------------------------------|-------|--------------------|
| $R_{thj-case}$ | Thermal resistance junction-case | 0.79 | $^\circ\text{C/W}$ |
| $R_{thj-amb}$ | Thermal resistance junction-amb | 62.5 | |

2 Electrical characteristics

($T_{\text{case}} = 25\text{ °C}$ unless otherwise specified)

Table 4: Static

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|-----------------------------|-----------------------------------|---|------|------|-----------|------------------|
| $V_{(\text{BR})\text{DSS}}$ | Drain-source breakdown voltage | $V_{\text{GS}} = 0\text{ V}$, $I_{\text{D}} = 1\text{ mA}$ | 40 | | | V |
| I_{DSS} | Zero gate voltage drain current | $V_{\text{GS}} = 0\text{ V}$, $V_{\text{DS}} = 40\text{ V}$ | | | 1 | μA |
| | | $V_{\text{GS}} = 0\text{ V}$, $V_{\text{DS}} = 40\text{ V}$, $T_{\text{case}} = 125\text{ °C}$ | | | 100 | |
| I_{GSS} | Gate-body leakage current | $V_{\text{DS}} = 0\text{ V}$, $V_{\text{GS}} = \pm 20\text{ V}$ | | | ± 100 | nA |
| $V_{\text{GS}(\text{th})}$ | Gate threshold voltage | $V_{\text{DS}} = V_{\text{GS}}$, $I_{\text{D}} = 250\text{ }\mu\text{A}$ | 3 | | 4.5 | V |
| $R_{\text{DS}(\text{on})}$ | Static drain-source on-resistance | $V_{\text{GS}} = 10\text{ V}$, $I_{\text{D}} = 60\text{ A}$ | | 2.1 | 2.7 | $\text{m}\Omega$ |

Table 5: Dynamic

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|------------------|------------------------------|--|------|------|------|-------------|
| C_{ISS} | Input capacitance | $V_{\text{DS}} = 20\text{ V}$, $f = 1\text{ MHz}$, $V_{\text{GS}} = 0\text{ V}$ | - | 7735 | - | pF |
| C_{OSS} | Output capacitance | | - | 745 | - | |
| C_{RSS} | Reverse transfer capacitance | | - | 560 | - | |
| Q_{g} | Total gate charge | $V_{\text{DD}} = 20\text{ V}$, $I_{\text{D}} = 120\text{ A}$, $V_{\text{GS}} = 10\text{ V}$ (see Figure 14: "Test circuit for gate charge behavior") | - | 130 | - | nC |
| Q_{gs} | Gate-source charge | | - | 36 | - | |
| Q_{gd} | Gate-drain charge | | - | 42 | - | |

Table 6: Switching times

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|----------------------------|---------------------|---|------|------|------|------|
| $t_{\text{d}(\text{on})}$ | Turn-on delay time | $V_{\text{DD}} = 20\text{ V}$, $I_{\text{D}} = 60\text{ A}$, $R_{\text{G}} = 4.7\text{ }\Omega$, $V_{\text{GS}} = 10\text{ V}$ (see Figure 13: "Test circuit for resistive load switching times" and Figure 18: "Switching time waveform") | - | 24 | - | ns |
| t_{r} | Rise time | | - | 150 | - | |
| $t_{\text{d}(\text{off})}$ | Turn-off delay time | | - | 106 | - | |
| t_{f} | Fall time | | - | 57 | - | |

Table 7: Source-drain diode

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|-----------------|-------------------------------|--|------|------|------|------|
| $I_{SD}^{(1)}$ | Source-drain current | | - | | 120 | A |
| $I_{SDM}^{(2)}$ | Source-drain current (pulsed) | | - | | 480 | A |
| $V_{SD}^{(2)}$ | Forward on voltage | $V_{GS} = 0 \text{ V}$, $I_{SD} = 120 \text{ A}$ | - | | 1.3 | V |
| t_{rr} | Reverse recovery time | $I_{SD} = 120 \text{ A}$, $di/dt = 100 \text{ A}/\mu\text{s}$, $V_{DD} = 32 \text{ V}$ (see Figure 15: "Test circuit for inductive load switching and diode recovery times") | - | 36 | | ns |
| Q_{rr} | Reverse recovery charge | | - | 40 | | nC |
| I_{RRM} | Reverse recovery current | | - | 2.3 | | A |

Notes:

(1) Limited by package.

(2) Pulse test: pulse duration = 300 μs , duty cycle 1.5%.

2.1 Electrical characteristics (curves)

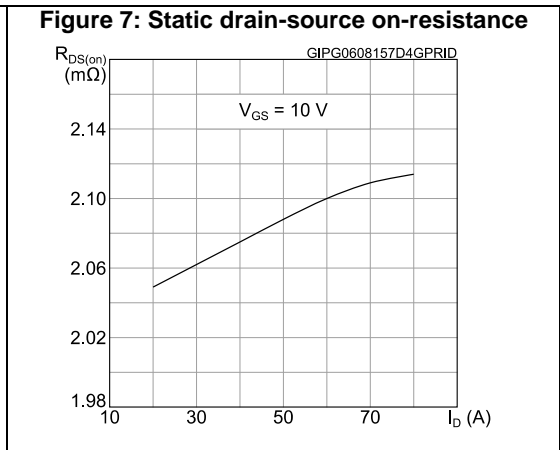
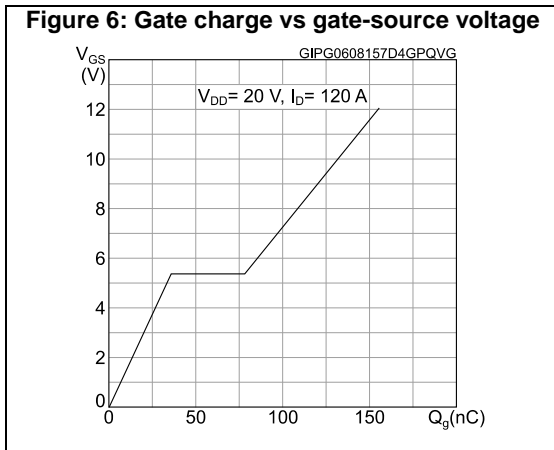
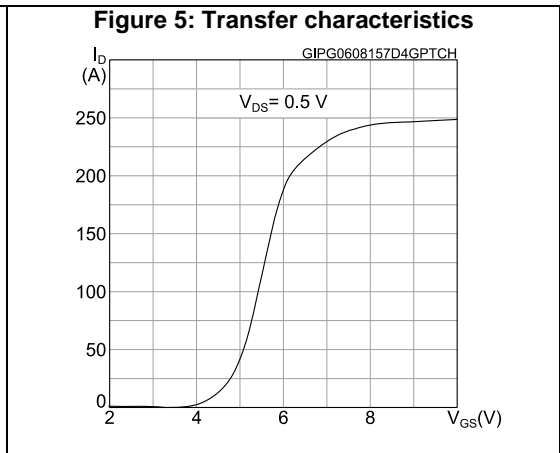
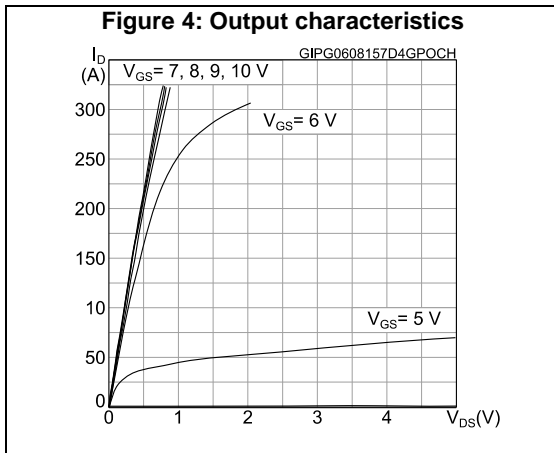
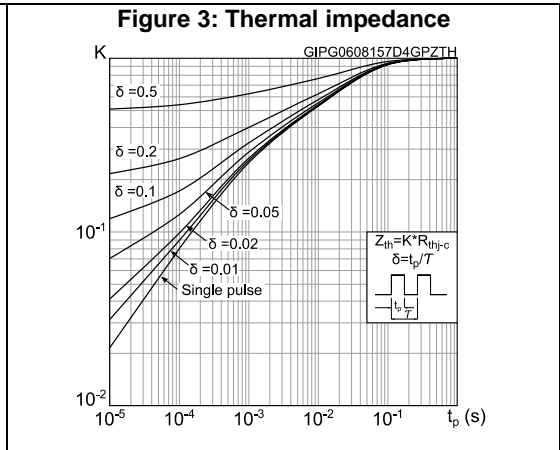
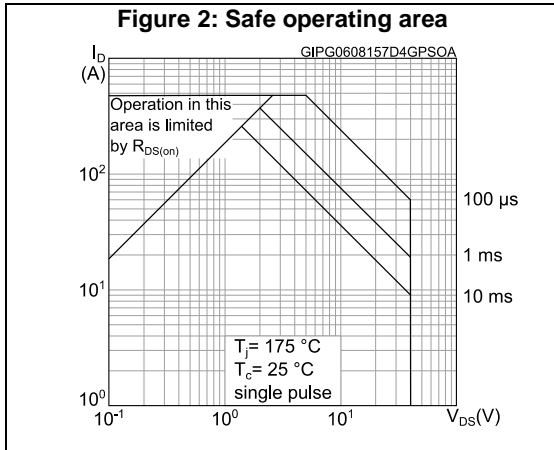


Figure 8: Capacitance variations

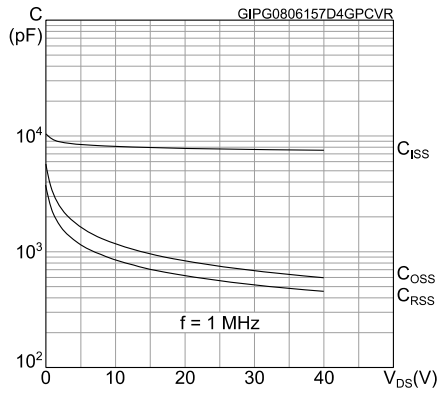


Figure 9: Normalized gate threshold voltage vs temperature

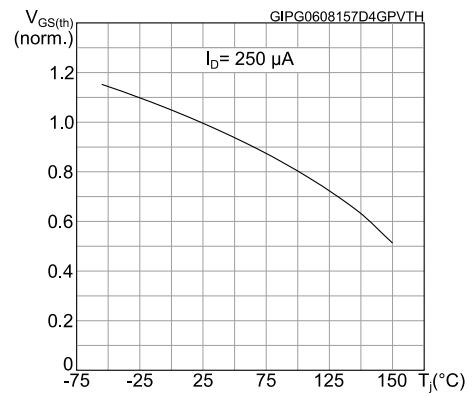


Figure 10: Normalized on-resistance vs temperature

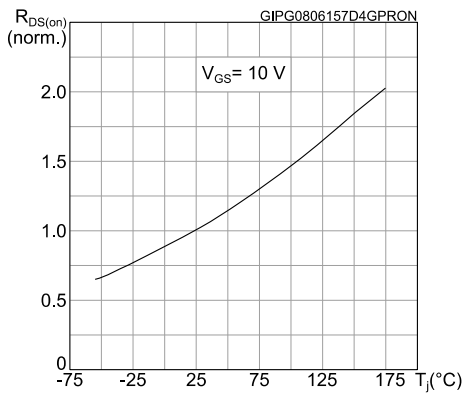


Figure 11: Normalized V(BR)DSS vs temperature

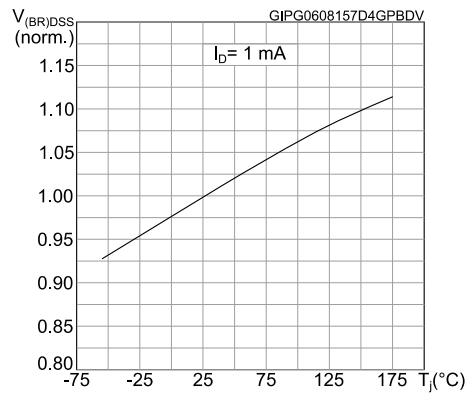
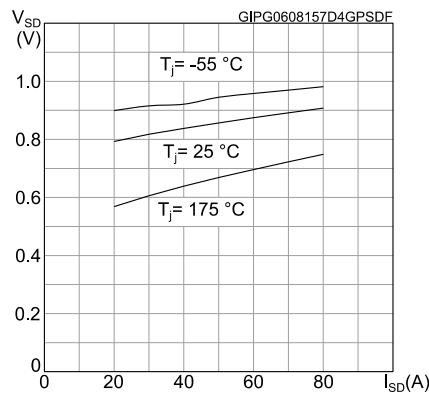
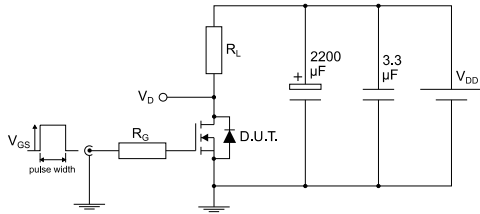


Figure 12: Source-drain diode forward characteristics



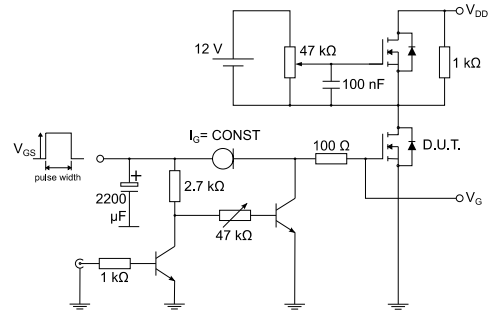
3 Test circuits

Figure 13: Test circuit for resistive load switching times



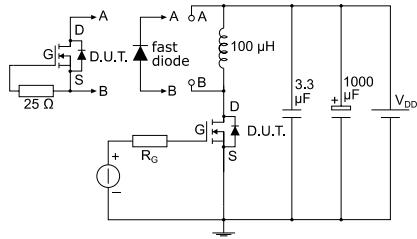
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Figure 14: Test circuit for gate charge behavior



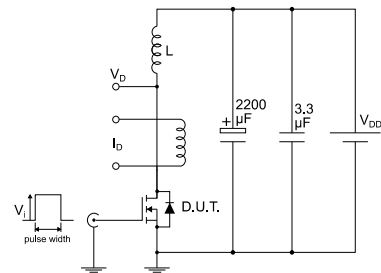
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Figure 15: Test circuit for inductive load switching and diode recovery times



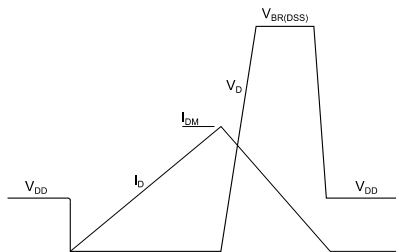
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Figure 16: Unclamped inductive load test circuit



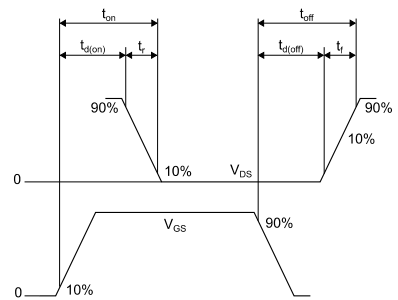
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Figure 17: Unclamped inductive waveform



AM01472v1

Figure 18: Switching time waveform



AM01473v1

4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

4.1 I²PAK package information

Figure 19: I²PAK package outline

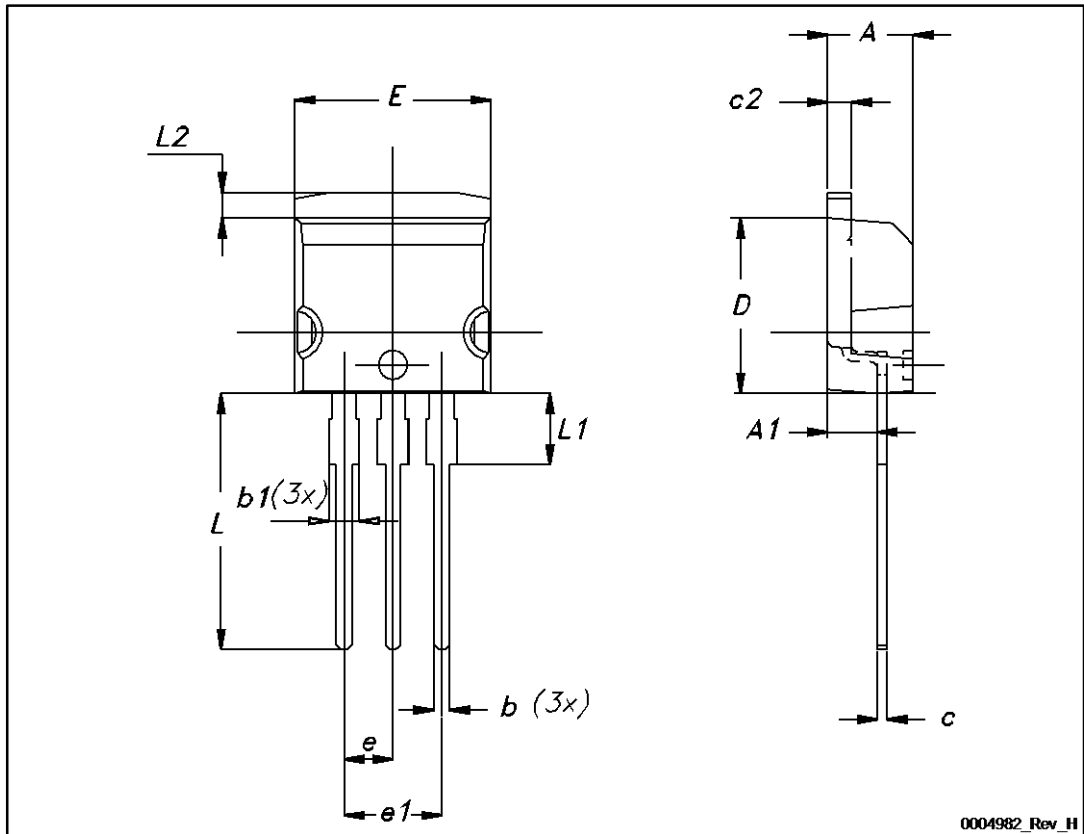


Table 8: I²PAK package mechanical data

| Dim. | mm | | |
|------|------|------|-------|
| | Min. | Typ. | Max. |
| A | 4.40 | – | 4.60 |
| A1 | 2.40 | – | 2.72 |
| b | 0.61 | – | 0.88 |
| b1 | 1.14 | – | 1.70 |
| c | 0.49 | – | 0.70 |
| c2 | 1.23 | – | 1.32 |
| D | 8.95 | – | 9.35 |
| e | 2.40 | – | 2.70 |
| e1 | 4.95 | – | 5.15 |
| E | 10 | – | 10.40 |
| L | 13 | – | 14 |
| L1 | 3.50 | – | 3.93 |
| L2 | 1.27 | – | 1.40 |

5 Revision history

Table 9: Document revision history

| Date | Revision | Changes |
|-------------|----------|----------------|
| 26-Jan-2016 | 1 | First release. |

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