

N-channel 250 V 0.14 Ω typ., 17 A low gate charge STripFET™ II Power MOSFET in a I²PAK package

Datasheet — production data

Features

Order code	V _{DSS}	R _{DS(on)} max.	I _D	P _{TOT}
STI17NF25	250V	< 0.165 Ω	17A	90W

- Low gate charge
- 100% avalanche tested
- Exceptional dv/dt capability

Application

- Switching applications

Description

This Power MOSFET has been developed using STMicroelectronics' unique STripFET process, which is specifically designed to minimize input capacitance and gate charge. This renders the devices suitable for use as primary switch in advanced high-efficiency isolated DC-DC converters for telecom and computer applications, and applications with low gate charge driving requirements.

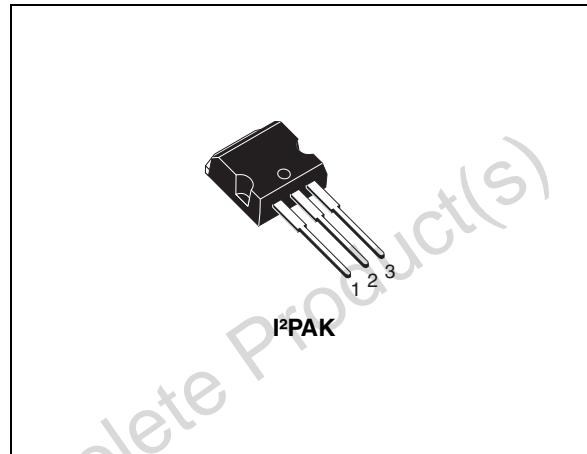


Figure 1. Internal schematic diagram

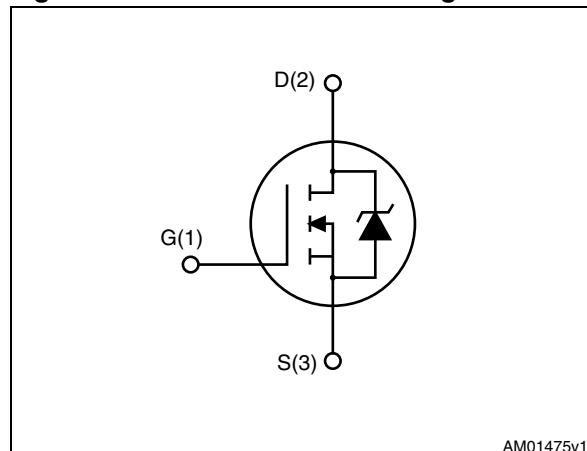


Table 1. Device summary

Order code	Marking	Package	Packaging
STI17NF25	17NF25	I ² PAK	Tube

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1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage	250	V
V_{GS}	Gate-source voltage	± 20	V
I_D	Drain current (continuous) at $T_C = 25^\circ\text{C}$	17	A
I_D	Drain current (continuous) at $T_C = 100^\circ\text{C}$	10	A
$I_{DM}^{(1)}$	Drain current (pulsed)	68	A
P_{TOT}	Total dissipation at $T_C = 25^\circ\text{C}$	90	W
	Derating factor	0.72	W/ $^\circ\text{C}$
$dv/dt^{(2)}$	Peak diode recovery voltage slope	10	V/ns
T_J T_{stg}	Operating junction temperature Storage temperature	-55 to 150	$^\circ\text{C}$

1. Pulse width limited by safe operating area
2. $I_{SD} \leq 17$ A, $dI/dt \leq 200$ A/ μs , $V_{DD} \leq 80\%V_{(BR)DSS}$

Table 3. Thermal data

Symbol	Parameter	Value	Unit
$R_{thj-case}$	Thermal resistance junction-case max	1.38	$^\circ\text{C}/\text{W}$
$R_{thj-amb}$	Thermal resistance junction-ambient max	62.5	$^\circ\text{C}/\text{W}$

Table 4. Avalanche data

Symbol	Parameter	Value	Unit
I_{AR}	Avalanche current, repetitive or not repetitive (pulse width limited by T_{jmax})	17	A
E_{AS}	Single pulse avalanche energy (starting $T_j=25^\circ\text{C}$, $I_D=I_{AR}$, $V_{DD}=50$ V)	100	mJ

2 Electrical characteristics

($T_{CASE}=25^{\circ}\text{C}$ unless otherwise specified)

Table 5. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$I_D = 1\text{mA}$, $V_{GS} = 0$	250			V
I_{DSS}	Zero gate voltage drain current ($V_{GS} = 0$)	$V_{DS} = 250\text{ V}$, $V_{DS} = 250\text{ V}, T_c = 125^{\circ}\text{C}$		1 10	μA μA	
I_{GSS}	Gate body leakage current ($V_{DS} = 0$)	$V_{GS} = \pm 20\text{V}$			± 100	nA
$V_{GS(\text{th})}$	Gate threshold voltage	$V_{DS} = V_{GS}$, $I_D = 250\text{ }\mu\text{A}$	2	3	4	V
$R_{DS(\text{on})}$	Static drain-source on resistance	$V_{GS} = 10\text{ V}$, $I_D = 8.5\text{ A}$		0.14	0.165	Ω

Table 6. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss} C_{oss} C_{rss}	Input capacitance Output capacitance Reverse transfer capacitance	$V_{DS} = 25\text{ V}$, $f = 1\text{ MHz}$, $V_{GS} = 0$	-	1000 178 28	-	pF pF pF
$C_{oss\text{ eq}}$	Equivalent output capacitance	$V_{GS} = 0$, $V_{DS} = 0$ to 200 V	-	135	-	pF
Q_g Q_{gs} Q_{gd}	Total gate charge Gate-source charge Gate-drain charge	$V_{DD} = 200\text{ V}$, $I_D = 17\text{ A}$ $V_{GS} = 10\text{ V}$ (see Figure 15)	-	29.5 4.8 15.6	-	nC nC nC
R_G	Gate input resistance	$f = 1\text{ MHz}$ gate DC bias = 0 test signal level = 20 mV open drain	-	2	-	Ω

Table 7. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$ t_r	Turn-on delay time Rise time	$V_{DD}=125\text{ V}$, $I_D=8.5\text{ A}$, $R_G=4.7\Omega$, $V_{GS}=10\text{ V}$ (see Figure 14)	-	8.8 17.2	-	ns ns
$t_{d(off)}$ t_f	Turn-off delay time Fall time	$V_{DD}=125\text{V}$, $I_D=8.5\text{A}$, $R_G=4.7\Omega$, $V_{GS}=10\text{V}$ (see Figure 14)	-	21 8.8	-	ns ns

Table 8. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD} $I_{SDM}^{(1)}$	Source-drain current Source-drain current (pulsed)		-		17 68	A A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD}=17\text{ A}$, $V_{GS}=0$	-		1.6	V
t_{rr} Q_{rr} I_{RRM}	Reverse recovery time Reverse recovery charge Reverse recovery current	$I_{SD} = 17\text{ A}$, $dI/dt = 100\text{ A}/\mu\text{s}$, $V_{DD} = 50\text{ V}$ (see Figure 16)	-	157 0.91 11.6		ns μC A
t_{rr} Q_{rr} I_{RRM}	Reverse recovery time Reverse recovery charge Reverse recovery current	$I_{SD} = 17\text{ A}$, $dI/dt = 100\text{ A}/\mu\text{s}$, $V_{DD} = 50\text{ V}$, $T_j=150\text{ }^\circ\text{C}$ (see Figure 16)	-	196 1.34 13.7		ns μC A

1. Pulse width limited by safe operating area
2. Pulsed: pulse duration=300 μs , duty cycle 1.5%

2.1 Electrical characteristics (curves)

Figure 2. Safe operating area

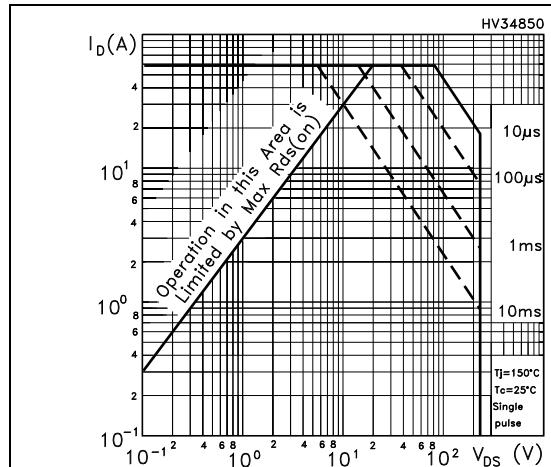


Figure 3. Thermal impedance

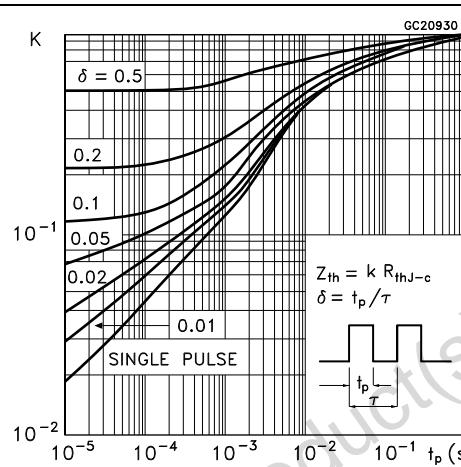


Figure 4. Output characteristics

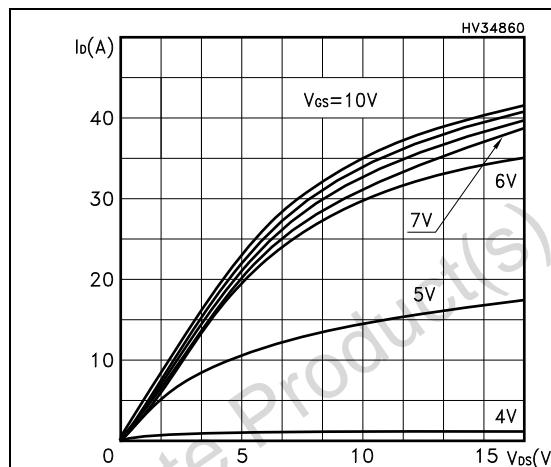


Figure 5. Transfer characteristics

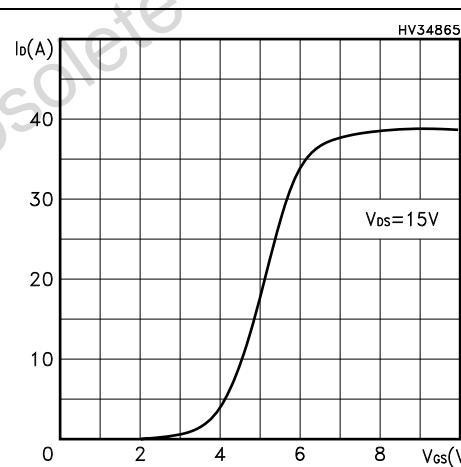
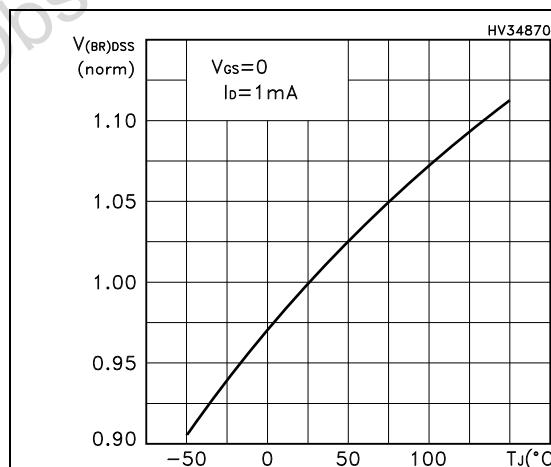
Figure 6. Normalized BV_{DSS} vs temperature

Figure 7. Static drain-source on resistance

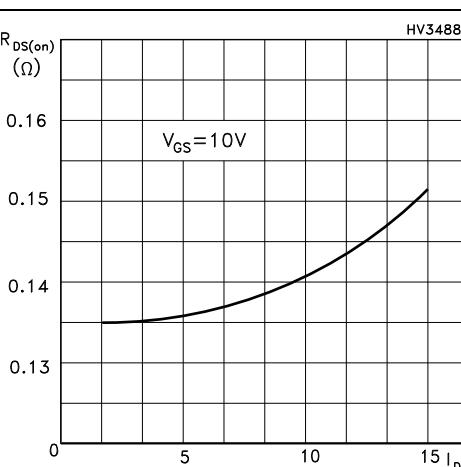
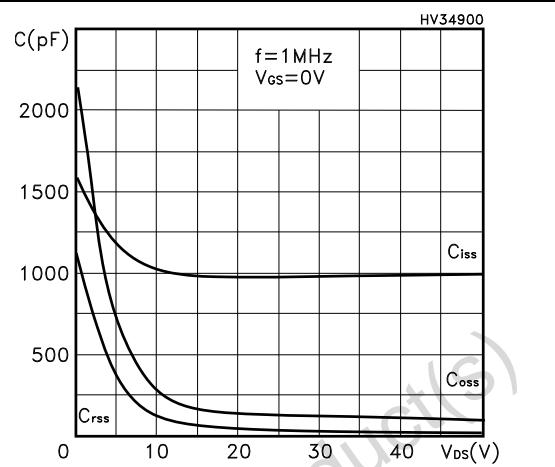
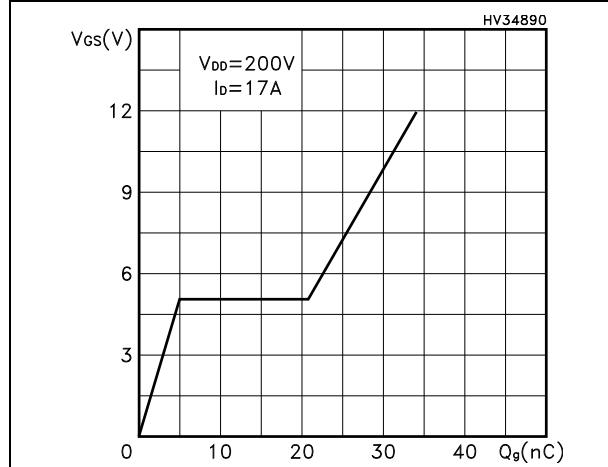
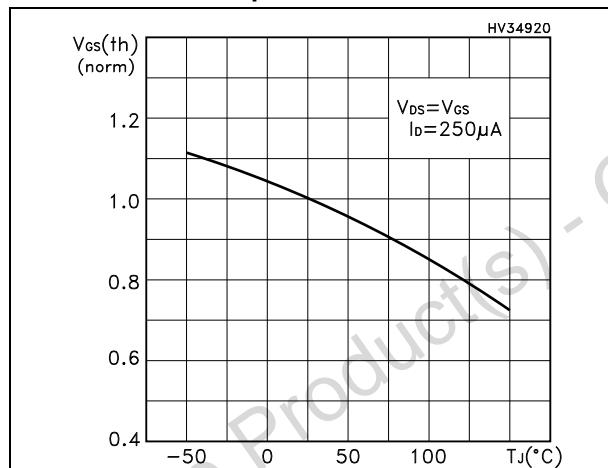
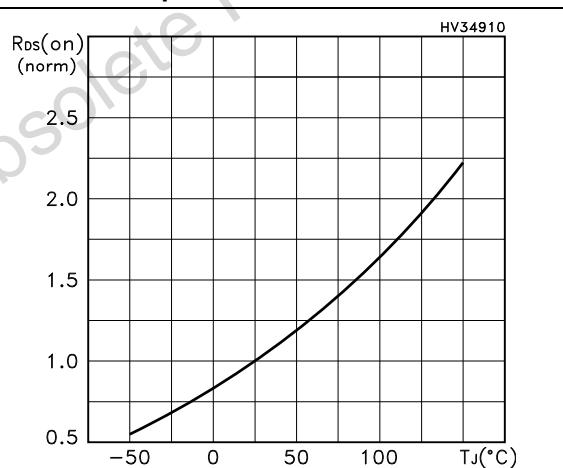
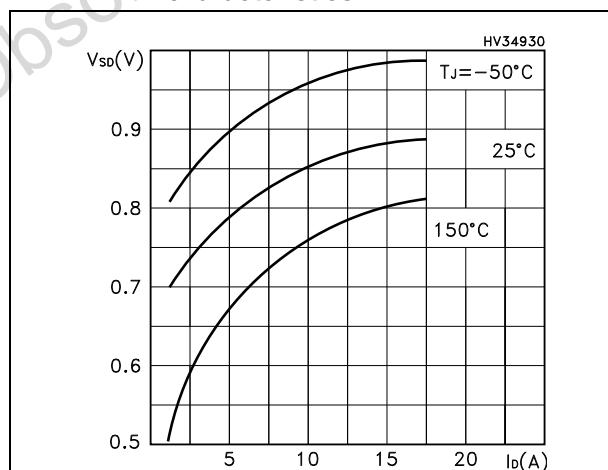
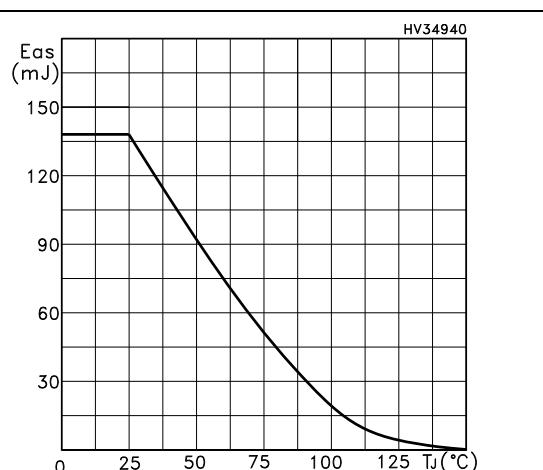


Figure 8. Gate charge vs gate-source voltage**Figure 10. Normalized gate threshold voltage vs temperature****Figure 11. Normalized on resistance vs temperature****Figure 12. Source-drain diode forward characteristics****Figure 13. Maximum avalanche energy**

3 Test circuits

Figure 14. Switching times test circuit for resistive load

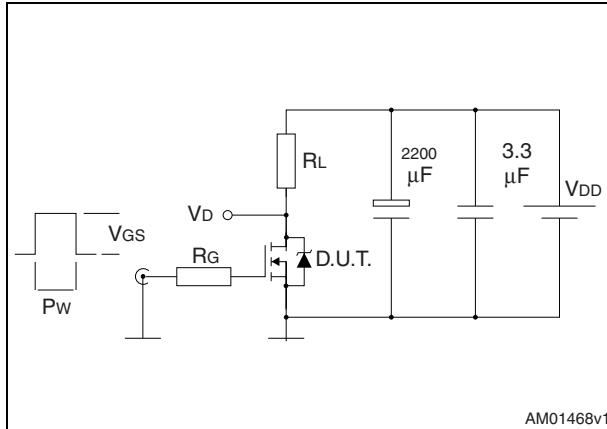


Figure 15. Gate charge test circuit

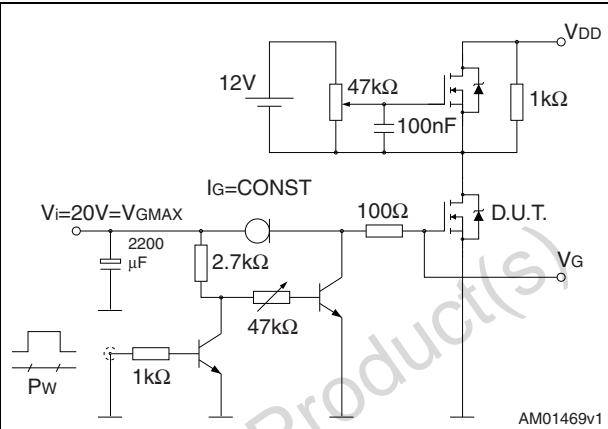


Figure 16. Test circuit for inductive load switching and diode recovery times

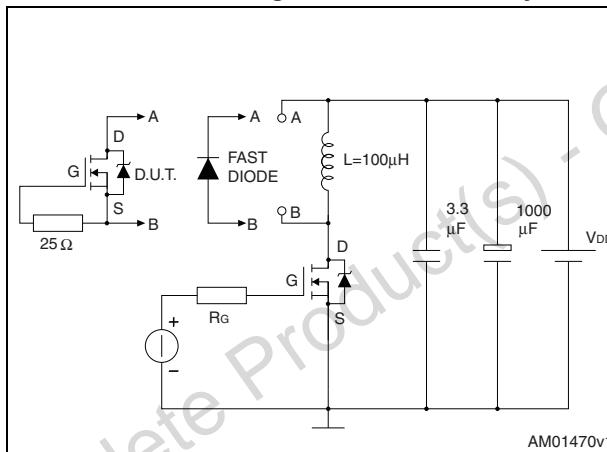


Figure 17. Unclamped Inductive load test circuit

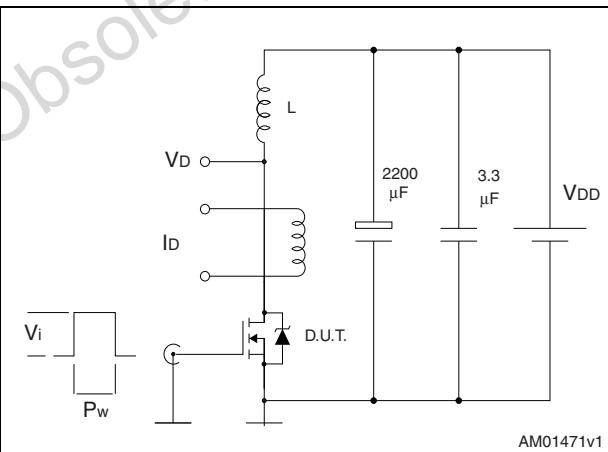


Figure 18. Unclamped inductive waveform

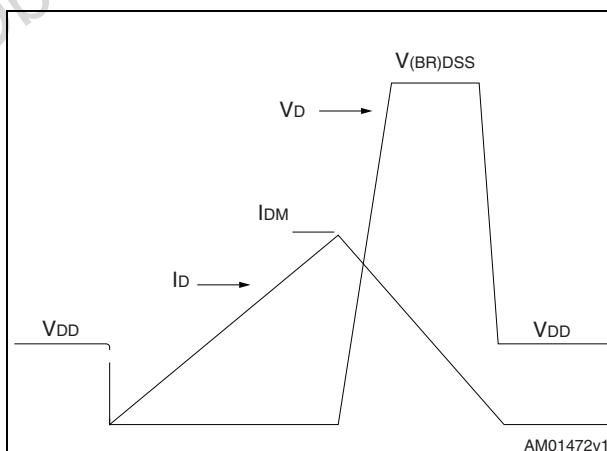
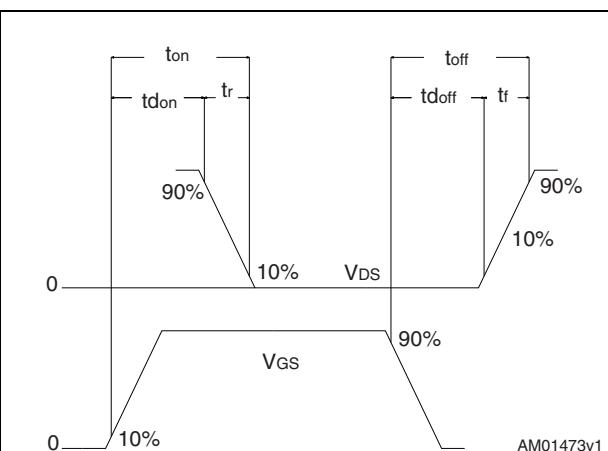


Figure 19. Switching time waveform

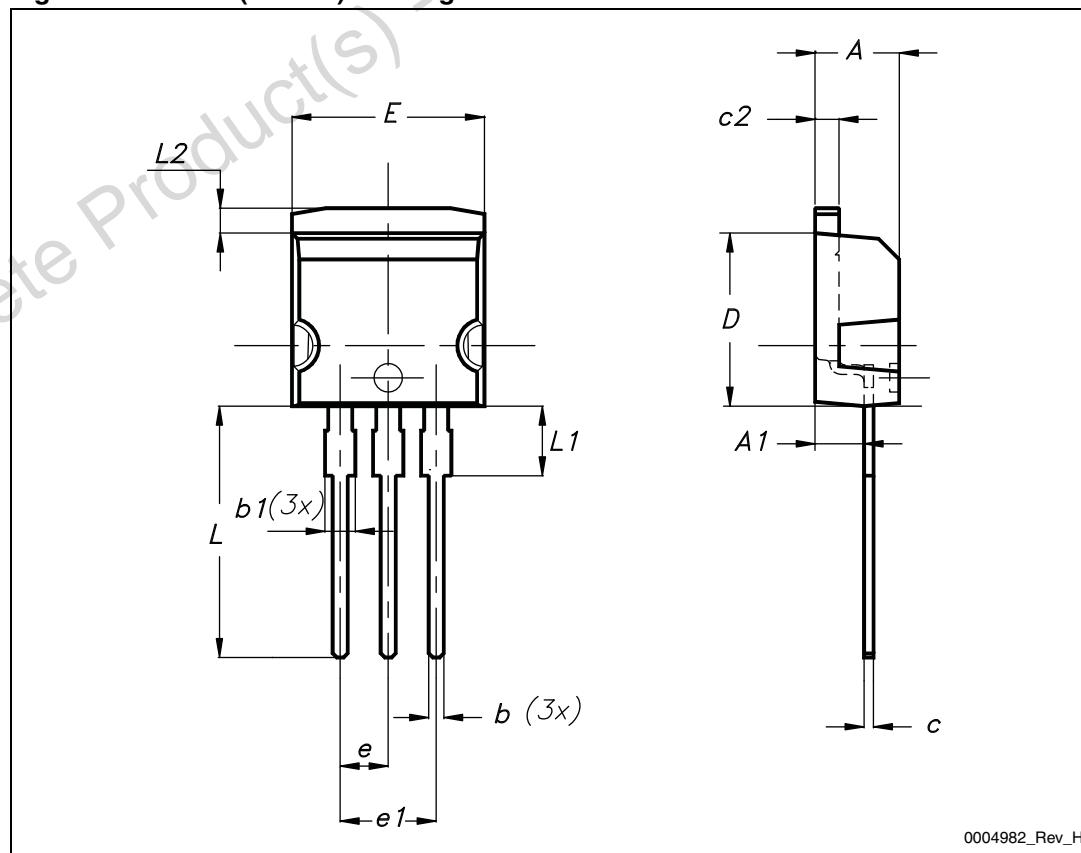


4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com.
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Table 9. I²PAK (TO-262) mechanical data

DIM.	mm.		
	min.	typ	max.
A	4.40		4.60
A1	2.40		2.72
b	0.61		0.88
b1	1.14		1.70
c	0.49		0.70
c2	1.23		1.32
D	8.95		9.35
e	2.40		2.70
e1	4.95		5.15
E	10		10.40
L	13		14
L1	3.50		3.93
L2	1.27		1.40

Figure 20. I²PAK (TO-262) drawing

5 Revision history

Table 10. Document revision history

Date	Revision	Changes
19-Dec-2012	1	First release. Part number previously included in datasheet CD00150910

Obsolete Product(s) - Obsolete Product(s)

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