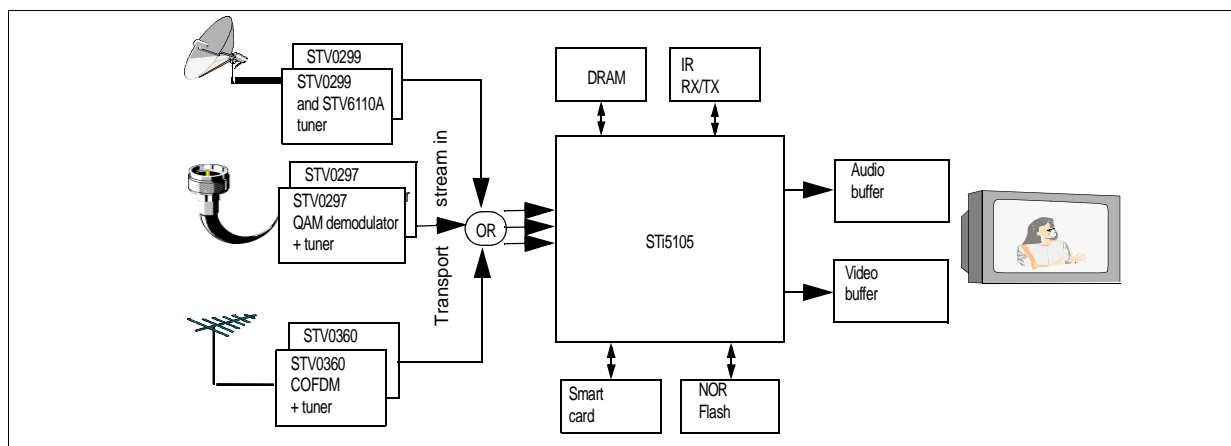


High-performance advanced SD decoder for set-top box

Data Brief

Features

- Enhanced ST20 32-bit VL-RISC CPU
 - 200 MHz, single cycle cache, 4 Kbyte instruction cache, 4 Kbyte data cache, 2 Kbyte SRAM
- Unified memory interface
 - Up to 133 MHz, 16-bit wide DDR interface
- Programmable flash memory interface
 - SRAM, peripheral, Flash, SFlash™ support
 - Support for low-cost DVB-CI and ATAPI
- Programmable transport interface (PTI)
 - Single transport stream input
 - Support for DVB transport streams
 - Integrated DVB, ICAM descramblers
- MPEG-2 MP@ML video decoder
 - Fully programmable horizontal and vertical SRCs
- Graphics/display
 - Advanced blitter base compositor
 - 8 bpp CLUT graphics, 256 x 30 bits (AYCbCr) CLUT entries
 - 16 bpp true color graphics, RGB565, ARGB1555, ARGB4444 formats with link-list control
 - Alpha blending, antialiasing, antiflutter, antiflicker filters
 - 2D paced blitter engine with fill function
- PAL/NTSC/SECAM encoder
 - RGB, CVBS, Y/C and YUV outputs with four 10-bit DAC outputs. RGB/CVBS or YUV/CVBS or YC/CVBS
 - Encoding of CGMS, Teletext, WSS, VPS, close caption
- Audio subsystem
 - MPEG-1 layers I/II
 - Simultaneous MPEG audio decode and output of Dolby streams on S/PDIF
 - IEC958/IEC1937 digital audio output interface
 - Integrated stereo audio DAC system
- Central DMA controller
- On-chip peripherals
 - Two ASCs (UARTs) with Tx and Rx FIFOs
 - Three 8-bit banks of parallel I/O and one 7-bit bank
 - One smartcard interface and clock generator
 - Two SSCs for I²C/SPI master/slave interfaces
 - Infrared transmitter/receiver
 - Integrated VCXO
 - Low-power/RTC/watchdog controller
- JTAG/TAP interface
- Package 24 mm x 24 mm LQFP216 or 23 mm x 23 mm BGA.



1 Description

STMicroelectronics sets a new standard for performance, price and integration in the single chip MPEG-2 set-top box decoder market with the introduction of the STi5105.

This highly integrated solution targets mass market STBs, offers increased performance over earlier devices, and includes many features to further reduce costs, including a unified memory architecture.

The STi5105 features the ST20 CPU that is standard across the OMEGA range but boosts the clock speed to 200 MHz which, when combined with the 2D graphics engine, gives the new device outstanding graphics performances.

Targeting low-cost, single tuner STB applications, the STi5105's DDR memory interface both reduces system costs and minimizes overall system latency, ensuring the new device can support the most demanding interactive TV applications and middlewares.

The integration of VCXO and audio DACs ensures that manufacturers using the STi5105 cut their bill of materials and significantly simplify board design and assembly.

STi5105 is supplied in either 24 mm x 24 mm LQFP216 or 23 mm x 23 mm BGA package.

2 Ordering information

Table 1. Ordering information

Order code	Packaging
STi5105ALC	24 mm x 24 mm LQFP216
STi5105AYC	23 mm x 23 mm BGA

3 Revision history

Table 2. Document revision history

Date	Revision	Changes
24-Nov-08	1	Initial release

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