Data Sheet

by

SYNTEK®

==========STK1160==========

USB2.0 TV Tuner/Video Capture Controller

Version 1.2

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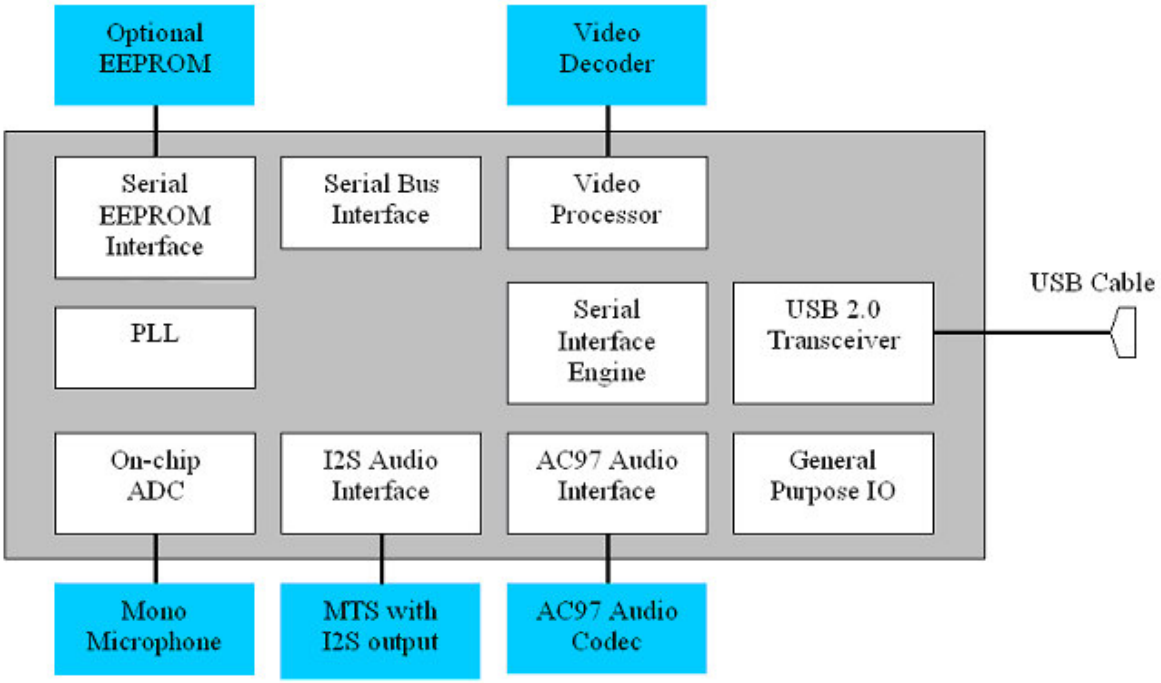
1 Product Overview

STK1160 is a highly integrated, single chip high-speed USB 2.0 compliant digital video imaging controller. Utilizing a high-speed, high-bandwidth isochronous pipe, it is able to transfer ITU-R 656 or ITU-R 601 format NTSC/PAL/SECAM video. It also provides 16-bit stereo audio stream through another USB 2.0 isochronous pipe.

STK1160 supports a wide range of video decoders, TV tuners, and demodulators. The device also provides AC97 and I2S interfaces for external stereo audio codec or uses an integrated low-cost 8-bit mono ADC.

2 Functional Block Diagram



3 Product Features

3.1 Video Stream Interface

- Support 8-bit ITU-R 656 interface standard, and compliance with 10-bit video inputs.
- Support 8-bit ITU-R 601 interface standard, and compliance with 10-bit video inputs.
- Support hardware windowing and decimation.

3.2 Serial Bus Interfaces

- Support a serial communication to video decoders, demodulators, and TV tuners.
- Support a serial communication to optional remote controller.
- Support a serial communication to optional serial EEPROM.
- Support 2-wire or 3-wire serial communications.

3.3 Integrated Hi-Speed USB 2.0 Transceiver

- High-speed USB 2.0 and USB 1.1 full-speed functionality
- USB composite device with video and audio interfaces
- USB 2.0 isochronous video pipe can transfer up to 24 MB/sec
- USB 2.0 isochronous audio pipe can transfer up to 192 KB/sec
- Vendor ID, product IDs and string descriptors can be stored in an external serial EEPROM

3.4 Audio Interface

- Integrated on-chip ADC supports 8-bit mono audio recording at 8 KHz sampling rate.
- AC97 interface supports 16-bit stereo audio recording at 48/32 KHz sampling rate.
- I2S interface supports 16-bit stereo audio recording at 48/32 KHz sampling rate.
- Audio data is in PCM audio format
- Audio device is USB audio class compliant

3.5 General Purpose Input/Output Interface

- 10 general purpose input/output pins

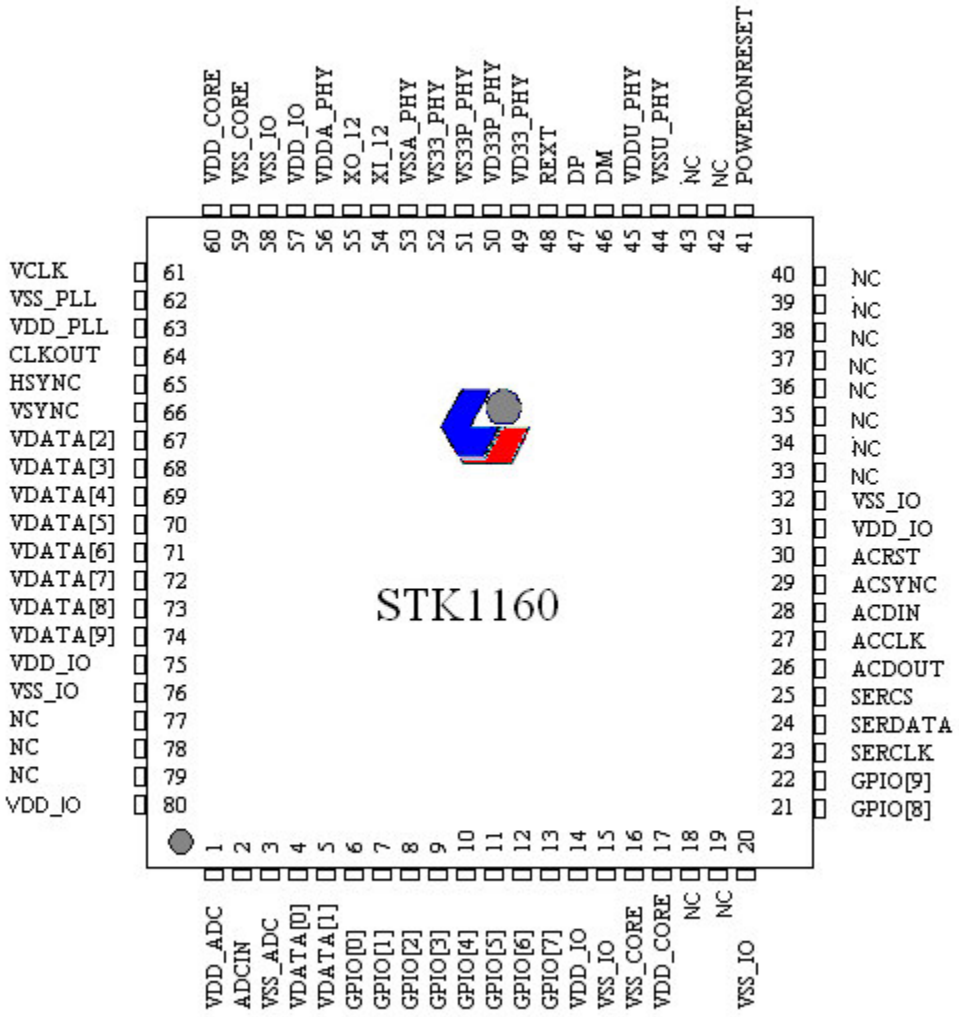
3.6 Power Management

- 1.8V power supply voltage for chip core.
- 1.8V and 3.3V power supply voltage for on-chip USB transceiver.
- 1.8V power supply voltage for on-chip PLL.
- 3.3V power supply voltage for IO.
- 3.3V power supply voltage for on-chip ADC.
- Supports advance power down mechanism.

3.7 Other Features

- Supports all test modes defined in the USB 2.0 specification
- 80-pin LQFP package

4 Pin Diagram

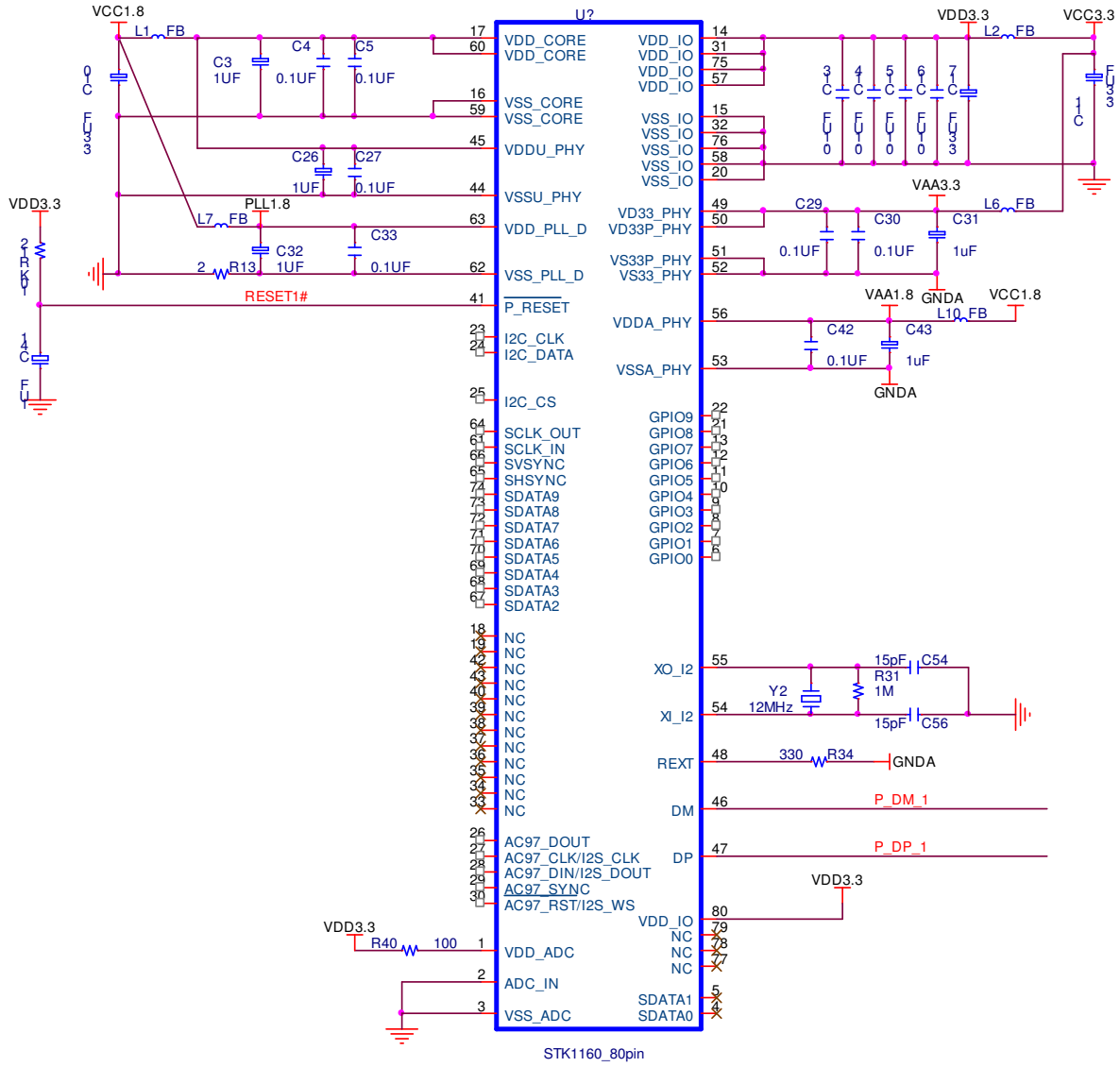


4.1 Pin Descriptions

Pin#	Name	Dir	Pull	Active	Description
4-5	VDATA[0]-[1]	I	PD		**Video Decoder data input**
67-74	VDATA[2]-[9]	I	PD		**Video Decoder data input** For 8-bit video data interface, use VDATA [2]-[9].
61	VCLK	I	PD		**Video Decoder clock input**
64	CLKOUT	O	PD		**Video Decoder clock output**
65	HSYNC	I/O	PD		**Horizontal Sync signal**
66	VSYNC	I/O	PD		**Vertical Sync signal**
23	SERCLK	O			**Serial bus clock**
24	SERDATA	I/O			**Serial bus data**
25	SERCS	O	PD	H	**Serial bus chip select**
6	GPIO[0]	I/O	PD		**General purpose I/O 0** If 93C46 serial ROM is present, this pin is used for Clock (SK) signal.
7	GPIO[1]	I/O	PD		**General purpose I/O 1** If 93C46 serial ROM is present, this pin is used for Data (DIO) signal.
8	GPIO[2]	I/O	PD		**General purpose I/O 2** If 93C46 serial ROM is present, this pin is used for Chip Select (CS) signal.
9	GPIO[3]	I/O	PD		**General purpose I/O 3**
10	GPIO[4]	I/O	PD		**General purpose I/O 4**
11	GPIO[5]	I/O	PD		**General purpose I/O 5**
12	GPIO[6]	I/O	PU		**General purpose I/O 6**
13	GPIO[7]	I/O	PD		**General purpose I/O 7** If video source does not always output valid data, this pin can be used as data valid signal when VVLD register is enabled. “High” indicates the data is valid and “Low” indicates the data is invalid.
21-22	GPIO[8]-GPIO[9]	I/O			**General purpose I/O 8-9**
2	ADCIN	I			**Audio analog input** from microphone
26	ACDOUT	O	PD		**AC97 serial data out**
27	ACCLK	I	PD		**AC97 clock in / I2S clock in**
28	ACDIN	I	PD		**AC97 serial data in / I2S data in**
29	ACSYNC	O	PD	H	**AC97 Sync**
30	ACRST	I/O	PD	L	**AC97 reset out / I2S left/right channel in**
54	XI_12	I			**12 MHz oscillator input** to internal transceiver
55	XO_12	O			**12 MHz oscillator output** to crystal
41	POWERONRESET	I		L	**Power On Reset** Active low power on reset signal
77-79, 18,19, 33-40, 42,43	NC	I	PD		
46	DM	I/O			**USB D minus line**
47	DP	I/O			**USB D plus line**
48	REXT	I			Connect 330 ohm resistor to ground.

56	VDDA_PHY	I			1.8V supply for internal transceiver analog circuit
53	VSSA_PHY	I			Ground for internal transceiver analog circuit
50	VD33P_PHY	I			3.3V supply for internal transceiver
51	VS33P_PHY	I			Ground for internal transceiver
49	VD33_PHY	I			3.3V supply for internal transceiver
52	VS33_PHY	I			Ground for internal transceiver
45	VDDU_PHY	I			1.8V supply for internal transceiver digital circuit
44	VSSU_PHY	I			Ground for internal transceiver digital circuit
1	VDD_ADC	I			3.3V supply for ADC
3	VSS_ADC	I			Ground for ADC
63	VDD_PLL	I			1.8V supply for PLL
62	VSS_PLL	I			Ground for PLL
14, 31, 57, 75, 80	VDD_IO	I			3.3V supply for IO
15, 20, 32, 58, 76	VSS_IO	I			Ground for IO
17, 60	VDD_CORE	I			1.8V supply for core
16, 59	VSS_CORE	I			Ground for core

5 Typical Pin Connection Diagram



6 Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Power supply voltage for I/O	V_{DD33}	-0.5 to +4.6	V
Power supply voltage for core	V_{DD}	-0.5 to +2.5	V
Input voltage	V_I	-0.5 to +6	V
Output voltage	V_O	-0.5 to +4.6	V
Operating temperature range	T_{OPT}	-40 to +125	°C
Storage temperature range	T_{STG}	-65 to +150	°C

7 Electrical Characteristics

(Under the condition of V_{DD}=1.8V, V_{DD33}=3.3V, T_{OPT}=25°C if not specified.)

Parameter	Symbol	Min	Typ	Max	Unit
Power supply voltage for I/O	V_{DD33}	2.97	3.3	3.63	V
Power supply voltage for core	V_{DD}	1.62	1.8	1.98	V
Operation current of V_{DD33} (ATV)	I_{DD33}		29		mA
Operation current of V_{DD} (ATV)	I_{DD}		38		mA
Suspend current of V_{DD33}	I_{S33}		400		µA
Suspend current of V_{DD}	I_S		80		µA
Input high voltage	V_{IH}	1.5		5.5	V
Input low voltage	V_{IL}	-0.3		1.2	V
Input leakage current	I_L			±10	µA
Tri-state output leakage current	I_{OZ}			±10	µA
Pull up resistor	R_{PU}	39	65	116	Kohm
Pull down resistor	R_{PD}	40	56	108	Kohm
Input capacitance	C_{IN}			TBD	pF
Output capacitance	C_{OUT}			TBD	pF
Output high voltage @I_{OH}=8mA	V_{OH}	2.4			V
Output low voltage @I_{OL}=8mA	V_{OL}			0.4	V
Output high current @V_{OH}=2.4V	I_{OH}	11.1	23.4	37.3	mA
Output low current @V_{OL}=0.4V	I_{OL}	9.4	15.8	19.8	mA

8 Functional Descriptions

STK1160 comprises several major functional blocks.

- The power-on strapping block latches the power-on values from some of the pins so that the chip can get optional values from these pins.
- The GPIO block provides an interface to switches, buttons, and other input devices as well as a way to control external devices such as LEDs. In conjunction with the USB block, the GPIO block provides interrupt and remote wakeup functions.
- The video-processing block receives data from the video decoders and stores the data in a FIFO prior to transmission on USB.
- The serial bus interface links the peripheral devices to STK1160 so that the device driver can send commands to the peripheral devices.
- The programmable timing generator creates clock output and the timing to programmable serial interface block for decoder/demodulator/tuner configuration and control.
- The audio block takes an analog input signal, converts it to 8-bit 8K Hz PCM stream and places it into an audio FIFO.
- The AC97/I2S interface block receives digital audio data at 48K or 32K sampling rate from an external audio codec and places it in a FIFO before isochronous transfer.
- External EEPROM interface block makes the chip to get the customized information from the external EEPROM, and reports to the USB host.
- The USB block transmits data streams to a USB host and performs other USB-required functions.

Some additional miscellaneous functions are provided and will be described below.

8.1 Power-On Strapping

To configure STK1160, the power-on-strapping options are used. The strap pins have weak internal pull-ups or pull-downs. To override the internal values, an external 10K Ohm resistor should be used. The strap options are:

Strap Name	**Strap Pin**	**Default Pull Direction**	**Description (External Pull)**	**Register 10-12 Bit #**
Audio Control	ACDOUT	Low	Pull Low: Audio function is enabled. Pull High: Audio function is disabled. The corresponding audio descriptor will not be reported.	10b3
Audio Type	ACSYNC	Low	Pull Low: Audio data comes from AC97 or I2S codec (16 bit PCM @48K sample rate). Pull High: Audio data comes from internal ADC (8 bit PCM @8K sample rate).	10b2
Audio Sample	ACRST	Low	Pull Low: 16 bit PCM @48K sample rate from AC97 or I2S codec. Pull High: 16 bit PCM @32K sample rate from AC97 or I2S codec.	10b1
Audio Driver Type	GPIO[1]	Low	Pull Low: Use Microsoft USB audio class driver. Pull High: Use Syntek proprietary audio driver.	11b7
Serial ROM	{GPIO[2], GPIO[0]}	{Low, Low}	00: No external serial EEPROM is present. 01: 2 wire serial EEPROM (24C02 series) is present. (one byte sub-address) 10: 3 wire serial EEPROM (93C46) is present. 11: 2 wire serial EEPROM (24C64 series) is present. (two byte sub-address) When Serial ROM is not 00, the USB vendor, product IDs and string descriptors are read from external serial EEPROM. String descriptors stored in the EEPROM must follow the USB specification for string descriptor format. Serial number string is expected for 2 wire serial EEPROM only.	12b0, 11b6
Self Power	GPIO[3]	Low	Pull Low: To indicate non self-powered device.	12b1

			Pull high: To indicate self-powered device.	
Remote Wakeup	GPIO[4]	Low	Pull Low: Remote wakeup is disabled. Pull High: Remote wakeup is enabled.	12b2

8.2 General Purpose I/O

The GPIO registers define and control the functions of 10 General Purpose I/O pins. Through these registers, any of the GPIO pins can be used as user-defined I/O pins, Interrupt input pins, or Remote Wakeup input pins.

The 10 GPIO pins can be defined with individual direction control, and written to as output function or read from as input function. The Interrupts to the USB host are generated based on the value of the GPIO pins when they are configured as interrupt function. Interrupt active polarity can be set individually for each pin and interrupt for each pin can be individually enabled. The interrupt word sent to the USB host indicates the GPIO pins that are currently generating an interrupt with 1 bit regardless of the polarity set for that pin. Thus, a pin is enabled for an interrupt and will be indicated as active to the USB host with a 1 in its corresponding bit in the interrupt word. Remote wakeup to the USB host is generated in the same way as interrupts but controlled by separate 10-bit enable and polarity registers.

Interrupts in the STK1160 are based on levels and not edges. An unmasked and active interrupt bit will cause data to be returned on the USB interrupt pipe until the mask bit is cleared or the bit ceases to be active.

8.2.1 Registers

GCTRL GPIO Control

Read/Write **000H**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ROMD (0)	Reserved (0,0000)					GDIR (00,0000,0000)									

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved (00,0000)						GV (00,0000,0000)									

ROMD [31] – EEPROM Disable

When EEPROM is present, this register is to disable the EEPROM interface. The write to EEPROM cannot be successful when the EEPROM interface is disabled.

0	EEPROM interface is enabled when EEPROM is present.
1	EEPROM interface is disabled.

RVD [30:26] – Reserved

GDIR [25:16] – GPIO Direction

Setting 1 to one of these bits enables the corresponding GPIO pin as an output.

RVD [15:10] - Reserved

GV [9:0] – GPIO Value

A write to these bits sets the output value to the corresponding GPIO pins. A read from these bits returns the value present on the corresponding GPIO pin whether that pin is currently an input or an output.

RMCTL Remote Wakeup Control

Read/Write **00CH**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved (00,0000)						RWC (10,0000,0000)									

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved (00,0000)						RWP (00,0000,0000)									

RVD [31:26] – Reserved

RWC [25:16] – Remote Wakeup Control

Setting 1 enables USB remote wakeup for corresponding GPIO. Set 0 to disable.

RVD [15:10] – Reserved

RWP [9:0] – Remote Wakeup Polarity

This value sets the polarity to trigger USB remote wakeup.

POSVA Power-on Strapping Data

Read only **010H**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RVS (1000,0101)								Reserved (00)		POSV (x0,0000)					

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
POSV (0000,0001)															

RVS [31:24] –Reserved

Chip revision number

RVD [23:22] – Reserved

POSV [21:0] – Power-On Strap Value

This register latches the power-on strapping value during reset.

Please refer to power-on strapping section for detailed information.

8.3 Video Processor

The video capture takes 8-bit ITU-R 656 or ITU-R 601 YUV 4:2:2 data from an external video decoder or other video sources. The capture pixel clock and 8-bit format engine optionally receives horizontal and vertical synchronization signals as well as stores the data into a FIFO after performing any required windowing and decimation.

The video capture has the FIFO control logic and sends status signals to the USB block, telling it if data are ready in the FIFO and how many full packets of data are ready to be sent. The information about the number of full packets is used by the USB block to determine the data toggle to be used for the first isochronous packet in a microframe.

The capture window is programmable. The total number of rows and columns captured must both be multiples of four. The starting row and column can be arbitrarily chosen.

There is also the decimation logic for the incoming data to reduce the amount of data transferred to the USB host. Decimation operates independently in the horizontal and vertical directions, with separate enable and count registers for each direction. In addition to enable and count registers, there is a register bit that specifies whether decimation is to be more or less than half of the original image size. If the number of columns or rows to be decimated is less than half the total number of incoming columns or rows, the count register value is interpreted as the number of columns or rows to be sent for each column or row skipped. If equal or greater than half the incoming image size, the value is interpreted as the number of columns or rows to be skipped for each column or row sent.

Depending on the data format, decimation can work with a unit that consists of either two or four rows and columns at a time. The decimation count register counts the number of units regardless of whether the unit consists of two or four rows and columns.

The image capture clock can either come from the internal timing generator or an external clock source. There is also a register bit to control whether the clock is phase-inverted before it is fed to the image capture block. When the video decoder clock is sourced by STK1160, the trace delay to and from the video decoder may cause inadequate setup time to the data. The phase inversion can improve the setup time for the data from video decoder. See Timing Generator Section for details.

8.3.1 Registers

DCTRL Decoder Control Register

Read/Write **100H**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved (0000,0000)							VBI (0)	RVD (0000,0000)							

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SBFDC (0000)				SBFC (0)	Reserved (000)			VPCC (0)	VPTD (0)	DBW (0)	ITU656 (0)	VVLD (0)	DTSP (000)		

RVD [31:25] - Reserved

VBI [24] – VBI Mode

This register is used to turn the VBI mode on. During the VBI mode, STK1160 will capture data in the active horizontal window during vertical blanking interval in addition to the data in the active video window.

0	VBI mode is disabled
1	VBI mode is enabled

FDC [23:16] – Reserved

SBFDC [15:12] - Serial Bus Frame Decimation Count–

This register specifies the serial bus frame decimation count.

SBFC [11] – Serial Bus Frame Decimation Control

When this register is set, the frames will be dropped after a write command to the serial bus. The number of dropped frames is specified in SBFDC.

0	Serial bus frame decimation is disabled.
1	Serial bus frame decimation is enabled.

FDU [10:8] – Reserved

VPCC [7] – Video Processor Capture Control

0	*Default;* Disable
1	Run

VPTD [6] – Video Processor Test Data

0	Send data from video decoder input.
1	If set, data is sent from a 16-bit counter that increments every time the control signals from an external source indicate valid data. This counter is reset at the start of every video frame.

DBW [5] - Data Byte or Word

0	10 bit data (SDATA[9:0])
1	8 bit data (SDATA[9:2])

ITU 656 [4] – ITU 656 Data Input

0	Disabled, data is in ITU 601 format
1	Enabled, data is in ITU 656 format

VVLD [3] – Video Valid

This bit is to identify if the video source is sending a valid signal to qualify data.
If this register is set, GPIO [7] is used as a data-valid pin connected to video source.

0	Video data is always valid.
1	Video data will be qualified with GPIO [7].

DTSP [2:0] - Decoder Type and Sync Polarity

Bits 2 1 0	Decoder Type and Sync Polarity
0 0 0	Hsync negative, Vsync negative
0 0 1	Hsync negative, Vsync positive
0 1 0	Hsync positive, Vsync negative
0 1 1	Hsync positive, Vsync positive
Others	*Reserved*

CFSPO Capture Frame Starting Position

Read/Write **110H**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved (000)			STY (0,0000,0000,0000)												

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved (000)			STX (0,0000,0000,0000)												

RVD [31:29] - Reserved

STY [28:16] – Starting Y Position

Indicate the number of vertical lines after vertical sync signal and before start of active video window.

RVD [15:13] - Reserved

STX [12:0] – Starting X Position

Indicate the number of horizontal pixels after horizontal sync signal and before start of active video window.

CFEPO Capture Frame Ending Position

Read/Write **114H**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved (000)			ENY (0,0001,1110,0000)												

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved (000)			ENX (0,0010,1000,0000)												

RVD [31:29] - Reserved

ENY [28:16] - Ending Y Position

Indicate the number of vertical lines after vertical sync signal.

RVD [15:13] - Reserved

ENX [12:0] - Ending X Position

Indicate the number of horizontal pixels after horizontal sync.

TCTRL Test Data Control

Read/Write **120H**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved (0000,0000,0000,0000)															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved (00,0000)						DDR (0)	UFTD (0)	FTD (0000,0000)							

RVD [31:10] - Reserved

DDR [9] - Delayed Data Ready

This bit is set to one to keep ready signal in pace with data for some video decoders.

UFTD [8] – Use Fixed Test Data

This bit is set to one to replace decoder input data by FTD except the last data of a video frame which is fixed to 99H.

FTD [7:0] - Fixed Test Data

Contain the fixed data for test. The LSB will be set when FIFO full.

8.4 Serial Interface

STK1160 supports a two or three-wire serial protocol for video decoder configuration and control. The protocol is programmable by the USB host to support the serial interfaces. The USB host initiates serial bus traffic via vendor-specific control transfers described in the USB interface section.

The clock used for serial communication is derived from the system clock using a programmable clock divider. Access to the bus target devices can be synchronized to the vertical blanking period. There is an eight-entry FIFO that can be loaded with write data so that multiple accesses can be performed during a single vertical blanking period. Once the vertical blanking period begins, all entries in the FIFO will be sent out even if the vertical blanking period ends before the FIFO is completely emptied.

There is a register to hold the target device address. The write FIFO has pairs of sub-address/value pairs that are sent. When loading the FIFO, data must be sent as sub-address followed by value.

In order to maintain integrity, the bus protocol supports retry on failed device ACK and also read back and retry on mismatch. These options are controlled via register bits. If both read and write accesses are initiated at the same time, the write will be performed first if it can be performed immediately. If the write is to be synchronized with the start of the vertical blanking period, the read will be performed first. Status bits are cleared when a new value is written to the control register.

For the bus protocol which needs multiple bytes of sub-address or values within a program cycle, STK1160 provides an alternate way to control the serial interface. By holding the clock, there will be no limit on the maximum bytes of read or write access.

For the three-wire bus protocol, the data sent are the sub-address and values. Data is sent from the LSB to the MSB of the serial data followed by the LSB to the MSB of the sub-address.

8.4.1 Registers

SICTL Serial Interface Control Register

Read/Write **200H**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SDA (000,0000)							RVD (0)	CD (0000,0000)							

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CWFL (000)			BS (0)	FWDA (0)	WF (0)	FRDA (0)	RF (0)	RST (0)	RR (0)	RD (0)	RB (0)	AW (0)	RW (0)	AB (0)	AI (0)

SDA [31:25] - Serial Device Address

This field holds the serial interface device address. If the power on strapping is configured to get USB IDs and strings from the 2-wire serial EEPROM, the default value will be 50H.

RVD [24] – Reserved

CD [23:16] – Clock Divider

Serial bus clock = (30MHz master clock) / (CD * 16 + 2). If the power on strapping is configured to get USB IDs and strings from the 2-wire serial EEPROM, the default valued will be 14H.

CWFL [15:13] – Current Write FIFO Length

For alternate 2-wire serial interface, these read only bits indicate current length of 4-entry FIFO.

BS [12] – Busy Status

For alternate 2-wire serial interface, this read-only bit indicates the interface is busy.

FWDA [11] – Write Failed Device ACK

This read-only bit indicates write failure due to lack of device acknowledgement. If write retry is enabled, the access will be retried. This bit set and WF clear with retry enabled indicate that write retry is still in progress. This bit set and WF clear with retry disabled indicate that the write operation has been aborted. This bit and WF both set indicate that at least one failed device ACK occurred but that retry was successful. This and all other status bits are cleared when a new value is written to the control bit.

For alternate 2-wire serial interface, this bit also indicates write failure due to lack of device acknowledgement. But there is no retry mechanism.

WF [10] – Write Finish

This read-only bit indicates that all entries in the write FIFO have been successfully sent out.

FRDA [9] – Read Failed Device ACK

This read-only bit indicates read failure due to lack of device acknowledgement. If read retry is enabled, the access will be retried. This bit set and RF clear with retry enabled indicate that read retry is still in progress. This bit set and RF clear with retry disabled indicate that the read operation has been aborted. This bit and RF both set indicate that there was at least one failed device ACK but that retry was successful.

For alternate 2-wire serial interface, this bit indicates no acknowledgement when writing the sub-address.

RF [8] – Read Finish

This read-only bit indicates read success.

RST [7] – Reset Serial Interface

Set this bit to reset serial interface and clear FIFO.

RR [6] – Retry Read

Retry read on failed device ACK.

For alternate 2-wire serial interface, set this bit holds the clock until next access starts.

RD [5] – Read Now

Start read operation.

RB [4] – Read Back and Retry if Failed

If this bit is set, every write from the FIFO will be followed by a read to the same address. If the read data does not match the write data, the write will be retried.

For alternate 2-wire serial interface, this bit is not applicable.

AW [3] – Abort Write on Failed Device ACK

Set this bit to abort the current write on failed device ACK and move to next FIFO entry.

For alternate 2-wire serial interface, this bit is not applicable.

RW [2] – Retry Write on Failed ACK

Set this bit to retry write on failed device ACK.

For alternate 2-wire serial interface, set this bit will retry polling the device when there is no acknowledgement for the sub-address.

AB [1] – Access at Blanking Interval

This bit and AI can both be used to initiate write accesses. If this bit is set, the writes will be performed at the start of the blanking interval. Only one of AB and AI should be set.

For alternate 2-wire serial interface, both AB and AI set will perform write at the start of the blanking interval. If only AI is set, the write will be performed immediately.

AI [0] – Access Immediately

If this bit is set, write accesses will begin immediately.

SBUSW Serial Bus Write

Read/Write **204H**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved (00,0000,0000,0000)														WCNT (01)	

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
WD (0000,0000)								WA (0000,0000)							

RVD [31:18] – Reserved

WCNT [17:16] – Write Count

For each write cycle, these bits indicate the number of bytes which are written in addition to the sub-address. The default is one byte of data follows the sub-address. WCNT can be 0 to 3.

WD [15:8] – Write Data

Contain data that will be written through serial bus interface.

WA [7:0] – Write Address

Contain the device sub-address to be written.

SBUSR Serial Bus Read

Read/Write **208H**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved (0000,0000,0000,0000)															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RD (0000,0000)								RA (0000,0000)							

RVD [31:16] – Reserved

RD [15:8] – Read Data

Contain the data that will be read through serial bus interface.

RA [7:0] – Read Address

Contain the device sub-address to be read.

SCSI Software Control Serial Interface

Read/Write **20CH**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved (0000,0000,0000,0000)															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved (0,0000)					SDA (0)	SCL (0)	SM (0)	Reserved (000,0000)							BT (0)

RVD [31:11] – Reserved

SDA [10] – Software Control SDA

For alternate 2-wire serial interface, when SM is set, I2CDATA will be controlled by this bit.

SCL [9] – Software Control SCL

For alternate 2-wire serial interface, when SM is set, I2CCLK will be controlled by this bit..

SM [8] – Software Mode

For alternate 2-wire serial interface, set this bit to control data and clock signals by driver.

RVD [7:1] – Reserved

BT [0] – Bus Type

Set this bit to use 3-wire serial interface.

GSBWP General Serial Bus Write Port

Read/Write **210H**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RVD (0)	VL (000,0000)							BSEL (0000)				GP (0)	GOC (0)	CH (00)	

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved (00,0000)						BZ (0)	ST (0)	WD (0000,0000)							

RVD [31] - Reserved

VL [30:24] - Valid Length

This is to indicate how many bits in the 3-wire serial interface FIFO are valid for execution.

BSEL [23:20] – Byte Selection

Contain the byte selection among 13 bytes FIFO for each channel.

GP [19] – GPIO Selection

0	Use GPIO [2:0].
1	Use GPIO [5:3].

GOC [18] – GPIO Output Control

0	Disable
1	Enable

CH [17:16] – Channel Selection

Channel selection for channel [3:0].

RVD [15:10] - Reserved

BZ [9] – Busy

Read-only. This bit indicates if programming is still under way since start.

ST [8] – Start Programming

Start to program 3-wire serial interface with the timing information from the 13-byte FIFO.

WD [7:0] – Write Data

Write data to the 13-byte FIFO through this register.

GSBRP General Serial Bus Read Port

Read/Write **214H**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved (0000,0000)								RD (0000,0000)							

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved (0000,0000)								CDIV (0001,0100)							

RVD [31:24] - Reserved

RD [23:16] - Read Data

Read data from the 13-byte FIFO through this register.

RVD [15:8] - Reserved

CDIV [7:0] – Clock divide

The actual clock running is 30MHz/ (CDIV * 8 + 2).

AIC Alternate Serial Interface Control

Read/Write **2FCH**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved (000,0000)							EASI (0)	Reserved (0000,0000)							

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved (0000,0000,0000,0000)															

RVD [31:25] - Reserved

EASI [24] - Enable Alternate 2-wire Serial Interface

Enable alternate 2-wire serial interface.

RVD [23:0] - Reserved

8.5 Timing Generator

With the built-in timing generator logic, various frequencies for the clock can be programmed. When using this internal timing generator, users need to program the following registers.

Clock Out: Register 350H (Index 0x12) – Duty cycle and frequency
Enable TG: Register 300H bit 7
Enable CLK: Register 18 bit 4

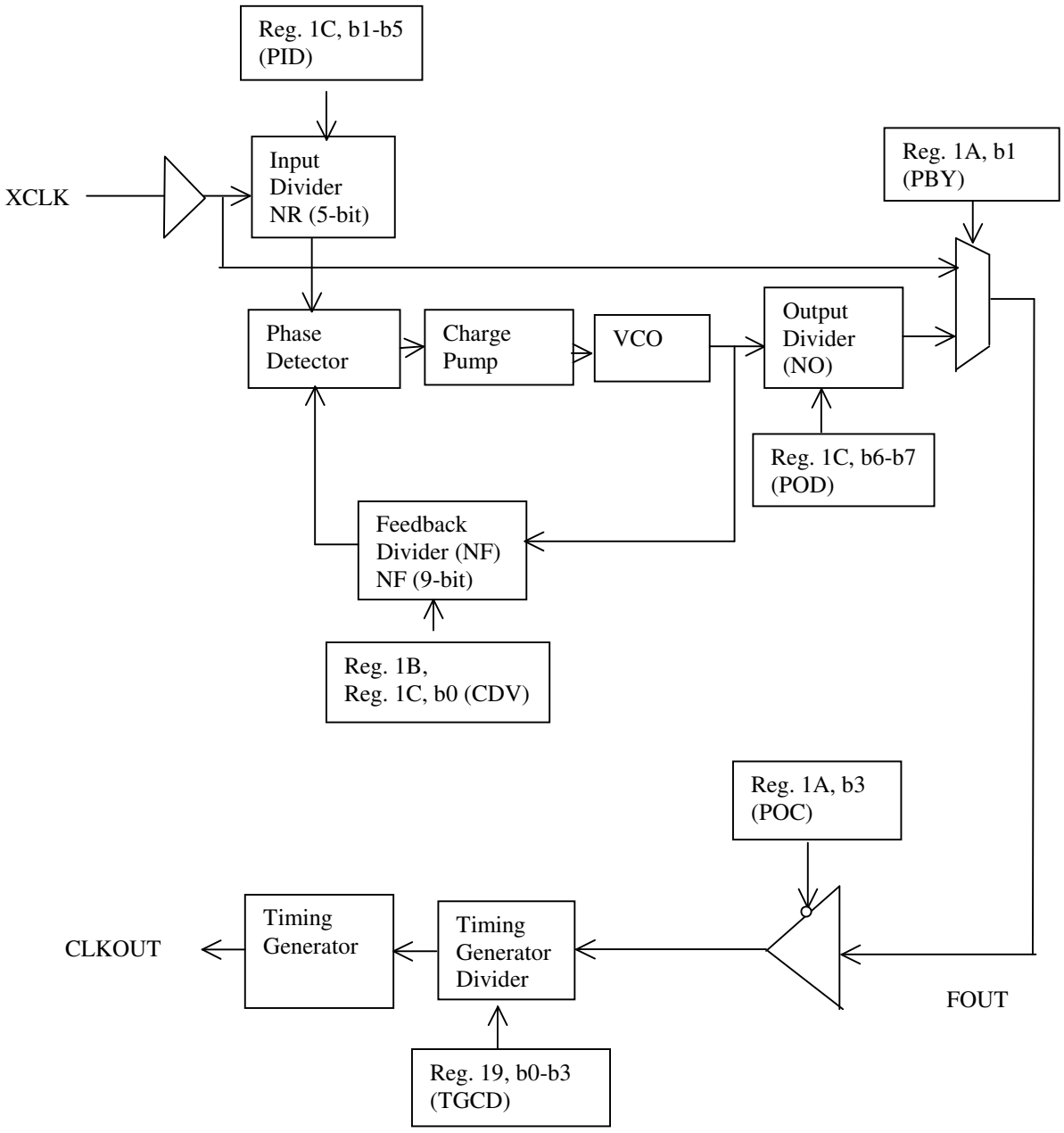
A PLL can be used as the clock source for the video decoder or remote controller. The PLL is feed from the internal transceiver clock. The PLL has bypass and power down modes. PLL output frequency equation is derived as follows:

FOUT = XCLK * (CVD + 2) / ((ID +2) * NO)

NO = 1 when OD [1:0] = 0,
NO = 2 when OD [1:0] = 1,
NO = 3 when OD [1:0] = 2,
NO = 4 when OD [1:0] = 3;

CVD: PLL feedback divider.
PID: PLL input divider.
POD: PLL output divider.
XCLK: Transceiver clock.

8.5.1 PLL Functional Diagram



8.5.2 Registers

PLLSO PLL Select Options

Read/Write **018H**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
CDV (0000,1110)								RVD (000)			RVD (1)	POC (0)	RVD (1)	PBY (0)	PPD (1)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RVD (00)		TGCS (1)	TGCBY (0)	TGCD (0)				Reserved (000)			COC (0)	RVD (0)	RVD (0)	DCI (0)	RVD (0)

CDV [31:24] – PLL Feedback Clock Divider

Contain lower 8 bits of PLL feedback divider.

RVD [23:21] – Reserved

RVD [20] – Reserved

POC [19] – PLL Output Control

0	PLL output is enabled.
1	PLL output is disabled.

RVD [18] – Reserved

PBY [17] – PLL Bypass

0	Clock goes through PLL.
1	Bypasses the PLL.

PPD [16] – PLL Power Down

0	Don't power down PLL.
1	Power down PLL.

RVD [15:14] – Reserved

TGCS [13] –Timing Generator Clock STOP

0	Don't stop TG clock.
1	Stop TG clock.

TGCBY [12] – Timing Generator Clock Source Bypass

0	TG clock source from PLL.
1	N.A. (Stop TG clock.)

TGCD [11:8] – Timing Generator Clock Divider

This field divides the clock input to the timing generator. If zero, the clock will not be divided. For other values, the clock is divided by twice of the value of this register plus one.
For 48 MHz clock input, the following table shows an example of the output clock with different numbers programmed.

TGCD value	TG input clock
0	48 MHz
1	12 MHz
3	6 MHz
7	3 MHz

RVD [7:5] - Reserved

COC [4] – Clock Output Control

0	CLKOUT is disabled.
1	CLKOUT is enabled.

RVD [3] – Reserved

RVD [2] – Reserved

DCI [1] –Clock Invert

0	Clock is not inverted.
1	Clock is inverted.

RVD [0] – Reserved

PLLFD PLL Frequency Divider

Read/Write **01CH**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved (0000,0000,0000,0000)															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved (0000,0000)								POD (01)		PID (0,0011)					CVD (0)

RVD [31:8] – Reserved

POD [7:6] – PLL Output Divider

This field specifies the VCO clock output divider.

PID [5:1] – PLL Input Divider

This field specifies the input clock divider prior to the phase detector.

CVD [0] – PLL Feedback Clock Divider

This is bit 8 of the PLL feedback divider.

Timing Generator

Read/Write at offset **300H**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved (00,0000)						Reserved (00,0000,0000)									

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CEN (0000,0000)								TGC (0)	Reserved (00)		Index (0,0000)				

RVD [31:26] - Reserved

RVD [25:8] – Reserved

TGC [7] – Timing Generation Logic Control

0	Disable
1	Enable

RVD [6:5] - Reserved

IDX [4:0] - Timing Signal Index

This field will index to timing signals. Users must write to this field prior to programming timing generator parameter registers 350-35C.

Value	Description
13-1F	Reserved
12	CLKOUT
11-0	Reserved

Timing Control Parameter 1

Write only at offset **350H**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
PARA1															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PARA1															

PARA1 [31:0] - Timing Generator Control Parameter 1

This register is used to program timing generator signals.

Indexed Signal	Field	Value	Description
CLKOUT	31	0	This bit is valid to set the polarity of pulse that is generated by the positive edge clock. The pulsed signals are the index field signals. Set this bit to zero for non-inverted polarity.
		1	Set this bit to 1 for inverted pulse signal polarity.
	30	0	Pixel signal polarity is non-inverted.
		1	Invert pixel signal polarity.
	29	0	"OR" timing signal operation for indexed signals.
		1	"AND" timing signal operation for indexed signals.
	11:9	0	No delay.
		1	Delay signal for 1 ns.
		2	Delay signal for 2 ns.
		3	Delay signal for 4 ns.
		4	Delay signal for 7 ns.
		5	Delay signal for 10 ns.
		6	Delay signal for 12 ns.
		7	Delay signal for 14 ns.
	8:6	N	Sets up total clock count for each pixel.
	5:3	0	Set negative edge clocked pulse always low
		1	Set negative edge clocked pulse high when pixel counter is "=0" and low otherwise.
		2	Set negative edge clocked pulse high when pixel counter is "=1" and low otherwise.
		3	Set negative edge clocked pulse high when pixel counter is "=2" and low otherwise.
		4	Set negative edge clocked pulse high when pixel counter is "=3" and low otherwise.
		5	Set negative edge clocked pulse high when pixel counter is "=0" or "=1" and low otherwise.
		7	Set negative edge clocked pulse high when pixel counter is "<8" and low otherwise.
	2:0	0	Set positive edge clocked pulse always low
		1	Set positive edge clocked pulse high when pixel counter is "=0" and low otherwise.
		2	Set positive edge clocked pulse high when pixel counter is "=1" and low otherwise.
		3	Set positive edge clocked pulse high when pixel counter is "=2" and low otherwise.
		4	Set positive edge clocked pulse high when pixel counter is "=3" and low otherwise.
		5	Set positive edge clocked pulse high when pixel counter is "=0" or "=1" and low otherwise.
		7	Set positive edge clocked pulse high when pixel counter is "<8" and low otherwise.

8.6 Audio Interface

There are three audio interfaces designed in STK1160.
1. Chip built-in 8-bit ADC
2. AC-Link for AC97 codec
3. I2S interface for I2S audio encoder.

8.6.1 ADC

STK1160 provides an 8-bit analog digital converter for sampling rate 8 KHz. The main operation is to compare the analog input signal with D/A output. If the analog input is greater then D/A output, the A/D conversion process has to continue until the D/A output is slight higher than the analog input signal. Upon completion of the conversion, the ADC stops operation and the correct 8-bit ADC data is generated.

8.6.2 AC97 Interface

STK1160 provides AC-Link to AC97 codec. It supports 16 bits, 48/32 KHz, stereo recording. For 48KHz and 32KHz sample rate selections, please refer to the power-on strapping section for more detail. The Reset signal to the AC97 codec can be controlled via register. After the AC97 codec is reset, the AC97 interface block can be enabled. STK1160 begins generating SYNC signaling to the AC97 codec as soon as it is enabled. There is a 256-byte FIFO to hold data received from the codec.

The control information to and from the AC97 codec is accessed through control registers. To write to the codec registers, the command address and data registers are programmed first and then the CmdWrite bit in the control register is set. To read from the codec registers, the address is loaded first and then the CmdRead bit in the control register is set. When the transfer to the codec is complete, command request bits will be cleared.

8.6.2.1 Registers

Audio Control Register 0

Read/Write at offset **500H**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
CMD (0000,0000,0000,0000)															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
AD (0000,0000)								AC (0)	RVD (00)		RS (1)	HRST (0)	CW (0)	CR (0)	DIR (0)

CMD [31:16] - Command Data

Stores command data to transfer control information to and from the codec.

AD [15:8] - Audio Data

This is snapshot lower byte audio data at any time it is read.

AC [7] – AC97 Interface Control

0	Disable AC97 interface
1	Enable AC97 interface

RVD [6:5] - Reserved

RS [4] - Reset AC97 Interface

0	AC97 operation
1	Reset AC97 Interface

HRST [3] – Hardware Reset AC97 Codec

0	Hardware Reset AC97 Codec
1	AC97 operation

CW [2] - Command Write

0	Data phase
1	Control write phase

CR [1] - Command Read

0	Data phase
1	Control read phase

DIR [0] - Direction

0	Out – Data out
1	In - Data In

Audio Control Register 1

Read/Write at offset **504H**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved (00,0000,0000,0000)														CHSEL (0)	D16 (0)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FIFO (0000,0000)								RVD (0)	CMA (000,0000)						

RVD [31:18] - Reserved

CHSEL [17] - Input Channel Selection

0	L & R channel
1	Microphone channel

D16 [16] - Data16

0	8-bit data
1	16-bit audio data

FIFO [15:8] - FIFO available

These read only bits indicate current FIFO length available in byte.

RVD [7] - Reserved

CMA [6:0] - Command address

The command address is to transfer control information to and from the codec.

8.6.3 I2S Interface

STK1160 provides I2S interface to I2S encoder. It supports 16 bits, 48/32 KHz, stereo recording. For 48KHz and 32KHz sample rate selections, please refer to the power-on strapping section for more detail. The I2S bus master device sends the clock, data, and the word select signals, and STK1160 receives these signals.

8.6.3.1 Registers

I2S Control

Read/Write at offset **50CH**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved (0000,0000,0000,0000)															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved (00000000,00000)													RVD (0)	IM (0)	IE (0)

RVD [31:16] – Reserved

RVD [15:3] - Reserved

RVD [2] – Reserved

IM [1] – I2S Mode or Left Adjust Mode

Set this bit to operate I2S interface in left adjust mode.

IE [0] – I2S Enable

Set this bit to enable I2S interface.

8.7 External EEPROM Interface

STK1160 provides an optional 3-wire EEPROM interface that allows the vendor ID, product ID and string descriptors to be customized. The external EEPROM interface uses pins GPIO [0] - GPIO [2], so if a 93C46 EEPROM is present, these pins are not available for other uses. STK1160 also supports 2-wire interface serial EEPROM. "Word" Addresses for data in these EEPROM are as follows:

Address	Value
0x0	Vendor ID
0x1	Product ID
0x2	String Index 1 (Manufacturer)
0xd	String Index 2 (Product)
0x26	String Index b (Audio interface)

Descriptors in the EEPROM can be set using the USB standard SetDescriptor control transfer. To set the vendor and product IDs, use SetDescriptor for index 16 with length 4. When setting the IDs, do not precede the ID values with descriptor type or index information.

8.7.1.1 Registers

EEPROM Size

Read/Write at offset **5F0H**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved (0000,0000,0000,0000)															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved (0000,0000,0000)												ADW (0)	ROMSIZE (000)		

RVD[31:4] - Reserved

ADW [3] – Always in Double Word

Set this bit to ensure STK1160 always sends even number of 16 bit data in a frame.

ROMSIZE [2:0] – EEPROM Size

Bits 2:0	EEPROM Size (for 3-wire serial interface)
000	1K bits – 64X16
Others	Reserved

8.8 USB Interface

8.8.1 Register Accessing

All blocks within STK1160 are connected by an 8-bit register bus. Register bus reads and writes are initiated by the USB with the vendor-specific Register Read and Register Write control transfers. The bRequest value for Register Read is 0 and bRequest for Register Write is 1. For both, the high byte of the wIndex contains the functional block to be accessed and the low byte contains the 8-bit address within the block. For a read,

wLength should be set to one and the requested data will be returned in the control transfer data phase. For a write, wLength should be set to zero and the low byte of wValue should be set to the value to be written. Block addresses are given in the following table:

Block Select	STK1160 Registers	STK1160 Functional Block
0	0xxH	GPIO
1	1xxH	Video decoder interface
2	2xxH	Serial bus interface
3	3xxH	Timing generator
5	5xxH	Audio interface

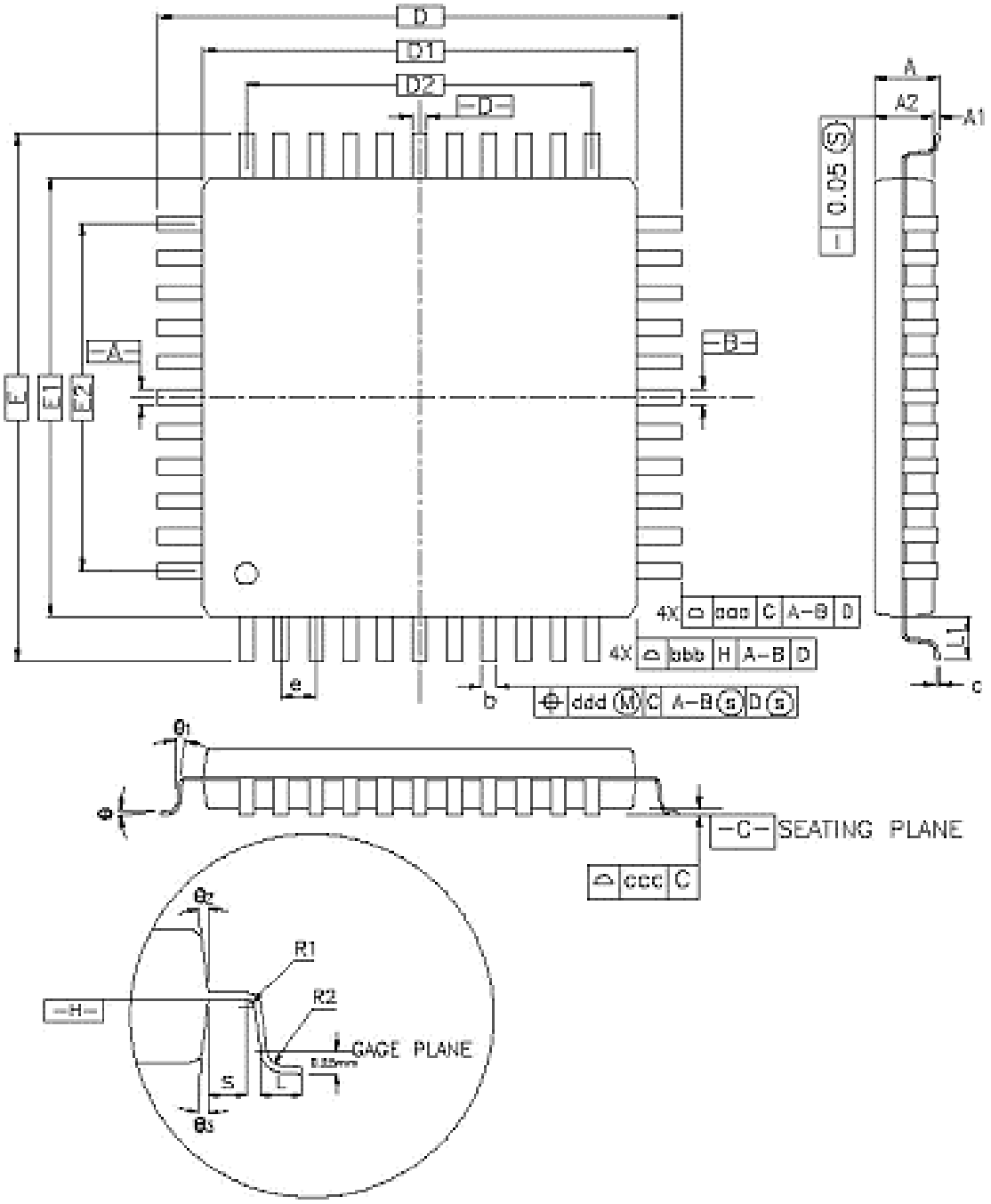
STK1160 supports two USB vendor specific requests, Register Read and Register Write. Register Read and Register Write utilize control endpoint 0, one byte per request, to access registers. Since the register size is 4 bytes, to access bits 31 to 24, add 3 to the register number to get final address. Add 2 to access bits 16 to 23, and add 1 to access bits 15 to 8. For example, to access register 0x300, bits 16 to 23, you have to access register 0x302.

Vendor request	bmRequest type	bRequest	wValue	wIndex	wLength	Data returned in data phase
Register Read	0xC0	0x00	0x00	Address	0x0001	Register value
Register Write	0x40	0x01	Register value in low byte	Address	0x0000	None

8.9 Power management

When STK1160 enters USB suspend state, the oscillator and PLL are automatically powered down to reduce suspend mode current. Before entering suspend, software should set the audio and video streaming interfaces to alternate setting 0, which will power down the ADC and video data FIFO SRAM respectively.

9 Package Drawing



80 LQPF Package

Symbol	Millimeter			Inch		
	Minimum	Normal	Maximum	Minimum	Normal	Maximum
A			1.60			0.063
A1	0.05		0.15	0.002		0.006
A2	1.35	1.40	1.45	0.053	0.055	0.057
D	12.00 BSC			0.472 BSC		
D1	10.00 BSC			0.393 BSC		
E	12.00 BSC			0.472 BSC		
E1	10.00 BSC			0.393 BSC		
R2	0.08		0.20	0.003		0.008
R1	0.08			0.003		
θ	0°	3.5°	7°	0°	3.5°	7°
θ_1	0°			0°		
θ_2	11°	12°	13°	11°	12°	13°
θ_3	11°	12°	13°	11°	12°	13°
c	0.09		0.20	0.004		0.008
L	0.45	0.60	0.75	0.018	0.024	0.030
L1	1.00 REF			0.039 REF		
S	0.20			0.008		
b	0.13	0.16	0.23	0.005	0.006	0.009
e	0.40 BSC			0.016 BSC		
D2	7.60			0.299		
E2	7.60			0.299		
Tolerances of form and position						
aaa	0.20			0.008		
bbb	0.20			0.008		
ccc	0.08			0.003		
ddd	0.07			0.003		

Note:
1. Dimension D1 and E1 do not include mold protrusion. Allowable protrusion is 0.25mm per side. D1 and E1 are maximum plastic body size dimensions including mold mismatch.
2. Dimension b does not include dambar protrusion. Allowable dambar protrusion shall not cause the lead width to exceed the maximum b dimension by more than 0.08mm.
Dambar cannot be located on the lower radius or the foot. Minimum space between protrusion and an adjacent lead is 0.07mm for 0.4mm and 0.5mm pitch packages.

Revision History

Revision	Date	Description
1.0	February 21, 2006	Initial release
1.1	February 22, 2006	Revision of the internal specification 0.92 version.
1.2	February 24, 2006	Revision of the internal specification 0.95 version.