STK1743

nvTime™
8K x 8 *AutoStore*™ nvSRAM with Real-Time Clock

ADVANCE

FEATURES

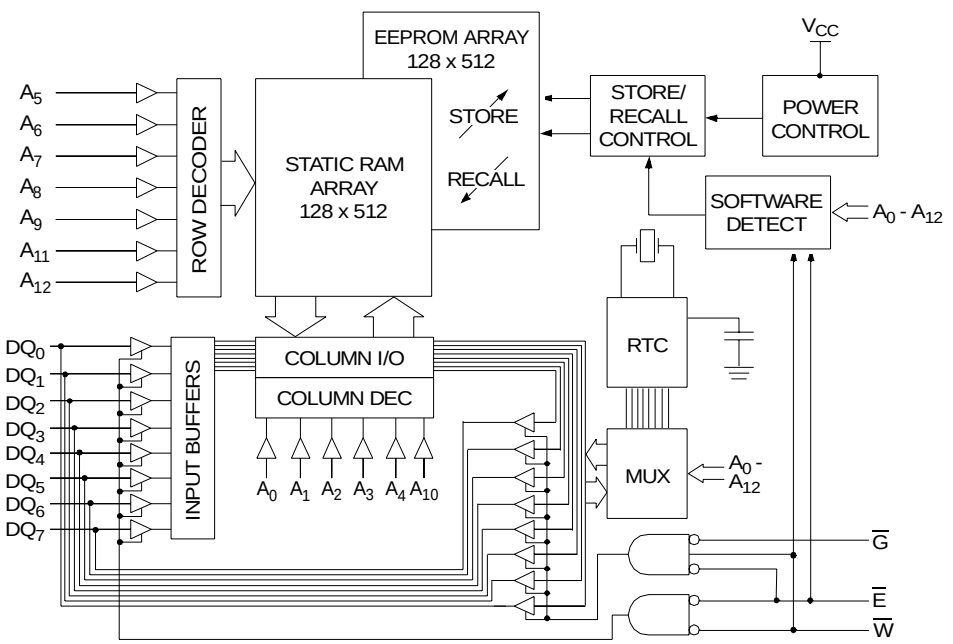
- **Data Integrity of Simtek nvSRAM Combined with Full-Featured Real-Time Clock**
- **Stand-Alone Nonvolatile Memory and Time-Keeping Solution—No Other Parts Required**
- **No Batteries to Fail**
- **Fast 25ns, 35ns and 45ns Access Times**
- **Software- and *AutoStore*™-Controlled Nonvolatile Cycles**
- **Year 2000 Compliant with Leap Year Compensation**
- **24-Hour BCD Format**
- **100-Year Data Retention over Full Industrial Temperature Range**
- **Full 30-Day RTC Operation on Each Power Loss**
- **Single 5V ± 10% Power Supply**

DESCRIPTION

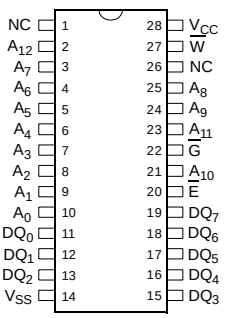
The Simtek STK1743 DIP module houses 64Kb of nonvolatile static RAM, a real-time clock (RTC) with crystal and a high-value capacitor to support systems that require high reliability and ease of manufacturing. READ and WRITE access to all RTC functions and the memory is the same as a conventional x 8 SRAM. The highest eight addresses of the RAM support clock registers for centuries, years, months, dates, days, hours, minutes and seconds.

Independent data resides in the integral EEPROM at all times. Automatic *RECALL* on power up transfers the EEPROM data to the SRAM, while an automatic *STORE* on power down transfers SRAM data to the EEPROM. A software *RECALL* and *STORE* are also possible on user command. *nvTime*™ allows unlimited accesses to SRAM, unlimited *RECALL*s and 10^6 *STORE*s.

BLOCK DIAGRAM



PIN CONFIGURATIONS



600 mil
Dual
In-Line
Module

PIN NAMES

A_0 - A_{12}	Address Inputs
$\overline{W}$	Write Enable
DQ_0 - DQ_7	Data In/Out
$\overline{E}$	Chip Enable
$\overline{G}$	Output Enable
V_{CC}	Power (+ 5V)
V_{SS}	Ground

ABSOLUTE MAXIMUM RATINGS[a]

Voltage on Input Relative to V_{SS} . . . . . –0.6V to (V_{CC} + 0.5V)
Voltage on DQ_{0-7} . . . . . –0.5V to (V_{CC} + 0.5V)
Temperature under Bias . . . . . –55°C to 125°C
Storage Temperature . . . . . –65°C to 150°C
Power Dissipation 1W
DC Output Current (1 output at a time, 1s duration) 15mA

Note a: Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This a stress rating only, and functional operation of the device at conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC CHARACTERISTICS

(V_{CC} = 5.0V ± 10%)

SYMBOL	PARAMETER	COMMERCIAL		INDUSTRIAL		UNITS	NOTES
		MIN	MAX	MIN	MAX		
I_{CC_1}[b]	Average V_{CC} Current		85 80 75		95 85 80	mA mA mA	t_{AVAV} = 25ns t_{AVAV} = 35ns t_{AVAV} = 45ns
I_{CC_2}[c]	Average V_{CC} Current during *STORE*		6		7	mA	All Inputs Don't Care, V_{CC} = max
I_{CC_3}[b]	Average V_{CC} Current at t_{AVAV} = 200ns		15		15	mA	$\overline{W} \geq (V_{CC} - 0.2V)$ All Others Cycling, CMOS Levels
I_{CC_4}[c]	Average V_{CC} Current during *AutoStore*™ Cycle		4		4	mA	All Inputs Don't Care
I_{SB_1}[d]	Average V_{CC} Current (Standby, Cycling TTL Input Levels)		30 26 23		31 27 24	mA mA mA	t_{AVAV} = 25ns, $\overline{E} \geq V_{IH}$ t_{AVAV} = 35ns, $\overline{E} \geq V_{IH}$ t_{AVAV} = 45ns, $\overline{E} \geq V_{IH}$
I_{SB_2}[d]	V_{CC} Standby Current (Standby, Stable CMOS Input Levels)		3		3	mA	$\overline{E} \geq (V_{CC} - 0.2V)$ All Others $V_{IN} \leq 0.2V$ or $\geq (V_{CC} - 0.2V)$
I_{ILK}	Input Leakage Current		±1		±1	µA	V_{CC} = max $V_{IN} = V_{SS}$ to V_{CC}
I_{OLK}	Off-State Output Leakage Current		±5		±5	µA	V_{CC} = max $V_{IN} = V_{SS}$ to V_{CC}, $\overline{E}$ or $\overline{G} \geq V_{IH}$
V_{IH}	Input Logic "1" Voltage	2.2	V_{CC} + .5	2.2	V_{CC} + .5	V	All Inputs
V_{IL}	Input Logic "0" Voltage	V_{SS} – .5	0.8	V_{SS} – .5	0.8	V	All Inputs
V_{OH}	Output Logic "1" Voltage	2.4		2.4		V	I_{OUT} = –4mA
V_{OL}	Output Logic "0" Voltage		0.4		0.4	V	I_{OUT} = 8mA
T_A	Operating Temperature	0	70	–40	85	°C	

Note b: I_{CC_1} and I_{CC_3} are dependent on output loading and cycle rate. The specified values are obtained at minimum cycle with outputs unloaded.
Note c: I_{CC_2} and I_{CC_4} are the average currents required for the duration of the respective *STORE* cycles (t_{STORE}).
Note d: $\overline{E} \geq V_{IH}$ will not produce standby current levels until any nonvolatile cycle in progress has timed out.

AC TEST CONDITIONS

Input Pulse Levels . . . . . 0V to 3V
Input Rise and Fall Times . . . . . ≤ 5ns
Input and Output Timing Reference Levels 1.5V
Output Load . . . . . See Figure 1

CAPACITANCE[e] (T_A = 25°C, f = 1.0MHz)

SYMBOL	PARAMETER	MAX	UNITS	CONDITIONS
C_{IN}	Input Capacitance	10	pF	ΔV = 0 to 3V
C_{OUT}	Output Capacitance	12	pF	ΔV = 0 to 3V

Note e: These parameters are guaranteed but not tested.

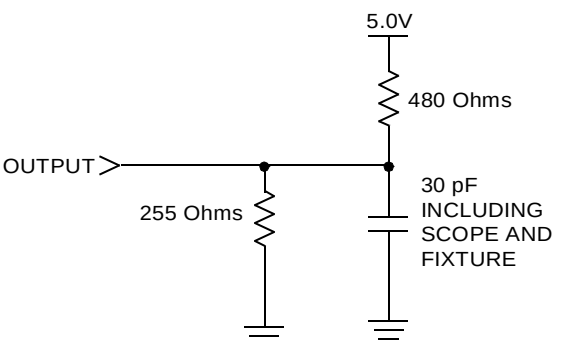


Figure 1: AC Output Loading

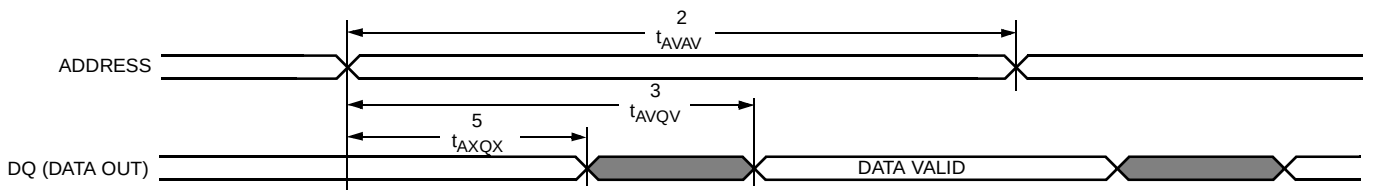
READ CYCLES #1 & #2

(V_{CC} = 5.0V ± 10%)

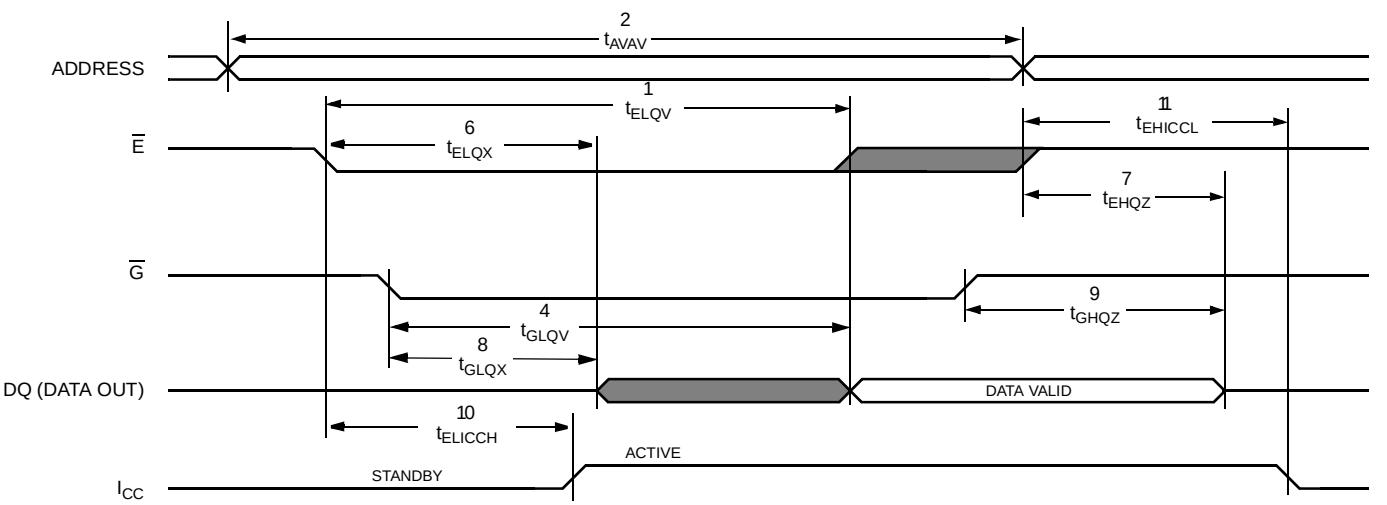
NO.	SYMBOLS		PARAMETER	STK1743-25		STK1743-35		STK1743-45		UNITS
	#1, #2	Alt.		MIN	MAX	MIN	MAX	MIN	MAX	
1	t_{ELQV}	t_{ACS}	Chip Enable Access Time		25		35		45	ns
2	t_{AVAV}[f]	t_{RC}	Read Cycle Time	25		35		45		ns
3	t_{AVQV}[g]	t_{AA}	Address Access Time		25		35		45	ns
4	t_{GLQV}	t_{OE}	Output Enable to Data Valid		10		15		20	ns
5	t_{AXQX}[g]	t_{OH}	Output Hold after Address Change	5		5		5		ns
6	t_{ELQX}	t_{LZ}	Chip Enable to Output Active	5		5		5		ns
7	t_{EHQZ}[h]	t_{HZ}	Chip Disable to Output Inactive		10		13		15	ns
8	t_{GLQX}	t_{OLZ}	Output Enable to Output Active	0		0		0		ns
9	t_{GHQZ}[h]	t_{OHZ}	Output Disable to Output Inactive		10		13		15	ns
10	t_{ELICCH}[e]	t_{PA}	Chip Enable to Power Active	0		0		0		ns
11	t_{EHICCL}[d, e]	t_{PS}	Chip Disable to Power Standby		25		35		45	ns

Note f: $\overline{W}$ must be high during SRAM READ cycles and low during SRAM WRITE cycles.
Note g: I/O state assumes $\overline{E}$, $\overline{G} \leq V_{IL}$ and $\overline{W} \geq V_{IH}$; device is continuously selected.
Note h: Measured ± 200mV from steady state output voltage.

READ CYCLE #1: Address Controlled[f, g]



READ CYCLE #2: $\overline{E}$ Controlled[f]



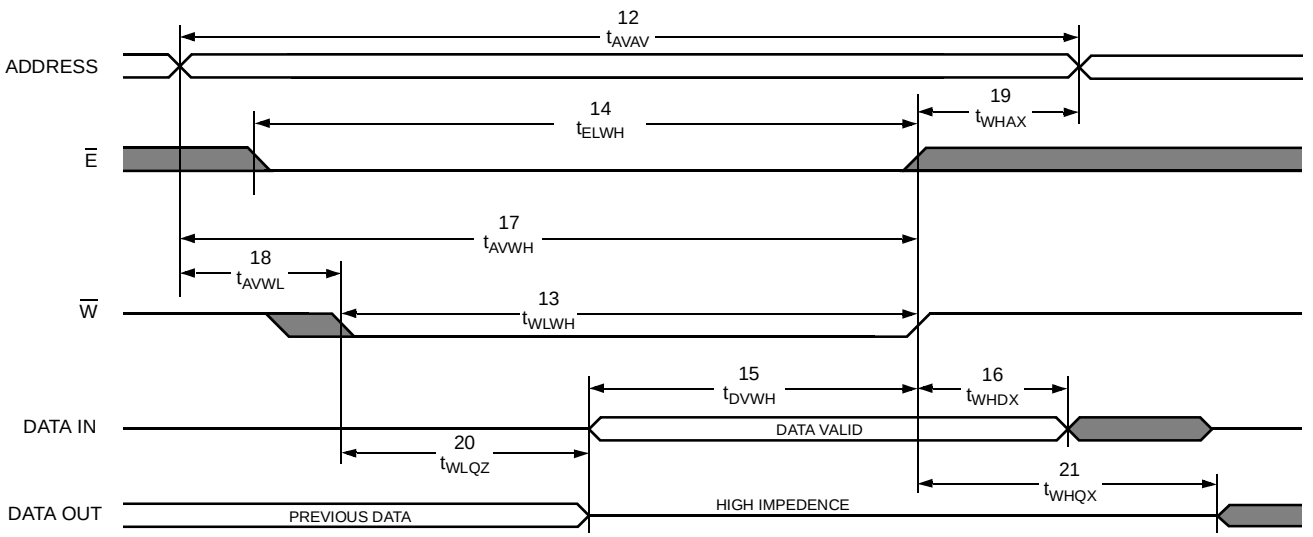
WRITE CYCLES #1 & #2

(V_{CC} = 5.0V ± 10%)

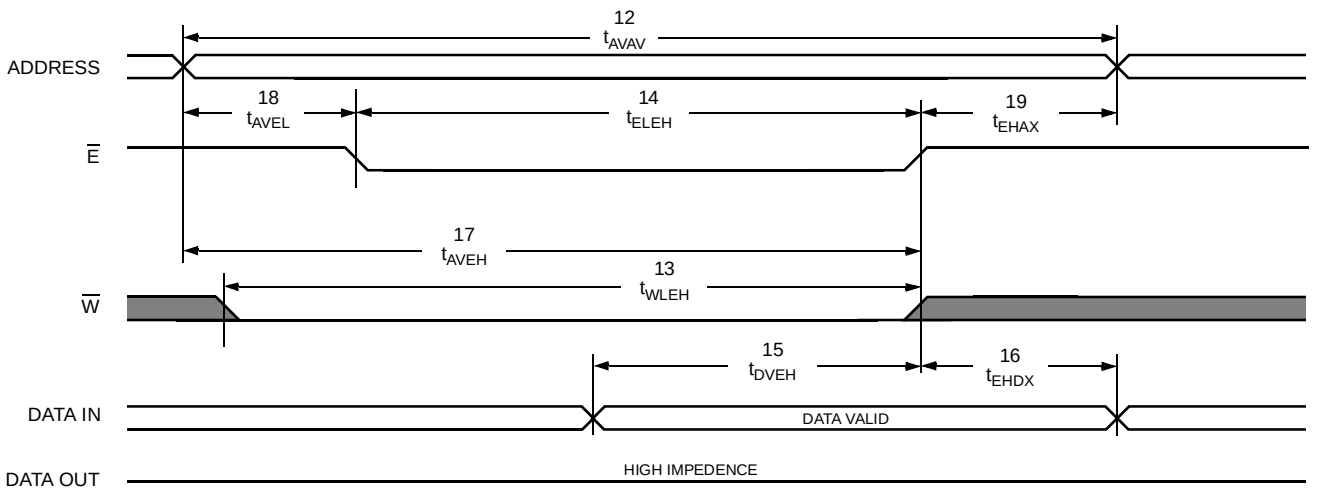
NO.	SYMBOLS			PARAMETER	STK1743-25		STK1743-35		STK1743-45		UNITS
	#1	#2	Alt.		MIN	MAX	MIN	MAX	MIN	MAX	
12	t_{AVAV}	t_{AVAV}	t_{WC}	Write Cycle Time	25		35		45		ns
13	t_{WLWH}	t_{WLEH}	t_{WP}	Write Pulse Width	20		25		30		ns
14	t_{ELWH}	t_{ELEH}	t_{CW}	Chip Enable to End of Write	20		25		30		ns
15	t_{DVWH}	t_{DVEH}	t_{DW}	Data Set-up to End of Write	10		12		15		ns
16	t_{WHDX}	t_{EHDX}	t_{DH}	Data Hold after End of Write	0		0		0		ns
17	t_{AVWH}	t_{AVEH}	t_{AW}	Address Set-up to End of Write	20		25		30		ns
18	t_{AVWL}	t_{AVEL}	t_{AS}	Address Set-up to Start of Write	0		0		0		ns
19	t_{WHAX}	t_{EHAX}	t_{WR}	Address Hold after End of Write	0		0		0		ns
20	t_{WLQZ}[h, i]		t_{WZ}	Write Enable to Output Disable		10		13		15	ns
21	t_{WHQX}		t_{OW}	Output Active after End of Write	5		5		5		ns

Note i: If $\overline{W}$ is low when $\overline{E}$ goes low, the outputs remain in the high-impedance state.
Note j: $\overline{E}$ or $\overline{W}$ must be ≥ V_{IH} during address transitions.

WRITE CYCLE #1: $\overline{W}$ Controlled[j]



WRITE CYCLE #2: $\overline{E}$ Controlled[j]



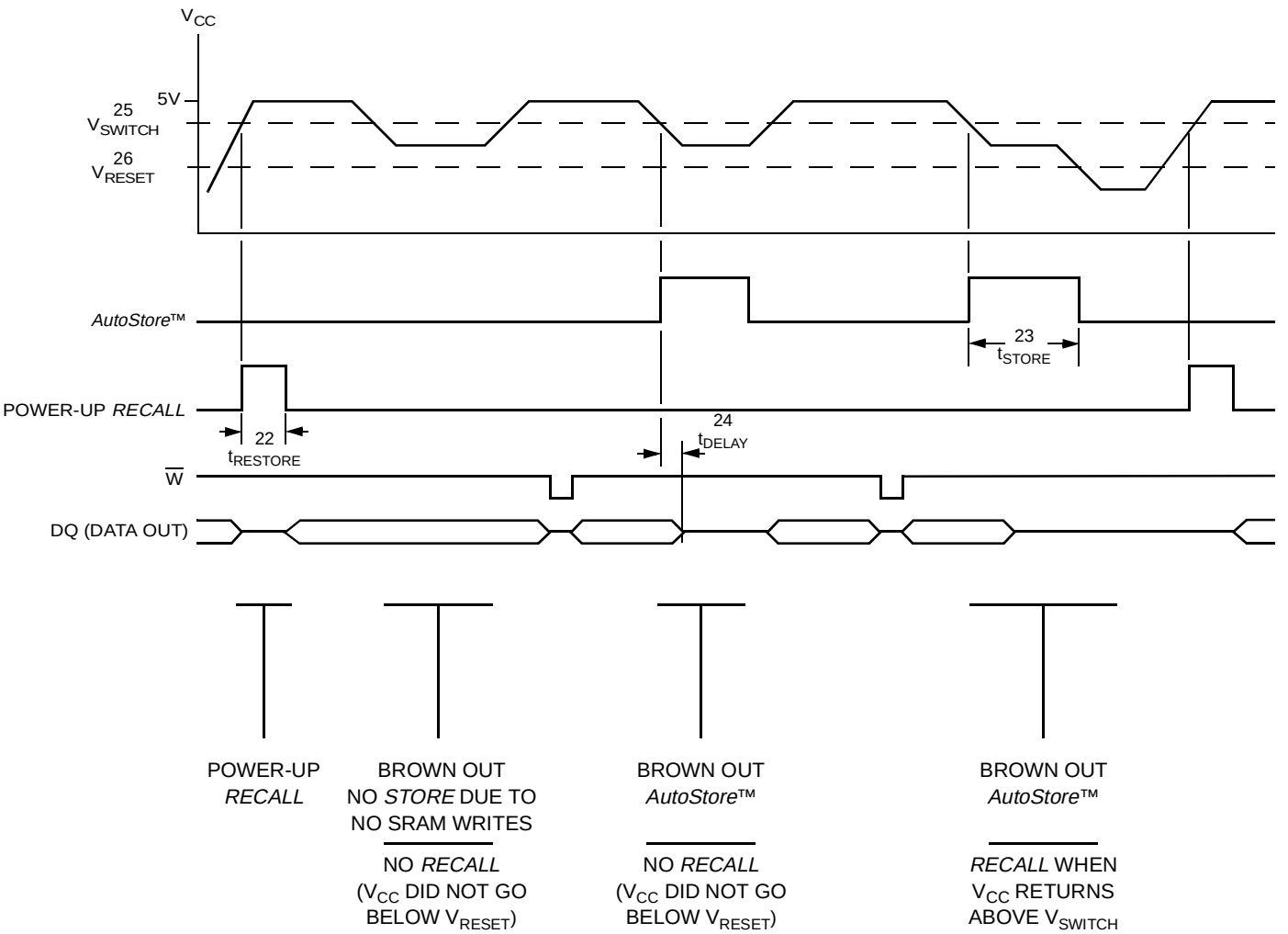
AutoStore™ / POWER-UP *RECALL*

(V_{CC} = 5.0V ± 10%)

NO.	SYMBOLS	PARAMETER	STK1743		UNITS	NOTES
	Standard		MIN	MAX		
22	$t_{RESTORE}$	Power-Up *RECALL* Duration		550	µs	k
23	t_{STORE}	*STORE* Cycle Duration		10	ms	g
24	t_{DELAY}	Time Allowed to Complete SRAM Cycle	1		µs	g
25	V_{SWITCH}	Low Voltage Trigger Level	4.0	4.5	V	
26	V_{RESET}	Low Voltage Reset Level		3.9	V	

Note k: $t_{RESTORE}$ starts from the time V_{CC} rises above V_{SWITCH}.

AutoStore™ / POWER-UP *RECALL*



SOFTWARE MODE SELECTION

$\overline{E}$	$\overline{W}$	A_{12} - A_0 (hex)	MODE	I/O	NOTES
L	H	0000	Read SRAM	Output Data	l
		1555	Read SRAM	Output Data	
		0AAA	Read SRAM	Output Data	
		1FFF	Read SRAM	Output Data	
		10F0	Read SRAM	Output Data	
		0F0F	Nonvolatile *STORE*	Output High Z	
L	H	0000	Read SRAM	Output Data	l
		1555	Read SRAM	Output Data	
		0AAA	Read SRAM	Output Data	
		1FFF	Read SRAM	Output Data	
		10F0	Read SRAM	Output Data	
		0F0E	Nonvolatile *RECALL*	Output High Z	

Note l: The six consecutive addresses must be in the order listed. $\overline{W}$ must be high during all six consecutive cycles to enable a nonvolatile cycle.

SOFTWARE CYCLES #1 & #2[m, n]

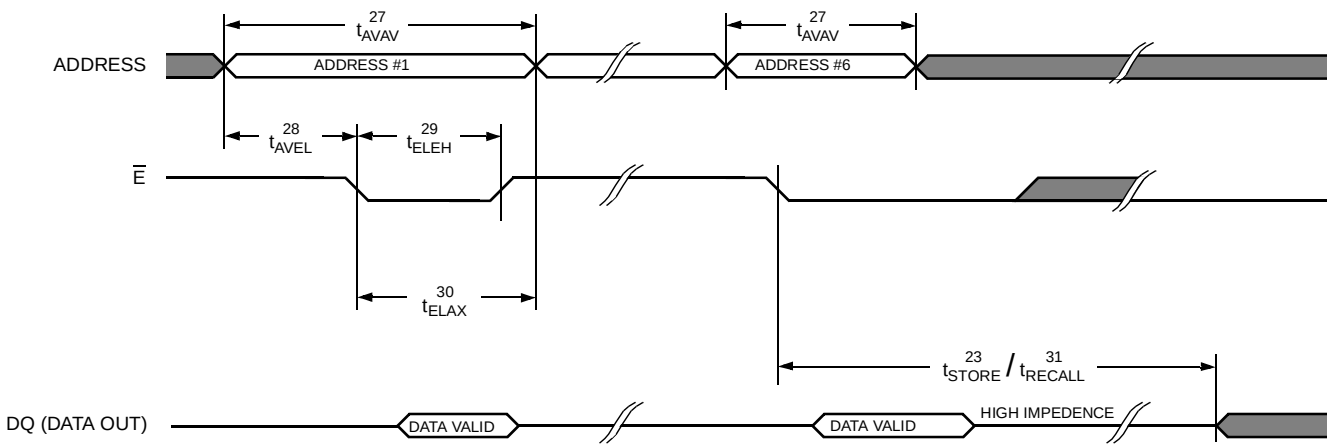
(V_{CC} = 5.0V ± 10%)

NO.	SYMBOLS	PARAMETER	STK1743-25		STK1743-35		STK1743-45		UNITS
	#1		MIN	MAX	MIN	MAX	MIN	MAX	
27	t_{AVAV}	*STORE*/*RECALL* Initiation Cycle Time	25		35		45		ns
28	t_{AVEL}[m]	Address Set-up Time	0		0		0		ns
29	t_{ELEH}[m]	Clock Pulse Width	20		25		30		ns
30	t_{ELAX}[g, m]	Address Hold Time	20		20		20		ns
31	t_{RECALL}	*RECALL* Duration		20		20		20	µs

Note m: The software sequence is clocked with $\overline{E}$ controlled reads.

Note n: The six consecutive addresses must be in the order listed in the Software Mode Selection Table: (0000, 1555, 0AAA, 1FFF, 10F0, 0F0F) for a *STORE* cycle or (0000, 1555, 0AAA, 1FFF, 10F0, 0F0E) for a *RECALL* cycle. $\overline{W}$ must be high during all six consecutive cycles.

SOFTWARE CYCLE: $\overline{E}$ Controlled



DEVICE OPERATION

The STK1743 is an 8K x 8 nonvolatile static RAM with a full-function real-time clock (RTC). The data integrity is secured in EEPROM, not subject to battery or capacitor discharge. The real-time clock registers reside in the eight uppermost RAM locations, and contain century, year, month, date, day, hour, minute and second data in 24-hour BCD format. Corrections for the day of the month and leap years are made automatically. This nonvolatile time-keeping RAM is functionally similar to any JEDEC standard 8K x 8 SRAM.

The RTC registers are double-buffered to avoid access of incorrect data that could otherwise occur during clock update cycles. The double-buffered system prevents time loss by maintaining internal clock operation while time register data is accessed. The STK1743 contains integral power-fail circuitry that deselects the device when V_{CC} drops below V_{SWITCH}.

The STK1743 is a pin-compatible replacement for the ST Microelectronics M48T08 and the Dallas Semiconductor DS1743, but without the limitations of an embedded lithium battery. The Simtek device uses a double-layer high-value capacitor to maintain RTC operation on power down for at least 30 days. The part can be soldered directly onto printed circuit boards and handled without concern for damaging or discharging internal batteries. Unlike some other RTCs, the STK1743 is Year 2000-compliant.

NOISE CONSIDERATIONS

Note that the STK1743 is a high-speed memory and so must have a high-frequency bypass capacitor of approximately 0.1µF connected between V_{CC} and V_{SS}, using leads and traces that are as short as possible. As with all high-speed CMOS ICs, normal careful routing of power, ground and signals will help prevent noise problems.

SRAM AND RTC READ

The STK1743 performs a READ cycle whenever $\overline{E}$ and $\overline{G}$ are low and $\overline{W}$ is high. The address specified on pins A_{0-12} determines which of the 8,192 data bytes will be accessed. When the READ is initiated by an address transition, the outputs will be valid after a delay of t_{AVQV} (READ cycle #1). If the READ is initiated by $\overline{E}$ or $\overline{G}$, the outputs will be valid at t_{ELQV} or at t_{GLQV}, whichever is later (READ cycle #2). The data outputs will repeatedly respond to address changes within the t_{AVQV} access time without the need for transitions on any control input pins, and will remain valid until another address change or until $\overline{E}$ or $\overline{G}$ is brought high or $\overline{W}$ is brought low.

Note that the eight most significant bytes of the address space are reserved for accessing the RTC registers, as shown in the Register Map below.

While the double-buffered RTC register structure reduces the chance of reading incorrect data from the clock, the user should halt internal updates to the

RTC REGISTER MAP

ADDRESS (HEXADECIMAL)	BCD DATA								FUNCTION/RANGE
	D7	D6	D5	D4	D3	D2	D1	D0	
1FF8	W	R	10 Centuries		Centuries				Centuries: 00-39, Control
1FF9	X	10 Seconds			Seconds				Seconds: 00 - 59
1FFA	X	10 Minutes			Minutes				Minutes: 00 - 59
1FFB	X	X	10 Hours		Hours				Hours: 00 - 23
1FFC	1	FT	X	X	X	Days			Days: 01 - 07
1FFD	X	X	10 Dates		Dates				Dates: 01 - 31
1FFE	X	X	X	10 Mos.	Months				Months: 01 - 12
1FFF	10 Years				Years				Years: 00 - 99

Key: R = Read Bit
W = Write Bit
1 = Battery Flag High (no battery to fail)
FT = Frequency Test Bit
X = Don't Care

STK1743 clock registers before reading clock data to prevent reading of data in transition. Stopping the internal register updates does not affect clock accuracy.

The updating process is stopped by writing a "1" to the read bit (the seventh most significant bit in the control register), and will not restart until a "0" is written to the read bit. The RTC registers can then be read while the internal clock continues to run.

Within one second after a "0" is written to the read bit, all STK1743 registers are simultaneously updated.

SRAM WRITE AND SETTING THE CLOCK

A WRITE cycle is performed whenever $\overline{E}$ and $\overline{W}$ are low. The address inputs must be stable prior to entering the WRITE cycle and must remain stable until either $\overline{E}$ or $\overline{W}$ goes high at the end of the cycle. The data on the common I/O pins DQ_{0-7} will be written into the memory if it is valid t_{DVWH} before the end of a $\overline{W}$ controlled WRITE or t_{DVEH} before the end of an $\overline{E}$ controlled WRITE.

It is recommended that $\overline{G}$ be kept high during the entire WRITE cycle to avoid data bus contention on the common I/O lines. If $\overline{G}$ is left low, internal circuitry will turn off the output buffers t_{WLQZ} after $\overline{W}$ goes low.

Setting the write bit (the eighth most significant bit of the control register) to a "1" halts updates to the STK1743 registers. The correct day, date and time can then be written into the registers in 24-hour BCD format. Resetting the write bit to "0" transfers those values to the actual clock counters, after which the clock resumes normal operation.

CLOCK ACCURACY

The STK1743 is guaranteed to be accurate to within ± 1 minute per month at 25°C. The part requires no additional calibration, and temperature variations will have a negligible effect in most applications.

DATA RETENTION MODE

During normal operation ($V_{CC} \geq 4.5V$), the STK1743 can be accessed with standard SRAM READ and WRITE cycles. However, when V_{CC} falls below the power-fail voltage, V_{SWITCH} (the voltage at which write protection occurs), access to the internal clock register and the SRAM is blocked. At this voltage, SRAM data is automatically stored to the integral EEPROM, and power for the clock oscillator switches from the V_{CC} pin to the internal capacitor. The capacitor maintains clock activity and data until V_{CC} returns to its nominal level.

SOFTWARE NONVOLATILE *STORE*

The STK1743 software *STORE* cycle is initiated by executing sequential READ cycles from six specific address locations. During the *STORE* cycle an erase of the previous nonvolatile data is first performed, followed by a program of the nonvolatile elements. The program operation copies the SRAM data into nonvolatile memory. Once a *STORE* cycle is initiated, further input and output are disabled until the cycle is completed.

Because a sequence of READs from specific addresses is used for *STORE* initiation, it is important that no other READ or WRITE accesses intervene in the sequence or the sequence will be aborted and no *STORE* or *RECALL* will take place.

To initiate the software *STORE* cycle, the following READ sequence must be performed:

1.	Read address	0000 (hex)	Valid READ
2.	Read address	1555 (hex)	Valid READ
3.	Read address	0AAA (hex)	Valid READ
4.	Read address	1FFF (hex)	Valid READ
5.	Read address	10F0 (hex)	Valid READ
6.	Read address	0F0F (hex)	Initiate *STORE* cycle

The software sequence must be clocked with $\overline{E}$ controlled READs.

Once the sixth address in the sequence has been entered, the *STORE* cycle will commence and the memory accesses will be disabled. It is important that READ cycles and not WRITE cycles be used in the sequence, although it is not necessary that $\overline{G}$ be low for the sequence to be valid. After the t_{STORE} cycle time has been fulfilled, the SRAM will again be activated for READ and WRITE operation.

SOFTWARE NONVOLATILE *RECALL*

A software *RECALL* cycle is initiated with a sequence of READ operations in a manner similar to the software *STORE* initiation. To initiate the *RECALL* cycle, the following sequence of READ operations must be performed:

1.	Read address	0000 (hex)	Valid READ
2.	Read address	1555 (hex)	Valid READ
3.	Read address	0AAA (hex)	Valid READ
4.	Read address	1FFF (hex)	Valid READ
5.	Read address	10F0 (hex)	Valid READ
6.	Read address	0F0E (hex)	Initiate *RECALL* cycle

Internally, *RECALL* is a two-step procedure. First, the SRAM data is cleared, and second, the nonvolatile information is transferred into the SRAM cells. After the t_{RECALL} cycle time the SRAM will once again be ready for READ and WRITE operations. The *RECALL* operation in no way alters the data in the EEPROM cells. The nonvolatile data can be recalled an unlimited number of times. Note that the RTC registers are not affected by nonvolatile operations.

AutoStore™ OPERATION

The STK1743 uses capacitance built into the module to perform an automatic *STORE* on power down.

In order to prevent unnecessary *STORE* operations, automatic *STORE*s will be ignored unless at least one WRITE operation has taken place since the most recent *STORE* or *RECALL* cycle. Software-initiated *STORE* cycles are performed regardless of whether a WRITE operation has taken place.

POWER-UP *RECALL*

During power up, or after any low-power condition (V_{CC} < V_{RESET}), an internal recall request will be latched. When V_{CC} once again exceeds V_{SWITCH}, a *RECALL* cycle will automatically be initiated and will take $t_{RESTORE}$ to complete.

HARDWARE PROTECT

The STK1743 offers hardware protection against inadvertent *STORE* and SRAM WRITE operation during low-voltage conditions. When V_{CC} < V_{SWITCH}, all software *STORE* operations and SRAM writes are inhibited.

LOW AVERAGE ACTIVE POWER

The STK1743 draws significantly less current when it is cycled at times longer than 50ns. Figure 2 shows the relationship between I_{CC} and READ cycle time. Worst-case current consumption is shown for both CMOS and TTL input levels (commercial temperature range, V_{CC} = 5.5V, 100% duty cycle on chip enable). Figure 3 shows the same relationship for WRITE cycles. If the chip enable duty cycle is less than 100%, only standby current is drawn when the chip is disabled. The overall average current drawn by the STK1743 depends on the following items: 1) CMOS vs. TTL input levels; 2) the duty cycle of chip enable; 3) the overall cycle rate for accesses; 4) the ratio of READs to WRITEs; 5) the operating temperature; 6) the V_{CC} level; and 7) I/O loading.

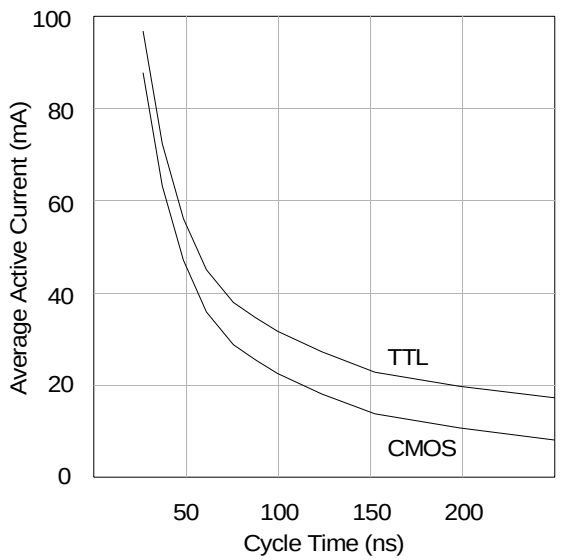


Figure 2: I_{CC} (max) Reads

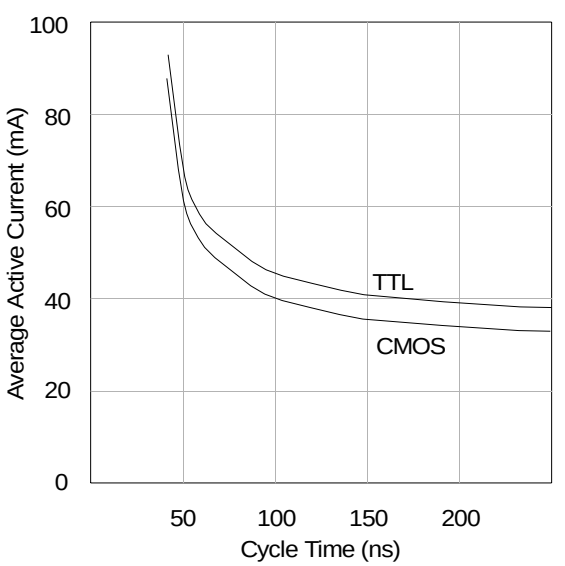


Figure 3: I_{CC} (max) Writes

ORDERING INFORMATION

STK1743 - D 25 I

Temperature Range

Blank = Commercial (0 to 70°C)

I = Industrial (–40 to 85°C)

Access Time

25 = 25ns

35 = 35ns

45 = 45ns

Package

D = 600 mil Dual In-Line Module