Ordering number : EN2131B

Thick Film Hybrid IC

STK4026V

AF Power Amplifier (Split Power Supply) (25W min, THD = 0.08%)

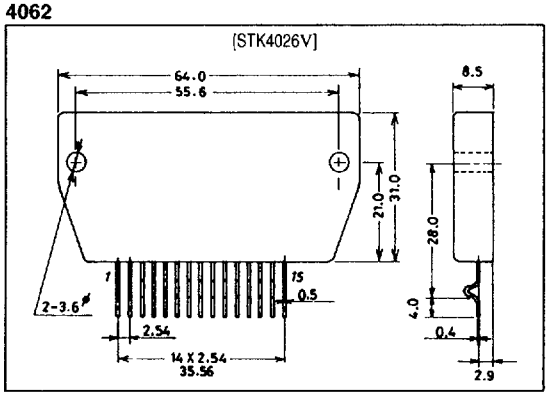
Features

- Small-sized package permitting audio sets to be made slimmer (up to 70W)
- The STK4024V series are available for output 20W to 100W (200W) and are pin-compatible. (120W to 200W : 18pins)
- Facilitates thermal design of slim stereo sets.
- Distortion 0.08% due to current mirror circuit
- Possible to design electronic supplementary circuits (pop noise muting at the time of power ON/OFF, load short protector, thermal shutdown)

Package Dimensions

unit: mm

4062



Specifications

Maximum Ratings at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	V_{CC} max		±39	V
Thermal resistance	θj-c		2.1	°C/W
Junction temperature	Tj		150	°C
Operating substrate temperature	Tc		125	°C
Storage temperature	Tstg		–30 to +125	°C
Available time for load short-circuit	t_s *1	V_{CC} = ±26V, R_L = 8Ω, f = 50Hz, P_O = 25W	2	s

Recommended Operating Conditions at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Recommended supply voltage	V_{CC}		±26	V
Load resistance	R_L		8	Ω

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Operating Characteristics

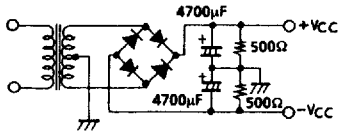
at Ta = 25°C, V_{CC} = ±26V, R_L = 8Ω, VG = 40dB, Rg = 600Ω, 100kHz LPF ON, R_L : non-inductive load

Parameter	Symbol	Conditions	min	typ	max	Unit
Quiescent current	I_{CCO}	V_{CC} = ±30V	15		120	mA
Output power	P_O (1)	THD = 0.08%, f = 20Hz to 20kHz	25			W
	P_O (2)	V_{CC} = ±22V, THD = 0.2%, R_L = 4Ω, f = 1kHz	30			W
Total harmonic distortion	THD	P_O = 1.0W, f = 1kHz			0.08	%
Frequency response	f_L, f_H	P_O = 1.0W, $^{+0}_{-3}$ dB		20 to 50k		Hz
Input impedance	r_i	P_O = 1.0W, f = 1kHz		55		kΩ
Output noise voltage	V_{NO} *2	V_{CC} = ±30V, Rg = 10kΩ			1.2	mVrms
Neutral voltage	V_N	V_{CC} = ±30V	-70	0	+70	mV

Notes. For power supply at the time of test, use a constant-voltage power supply unless otherwise specified.

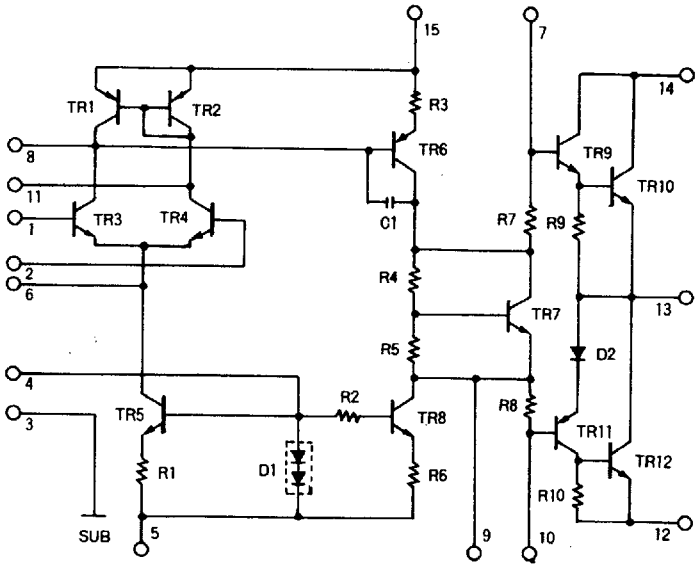
*1 For measurement of the available time for load short-circuit and output noise voltage, use the specified transformer power supply shown right.

*2 The output noise voltage is represented by the peak value on rms scale (VTVM) of average value indicating type. The noise voltage waveform includes no flicker noise.

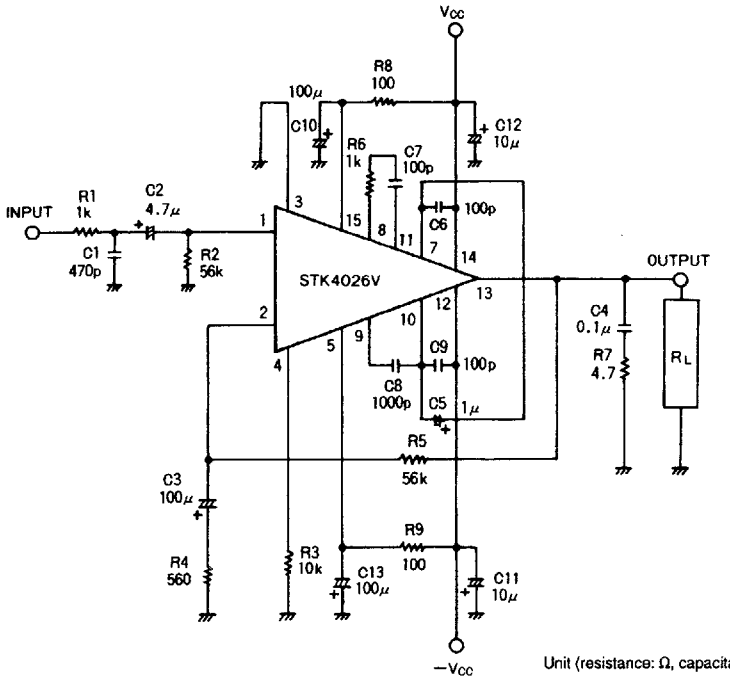


Specified Transformer Power Supply
(Equivalent to RP-25)

Equivalent Circuit

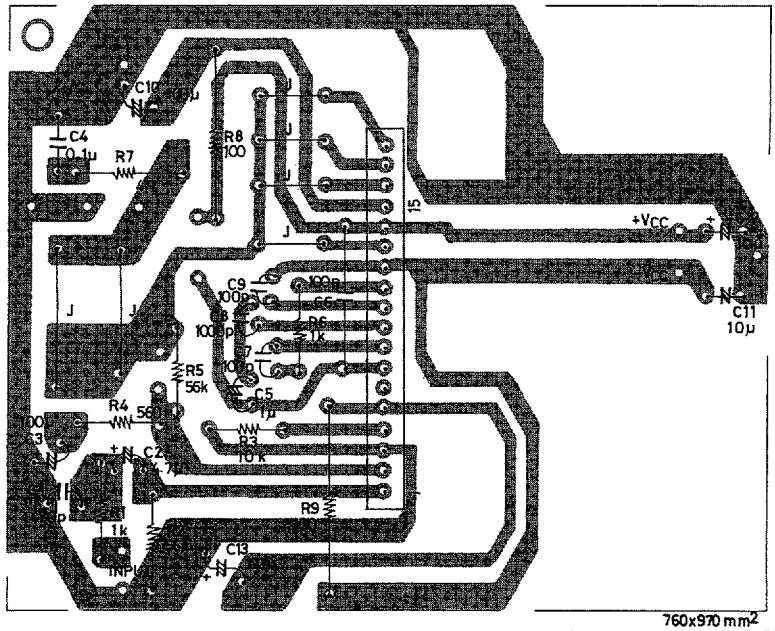


Sample Application Circuit : 25W min Single-Channel AF Power Amplifier



Unit (resistance: Ω, capacitance: F)

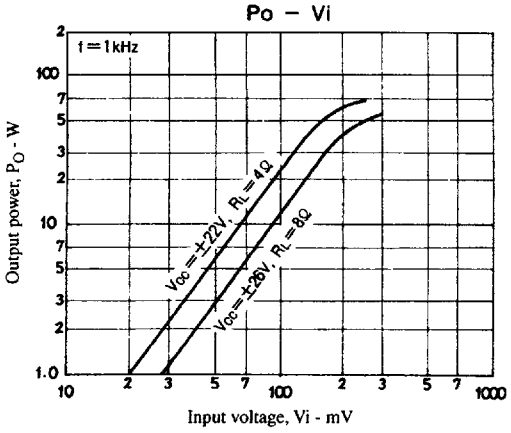
Sample Printed Circuit Pattern for Application Circuit (Cu-foiled side)



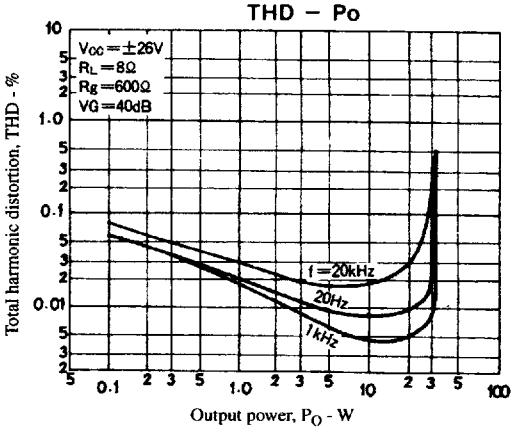
760x970 mm²

Unit (resistance: Ω, capacitance: F)

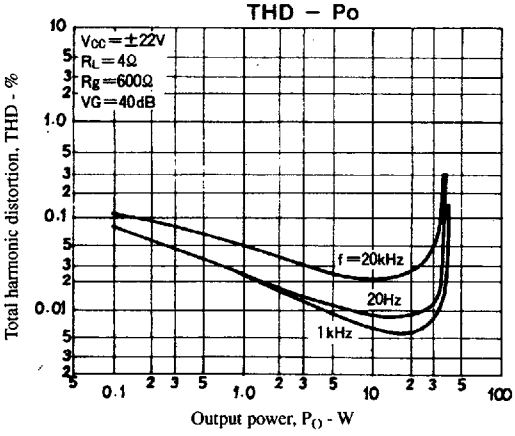
Po – Vi



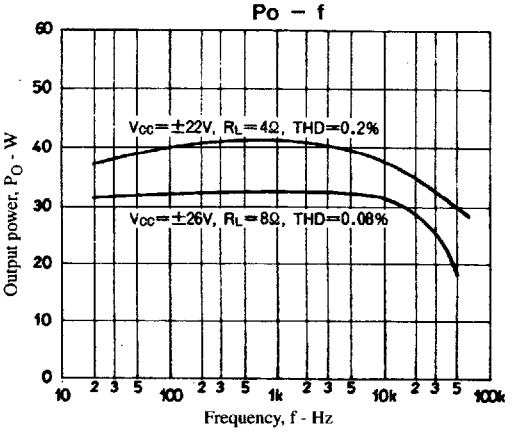
THD – Po



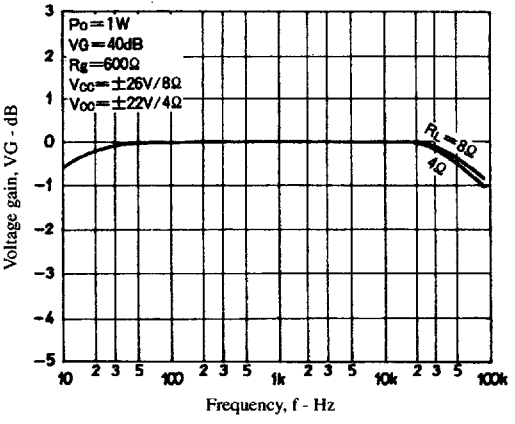
THD – Po



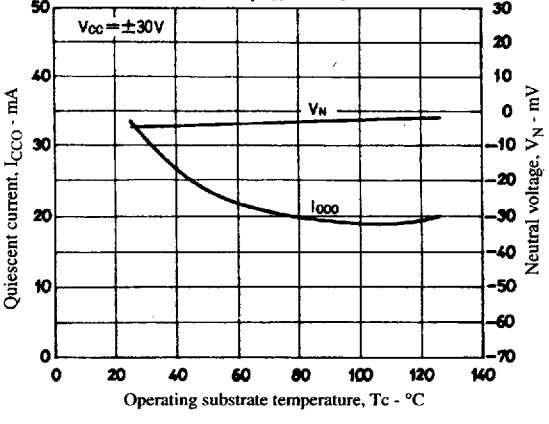
Po – f

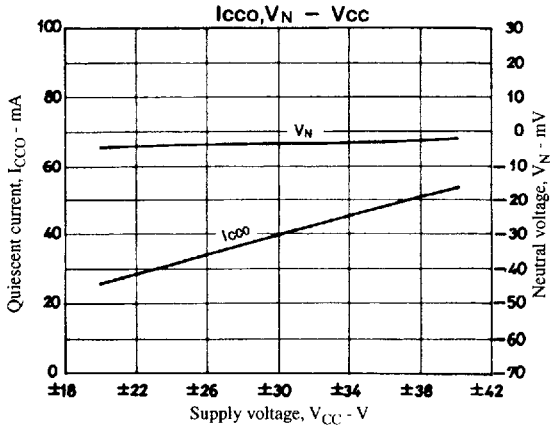


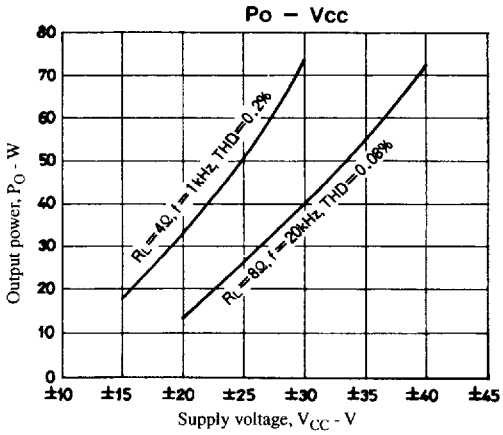
VG – f

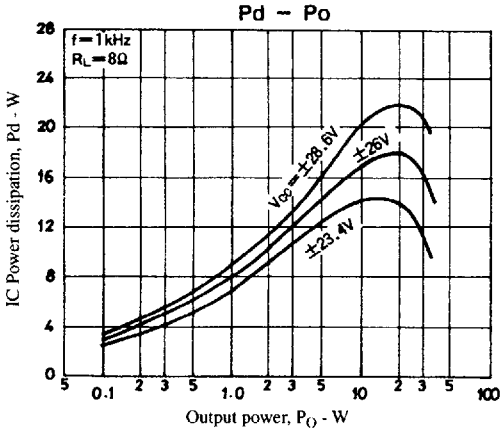


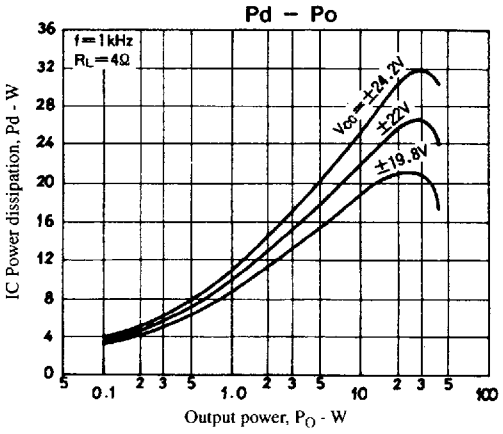
ICCO,VN – Tc

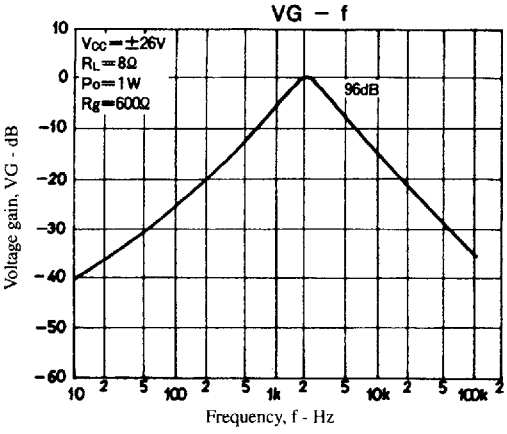


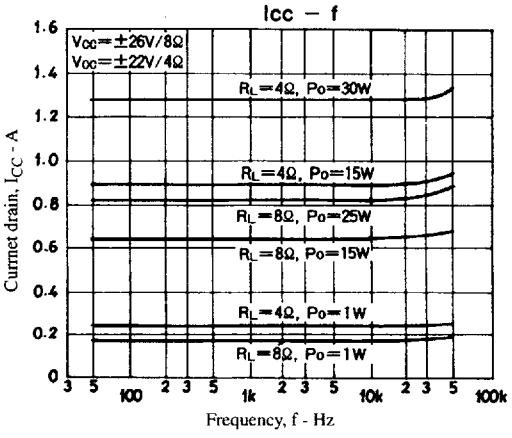


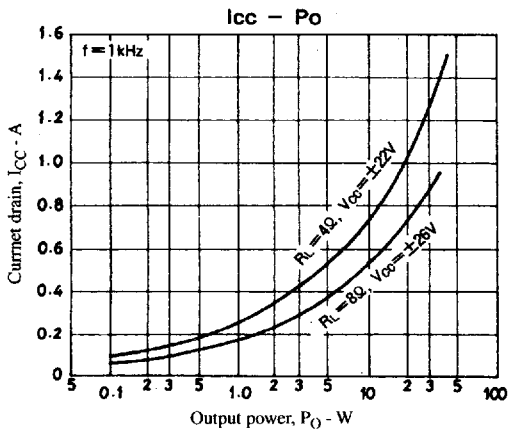


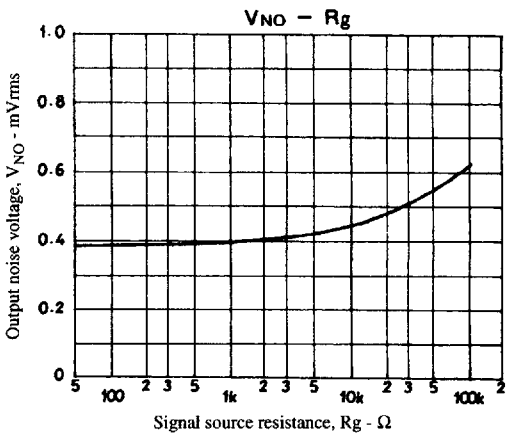




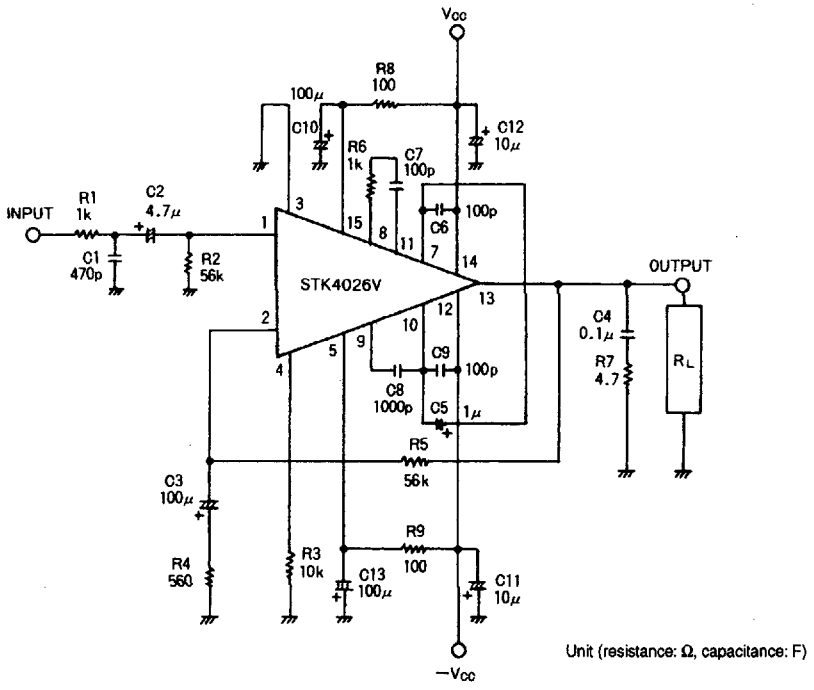


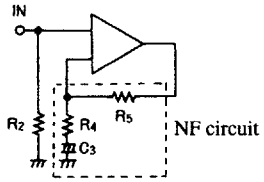




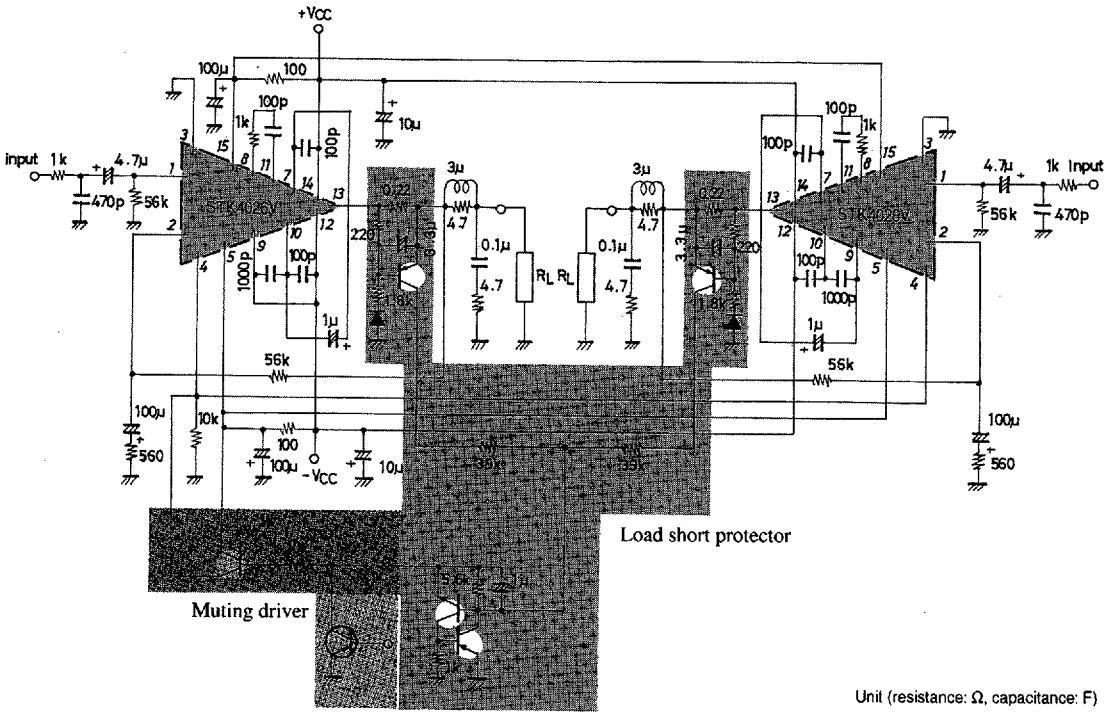


Description of External Parts



R1, C1	Input filter circuit • Used to reduce noise at high frequencies.
C2 -	Input coupling capacitor • Used to block DC current. When the reactance of the capacitor increases at low frequencies, the dependence of 1/f noise on signal source resistance causes the output noise to worsen. It is better to decrease the reactance.
R2	Input bias resistor • Used to bias the input pin to zero. • Affects V_N stability. (See NF circuit.) • Because of differential input, this resistor fixes the input resistance practically.
R4, R5 C3 (R2)	NFB circuit (AC NF circuit). It is desirable that the error of the resistor value is 1% or less.  C3 : Capacitor for AC NF R4, R5 : Used to set VG • VG setting obtained by using R4, R5 $\log 20 \cdot \frac{R_5}{R_4}$ 40dB is recommended. • Low cutoff frequency setting obtained by using, R4, C3. $f_L = \frac{1}{2\pi \cdot R_4 \cdot C_3}$ [Hz] To change VG setting, it is desirable to change R4. In this case, the low cutoff frequency setting needs to be rechecked. When VG setting is changed by changing R5, R5 must be made equal to R2 to ensure V_N balance. If the resistor value is increased more than the existing value, it may be hard to ensure V_N balance and the temperature characteristic of V_N may be also deteriorated.
R3	Differential constant-current bias resistor
R6, R7	Used for oscillation blocking and phase compensation
R7, C4	Used for oscillation blocking and phase compensation (C4 : A polyester film capacitor is recommended.)
C6, C9	Used for oscillation blocking and phase compensation Power amp stage (Must be connected near the pin) C6 : Power amp on (+) side C9 : Power amp on (–) side
C8	Used for oscillation blocking and phase compensation (Used for oscillation blocking before clip at power amp stage)
C5	Used for oscillation blocking and distortion improvement
R8, C10	Ripple filter circuit on (+) side
R9, C13	Ripple filter circuit on (–) side
C11, C12	Used for oscillation blocking • Used to decrease the power supply impedance to operate the IC stably. Must be connected near the IC pin. It is desirable to use an electrolytic capacitor.

Sample Application Circuit (protection circuit and muting circuit)



Unit (resistance: Ω, capacitance: F)

Thermal Design

The IC power dissipation of the STK4026V at the IC-operated mode is 17.8W max. at load resistance 8Ω and 26.4W max. at load resistance 4Ω for continuous sine wave as shown in Figure 1 and 2.

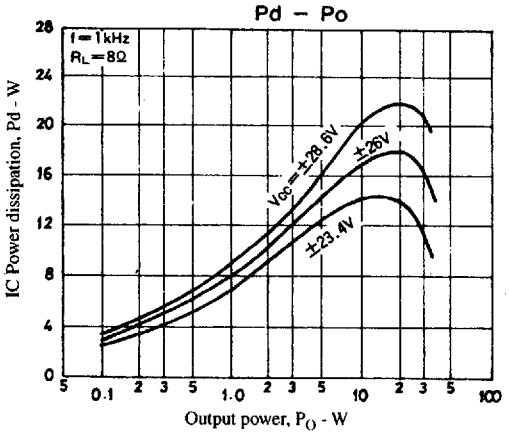


Figure 1. STK4026V Pd – P_O (R_L = 8Ω)

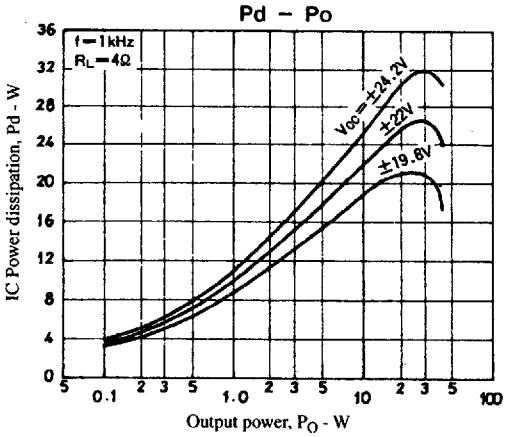


Figure 2. STK4026V Pd – P_O (R_L = 4Ω)

In an actual application where a music signal is used, it is impractical to estimate the power dissipation based on the continuous signal as shown in Figure 1 and 2, because too large a heat sink must be used. It is reasonable to estimate the power dissipation as 1/10 Po max. (EIAJ).
That is, Pd = 11.1W at 8Ω, Pd = 15.2W at 4Ω
Thermal resistance θc-a of a heat sink for this IC power dissipation (Pd) is fixed under conditions 1 and 2 shown below.

Condition 1: $Tc = Pd \times \theta c\text{-}a + Ta \leq 125°C$ ..... (1)
where Ta : Specified ambient temperature
Tc : Operating substrate temperature

Condition 2: $Tj = Pd \times (\theta c\text{-}a) + Pd/2 \times (\theta j\text{-}c) + Ta \leq 150°C$ ..... (2)
where Tj : Junction temperature of power transistor

Assuming that the power dissipation is shared equally between the two power transistors, thermal resistance θj-c is 2.1°C/W and

$$Pd \times (\theta c\text{-}a + 2.1/2) + Ta \leq 150°C \quad \text{..... (3)}$$

Thermal resistance θc-a of a heat sink must satisfy inequalities (1) and (3).
Figure 3 shows the relation between Pd and θc-a given from (1) and (3) with Ta as a parameter.

[Example] The thermal resistance of a heat sink is obtained when the ambient temperature specified for a stereo amplifier is 50°C.
Assuming $V_{CC} = \pm 26V$, $R_L = 8\Omega$,
$V_{CC} = \pm 22V$, $R_L = 4\Omega$,
$R_L = 8\Omega$: Pd1 = 11.1W at 1/10 Po max.
$R_L = 4\Omega$: Pd2 = 15.2W at 1/10 Po max.
The thermal resistance of a heat sink is obtained from Figure 3.
$R_L = 8\Omega$: θc-a1 = 6.76°C/W
$R_L = 4\Omega$: θc-a2 = 4.93°C/W
Tj when a heat sink is used is obtained from (3).
$R_L = 8\Omega$: Tj = 136.7°C
$R_L = 4\Omega$: Tj = 140.9°C

This design is based on the use of a constant-voltage regulated power supply. Pd differs when a transformer power supply is used. Redesign must be made based on Pd that suits the regulation of each transformer.

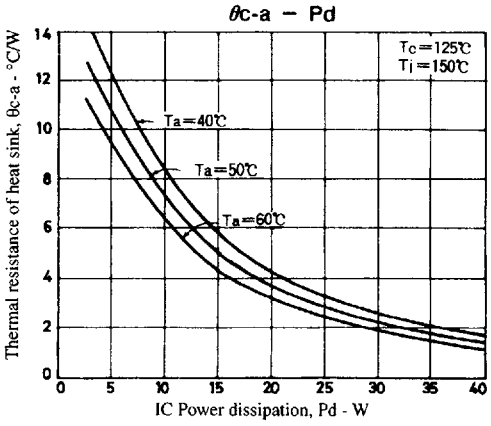


Figure 3. STK4026V θc-a – Pd