

# STK551U362A-E

## Intelligent Power Module (IPM) 600 V, 10 A



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### Overview

This “Inverter Power IPM” is highly integrated device containing all High Voltage (HV) control from HV-DC to 3-phase outputs in a single SIP module (Single-In line Package). Output stage uses IGBT / FRD technology and implements Under Voltage Protection (UVP) and Over Current Protection (OCP) with a Fault Detection output flag. Internal Boost diodes are provided for high side gate boost drive.

### Function

- Single control power supply due to Internal bootstrap circuit for high side pre-driver circuit
- All control input and status output are at low voltage levels directly compatible with microcontrollers
- Built-in dead time for shoot-thru protection
- Externally accessible embedded thermistor for substrate temperature measurement
- The level of the over-current protection current is adjustable with the external resistor, “RSD”

### Certification

- UL1557 (File Number : E339285)

### Specifications

#### Absolute Maximum Ratings at Tc = 25°C

| Parameter                  | Symbol             | Conditions                                                          | Ratings                 | Unit |
|----------------------------|--------------------|---------------------------------------------------------------------|-------------------------|------|
| Supply voltage             | V <sub>CC</sub>    | V+ to V-, surge < 500 V *1                                          | 450                     | V    |
| Collector-emitter voltage  | V <sub>CE</sub>    | V+ to U, V, W or U, V, W to V-                                      | 600                     | V    |
| Output current             | I <sub>o</sub>     | V+, V-, U, V, W terminal current                                    | ±10                     | A    |
|                            |                    | V+, V-, U, V, W terminal current at Tc = 100°C                      | ±5                      | A    |
| Output peak current        | I <sub>op</sub>    | V+, V-, U, V, W terminal current for a Pulse width of 1ms.          | ±20                     | A    |
| Pre-driver voltage         | VD1,2,3,4          | VB1 to U, VB2 to V, VB3 to W, V <sub>DD</sub> to V <sub>SS</sub> *2 | 20                      | V    |
| Input signal voltage       | V <sub>IN</sub>    | HIN1, 2, 3, LIN1, 2, 3                                              | -0.3 to V <sub>DD</sub> | V    |
| FAULT terminal voltage     | V <sub>FAULT</sub> | FAULT terminal                                                      | -0.3 to V <sub>DD</sub> | V    |
| Maximum power dissipation  | P <sub>d</sub>     | IGBT per channel                                                    | 30                      | W    |
| Junction temperature       | T <sub>j</sub>     | IGBT, FRD                                                           | 150                     | °C   |
| Storage temperature        | T <sub>stg</sub>   |                                                                     | -40 to +125             | °C   |
| Operating case temperature | T <sub>c</sub>     | IPM case temperature                                                | -40 to +100             | °C   |
| Tightening torque          |                    | Case mounting screws *3                                             | 1.0                     | Nm   |
| Withstand voltage          | V <sub>is</sub>    | 50 Hz sine wave AC 1 minute *4                                      | 2000                    | VRMS |

Reference voltage is “V<sub>SS</sub>” terminal voltage unless otherwise specified.

\*1: Surge voltage developed by the switching operation due to the wiring inductance between + and U-(V-, W-) terminal.

\*2: Terminal voltage: VD1 = VB1 to U, VD2 = VB2 to V, VD3 = VB3 to W, VD4 = V<sub>DD</sub> to V<sub>SS</sub>

\*3: Flatness of the heat-sink should be 0.15 mm and below.

\*4: Test conditions : AC 2500 V, 1 second.

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

### ORDERING INFORMATION

See detailed ordering and shipping information on page 15 of this data sheet.

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**Electrical Characteristics** at Tc = 25°C, VD1, VD2, VD3, VD4 = 15 V

| Parameter                                                     | Symbol                                   | Conditions                                   |               | Test circuit | Ratings |      |      | Unit |
|---------------------------------------------------------------|------------------------------------------|----------------------------------------------|---------------|--------------|---------|------|------|------|
|                                                               |                                          |                                              |               |              | min     | typ  | max  |      |
| Power output section                                          |                                          |                                              |               |              |         |      |      |      |
| Collector-emitter cut-off current                             | I <sub>CE</sub>                          | V <sub>CE</sub> = 600 V                      |               | Fig.1        | -       | -    | 0.1  | mA   |
| Bootstrap diode reverse current                               | IR(BD)                                   | VR(BD)                                       |               |              | -       | -    | 0.1  | mA   |
| Collector to emitter saturation voltage                       | V <sub>CE</sub> (SAT)                    | Io = 10 A<br>Tj = 25°C                       | Upper side    | Fig.2        | -       | 1.8  | 2.4  | V    |
|                                                               |                                          |                                              | Lower side *1 |              | -       | 2.1  | 2.7  |      |
|                                                               |                                          | Io = 5 A<br>Tj = 100°C                       | Upper side    |              | -       | 1.3  | -    |      |
|                                                               |                                          |                                              | Lower side *1 |              | -       | 1.6  | -    |      |
| Diode forward voltage                                         | V <sub>F</sub>                           | Io = 10 A<br>Tj = 25°C                       | Upper side    | Fig.3        | -       | 1.8  | 2.3  | V    |
|                                                               |                                          |                                              | Lower side *1 |              | -       | 2.1  | 2.6  |      |
|                                                               |                                          | Io = 5 A<br>Tj = 100°C                       | Upper side    |              | -       | 1.3  | -    |      |
|                                                               |                                          |                                              | Lower side *1 |              | -       | 1.6  | -    |      |
| Junction to case thermal resistance                           | θj-c(T)                                  | IGBT                                         |               |              | -       | -    | 4    | °C/W |
|                                                               | θj-c(D)                                  | FRD                                          |               |              | -       | -    | 5    |      |
| Control (Pre-driver) section                                  |                                          |                                              |               |              |         |      |      |      |
| Pre-driver power dissipation                                  | ID                                       | VD1, 2, 3 = 15 V                             |               | Fig.4        | -       | 0.08 | 0.4  | mA   |
|                                                               |                                          | VD4 = 15 V                                   |               |              | -       | 1.6  | 4    |      |
| High level Input voltage                                      | Vin H                                    | HIN1, HIN2, HIN3,<br>LIN1, LIN2, LIN3 to VSS |               |              | 2.5     | -    | -    | V    |
| Low level Input voltage                                       | Vin L                                    |                                              |               |              | -       | -    | 0.8  | V    |
| Input threshold voltage hysteresis *1                         | Vinth(hys)                               |                                              |               |              | 0.5     | 0.8  | -    | V    |
| Logic 1 input leakage current                                 | I <sub>IN+</sub>                         | VIN = +3.3 V                                 |               |              | -       | 100  | 143  | μA   |
| Logic 0 input leakage current                                 | I <sub>IN-</sub>                         | VIN = 0 V                                    |               |              | -       | -    | 2    | μA   |
| FAULT terminal input electric current                         | IoSD                                     | FAULT : ON / VFAULT = 0.1 V                  |               |              | -       | 2    | -    | mA   |
| FAULT clear time                                              | FLTCLR                                   | Fault output latch time.                     |               |              | 18      | -    | 80   | ms   |
| V <sub>CC</sub> and VS undervoltage positive going threshold. | V <sub>CCUV+</sub><br>V <sub>SUV+</sub>  |                                              |               |              | 10.5    | 11.1 | 11.7 | V    |
| V <sub>CC</sub> and VS undervoltage negative going threshold. | V <sub>CCUV-</sub><br>V <sub>SUV-</sub>  |                                              |               |              | 10.3    | 10.9 | 11.5 | V    |
| V <sub>CC</sub> and VS undervoltage hysteresis                | V <sub>CCUVH</sub><br>V <sub>SUVH-</sub> |                                              |               |              | 0.14    | 0.2  | -    | A    |
| Over current protection level                                 | ISD                                      | PW = 100 μs, RSD = 0 Ω                       |               | Fig.5        | 18.1    | -    | 22.9 | A    |
| Output level for current monitor                              | ISO                                      | Io = 10 A                                    |               |              | 0.31    | 0.33 | 0.35 | V    |
| Thermistor for substrate temperature                          | Rt                                       | Thermistor Resistance at 25°C (Vth)          |               |              | 90      | 100  | 110  | kΩ   |

Reference voltage is " $V_{SS}$ " terminal voltage unless otherwise specified.

\*1 : The lower side's  $V_{CE(SAT)}$  and  $V_F$  include a loss by the shunt resistance

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| Parameter                          | Symbol | Conditions                                                               | Test circuit | Ratings     |     |     | Unit |    |
|------------------------------------|--------|--------------------------------------------------------------------------|--------------|-------------|-----|-----|------|----|
|                                    |        |                                                                          |              | min         | typ | max |      |    |
| Switching Character                |        |                                                                          |              |             |     |     |      |    |
| Switching time                     | tON    | Io = 10 A                                                                | Fig.6        | 0.3         | 0.6 | 1.3 | μs   |    |
|                                    | tOFF   | Inductive load                                                           |              | -           | 1.0 | 1.8 |      |    |
| Turn-on switching loss             | Eon    | Ic = 5 A, V <sup>+</sup> = 300 V,<br>VDD = 15 V, L = 3.9 mH<br>Tc = 25°C |              | -           | 100 | -   | μJ   |    |
| Turn-off switching loss            | Eoff   |                                                                          |              | -           | 110 | -   | μJ   |    |
| Total switching loss               | Etot   |                                                                          |              | -           | 210 | -   | μJ   |    |
| Turn-on switching loss             | Eon    | Ic = 5 A, V <sup>+</sup> = 300 V,<br>VDD = 15V, L = 3.9mH<br>Tc = 100°C  |              | -           | 110 | -   | μJ   |    |
| Turn-off switching loss            | Eoff   |                                                                          |              | -           | 230 | -   | μJ   |    |
| Total switching loss               | Etot   |                                                                          |              | -           | 340 | -   | μJ   |    |
| Diode reverse recovery energy      | Erec   | IF = 5 A, V <sup>+</sup> = 400 V, VDD = 15 V,<br>L = 3.9 mH, Tc = 100°C  |              |             | -   | 10  | -    | μJ |
| Diode reverse recovery time        | Trr    |                                                                          |              |             | -   | 50  | -    | ns |
| Reverse bias safe operating area   | RBSOA  | Io = 20 A, VCE = 450 V                                                   |              | Full square |     |     |      |    |
| Short circuit safe operating area  | SCSOA  | VCE = 400 V, Tc = 100°C                                                  |              | 4           | -   | -   | μs   |    |
| Allowable offset voltage slew rate | dv/dt  | Between U, V, W to U-, V-, W-                                            |              | −50         | -   | 50  | V/ns |    |

Reference voltage is "V<sub>SS</sub>" terminal voltage unless otherwise specified.

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

## Notes :

- When the internal protection circuit operates, a Fault signal is turned ON (When the Fault terminal is low level, Fault signal is ON state : output form is open DRAIN) but the Fault signal does not latch. After protection operation ends, it returns automatically within about 18 ms to 80 ms and resumes operation beginning condition. So, after Fault signal detection, set all input signals to OFF (Low) at once. However, the operation of pre-drive power supply low voltage protection (UVLO : with hysteresis about 0.2 V) is as follows.

### Upper side :

The gate is turned off and will return to regular operation when recovering to the normal voltage, but the latch will continue till the input signal will turn 'low'.

### Lower side :

The gate is turned off and will automatically reset when recovering to normal voltage. It does not depend on input signal voltage.

- When assembling the IPM on the heat sink with M3 type screw, tightening torque range is 0.6 Nm to 0.9 Nm.
- The pre-drive low voltage protection is the feature to protect devices when the pre-driver supply voltage falls due to an operating malfunction.

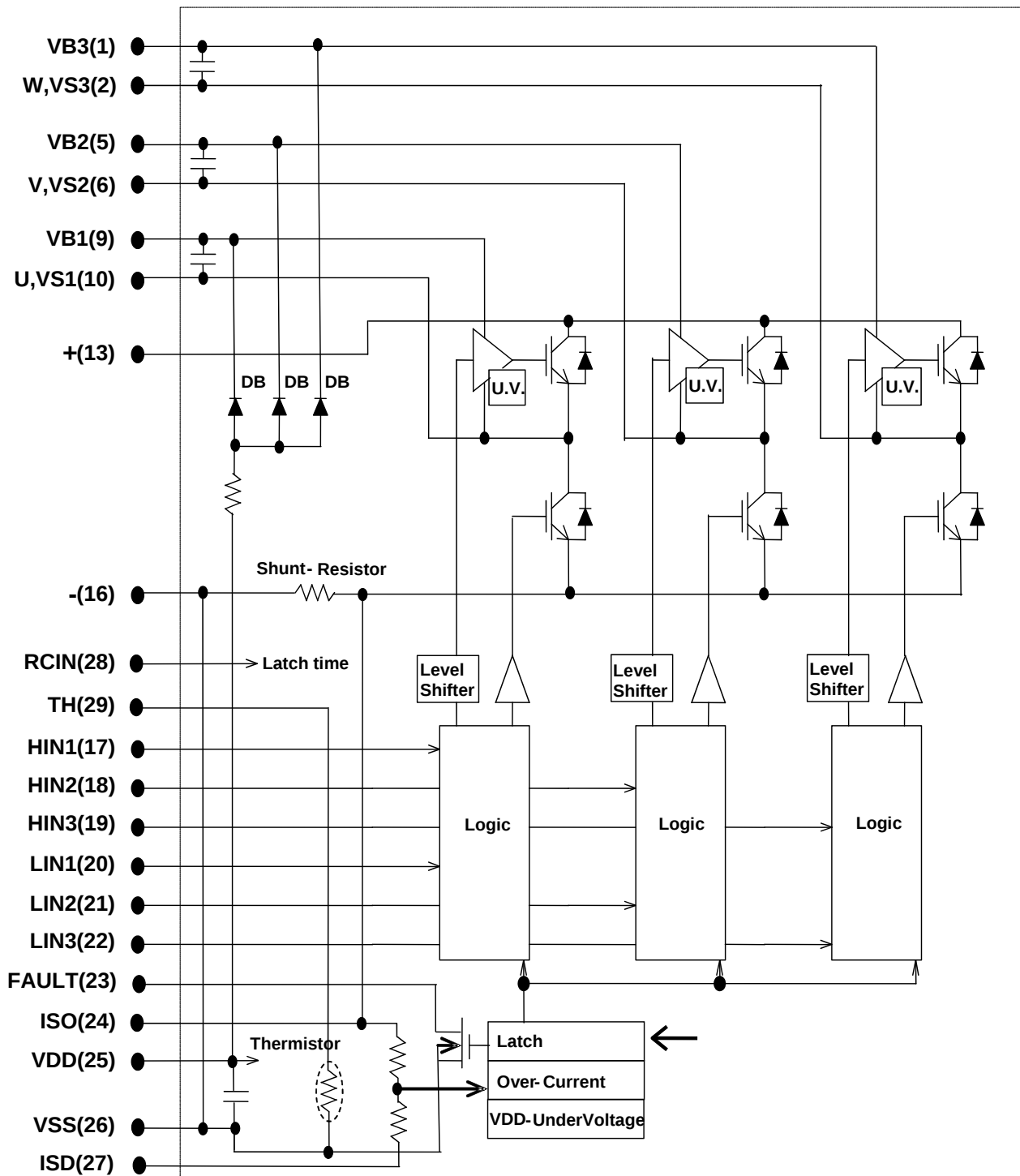
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## Module Pin-Out Description

| Pin | Name   | Description                                         |
|-----|--------|-----------------------------------------------------|
| 1   | VB3    | High Side Floating Supply Voltage 3                 |
| 2   | W, VS3 | Output 3 - High Side Floating Supply Offset Voltage |
| 3   | —      | Without Pin                                         |
| 4   | —      | Without Pin                                         |
| 5   | VB2    | High Side Floating Supply voltage 2                 |
| 6   | V, VS2 | Output 2 - High Side Floating Supply Offset Voltage |
| 7   | —      | Without Pin                                         |
| 8   | —      | Without Pin                                         |
| 9   | VB1    | High Side Floating Supply voltage 1                 |
| 10  | U, VS1 | Output 1 - High Side Floating Supply Offset Voltage |
| 11  | —      | Without Pin                                         |
| 12  | —      | none                                                |
| 13  | V+     | Positive Bus Input Voltage                          |
| 14  | NA     | none                                                |
| 15  | NA     | none                                                |
| 16  | V-     | Negative Bus Input Voltage                          |
| 17  | HIN1   | Logic Input High Side Gate Driver - Phase 1         |
| 18  | HIN2   | Logic Input High Side Gate Driver - Phase V         |
| 19  | HIN3   | Logic Input High Side Gate Driver - Phase W         |
| 20  | LIN1   | Logic Input Low Side Gate Driver - Phase U          |
| 21  | LIN2   | Logic Input Low Side Gate Driver - Phase V          |
| 22  | LIN3   | Logic Input Low Side Gate Driver - Phase W          |
| 23  | FLTEN  | Enable input / Fault output                         |
| 24  | ISO    | Current monitor output                              |
| 25  | VDD    | +15 V Main Supply                                   |
| 26  | VSS    | Negative Main Supply                                |
| 27  | ISD    | Over current detection and setting                  |
| 28  | RCIN   | Fault clear time setting output                     |
| 29  | TH     | Thermistor output                                   |

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## Equivalent Block Diagram



## Test Circuit

(The tested phase : U+ shows the upper side of the U phase and U- shows the lower side of the U phase.)

### ■ $I_{CE}$ / $I_R(BD)$

|   | U+ | V+ | W+ | U- | V- | W- |
|---|----|----|----|----|----|----|
| M | 13 | 13 | 13 | 10 | 6  | 2  |
| N | 10 | 6  | 2  | 16 | 16 | 16 |

|   | U(BD) | V(BD) | W(BD) |
|---|-------|-------|-------|
| M | 9     | 5     | 1     |
| N | 26    | 26    | 26    |

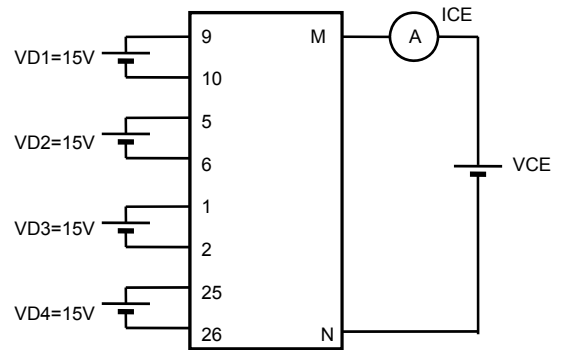


Fig. 1

### ■ $V_{CE(SAT)}$ (Test by pulse)

|   | U+ | V+ | W+ | U- | V- | W- |
|---|----|----|----|----|----|----|
| M | 13 | 13 | 13 | 10 | 6  | 2  |
| N | 10 | 6  | 2  | 16 | 16 | 16 |
| m | 17 | 18 | 19 | 20 | 21 | 22 |

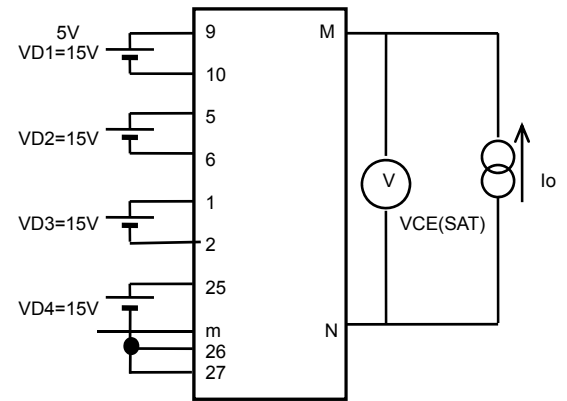


Fig. 2

### ■ $V_F$ (Test by pulse)

|   | U+ | V+ | W+ | U- | V- | W- |
|---|----|----|----|----|----|----|
| M | 13 | 13 | 13 | 10 | 6  | 2  |
| N | 10 | 6  | 2  | 16 | 16 | 16 |

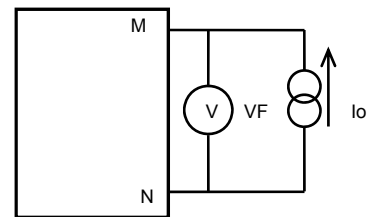


Fig. 3

### ■ $I_D$

|   | VD1 | VD2 | VD3 | VD4 |
|---|-----|-----|-----|-----|
| M | 9   | 5   | 1   | 25  |
| N | 10  | 6   | 2   | 26  |

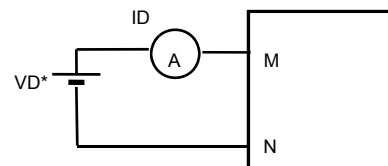


Fig. 4

## STK551U362A-E

### ■ ISD

Input signal

(0 to 5 V)

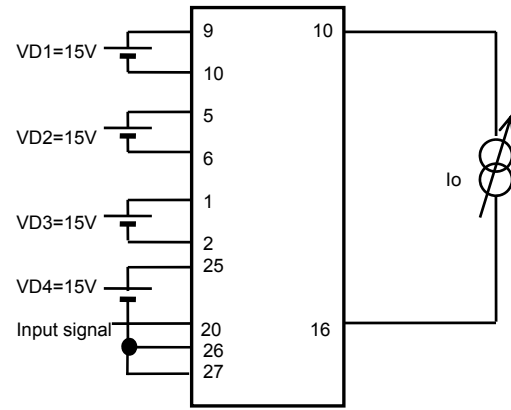
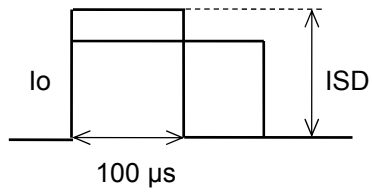


Fig. 5

### ■ Switching time (The circuit is a representative example of the lower side U phase.)

Input signal  
(0 to 5 V)

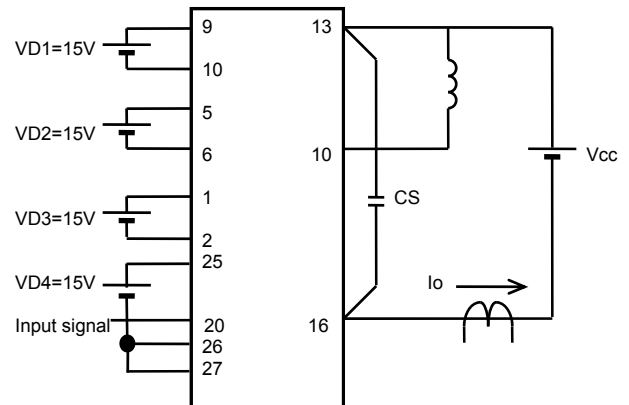
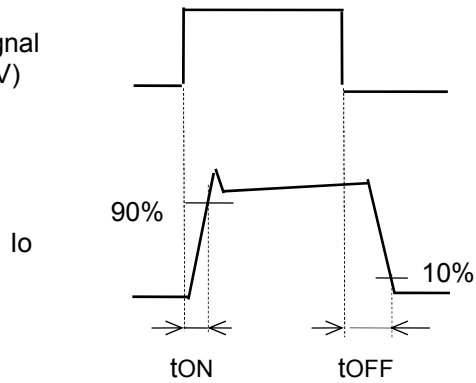


Fig. 6

Logic Timing Chart

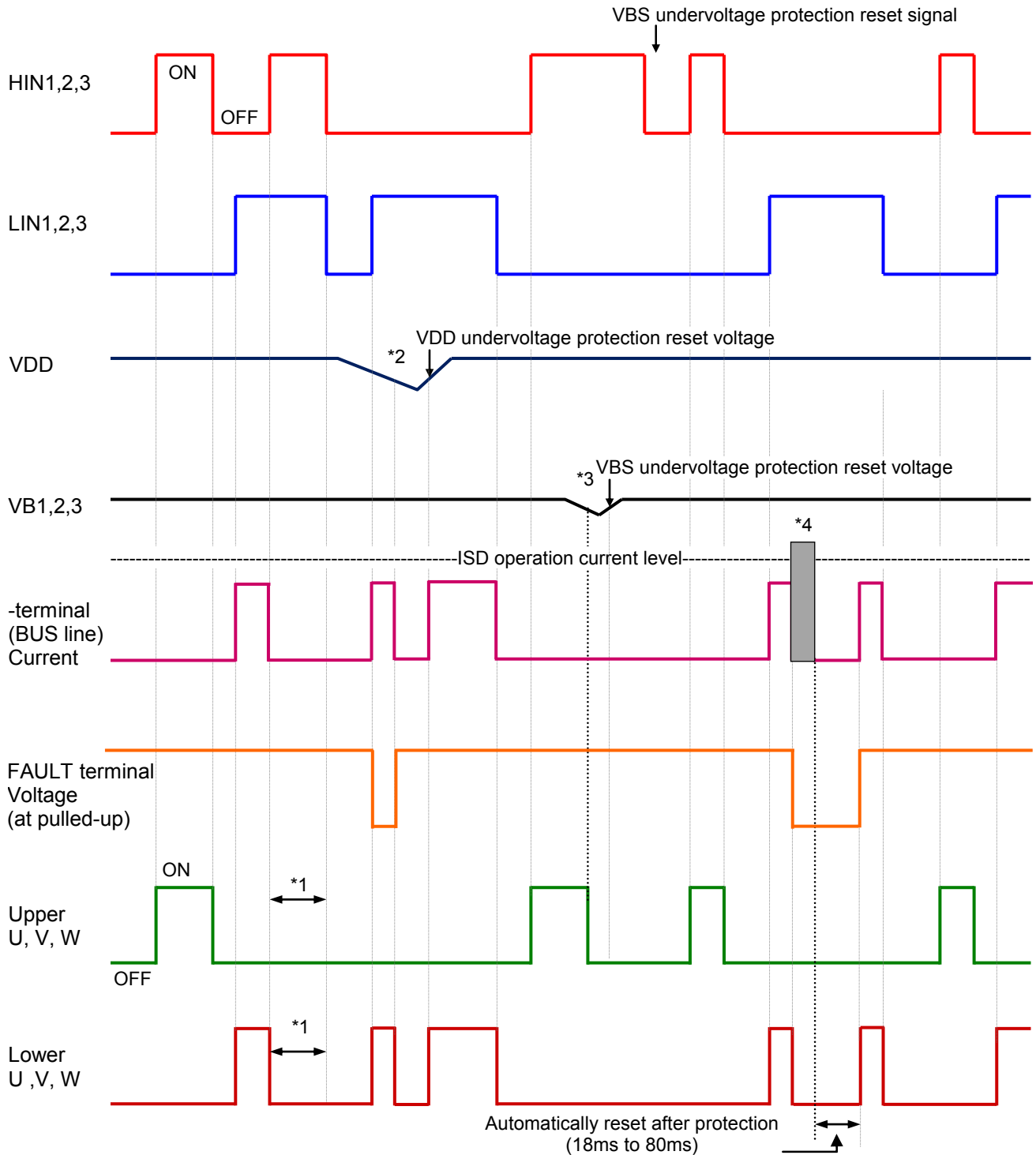
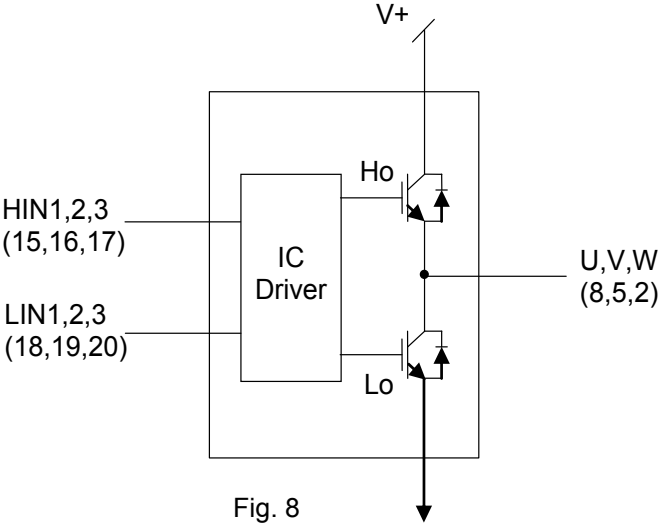


Fig. 7

Notes

- \*1 : Diagram shows the prevention of shoot-through via control logic. More dead time to account for switching delay needs to be added externally.
- \*2 : When  $V_{DD}$  decreases all gate output signals will go low and cut off all of 6 IGBT outputs. part. When  $V_{DD}$  rises the operation will resume immediately.
- \*3 : When the upper side gate voltage at VB1, VB2 and VB3 drops only, the corresponding upper side output is turned off. The outputs return to normal operation immediately after the upper side gat voltage rises.
- \*4 : In case of over current detection, all IGBT's are turned off and the FAULT output is asserted. Normal operation resumes in 18 to 80 ms after the over current condition is removed.

Logic level table



| FLTEN | Itrip | HIN1,2,3 | LIN1,2,3 | U,V,W |
|-------|-------|----------|----------|-------|
| 1     | 0     | 1        | 0        | Vbus  |
| 1     | 0     | 0        | 1        | 0     |
| 1     | 0     | 0        | 0        | Off   |
| 1     | 0     | 1        | 1        | Off   |
| 1     | 1     | X        | X        | Off   |
| 0     | X     | X        | X        | Off   |

Sample Application Circuit

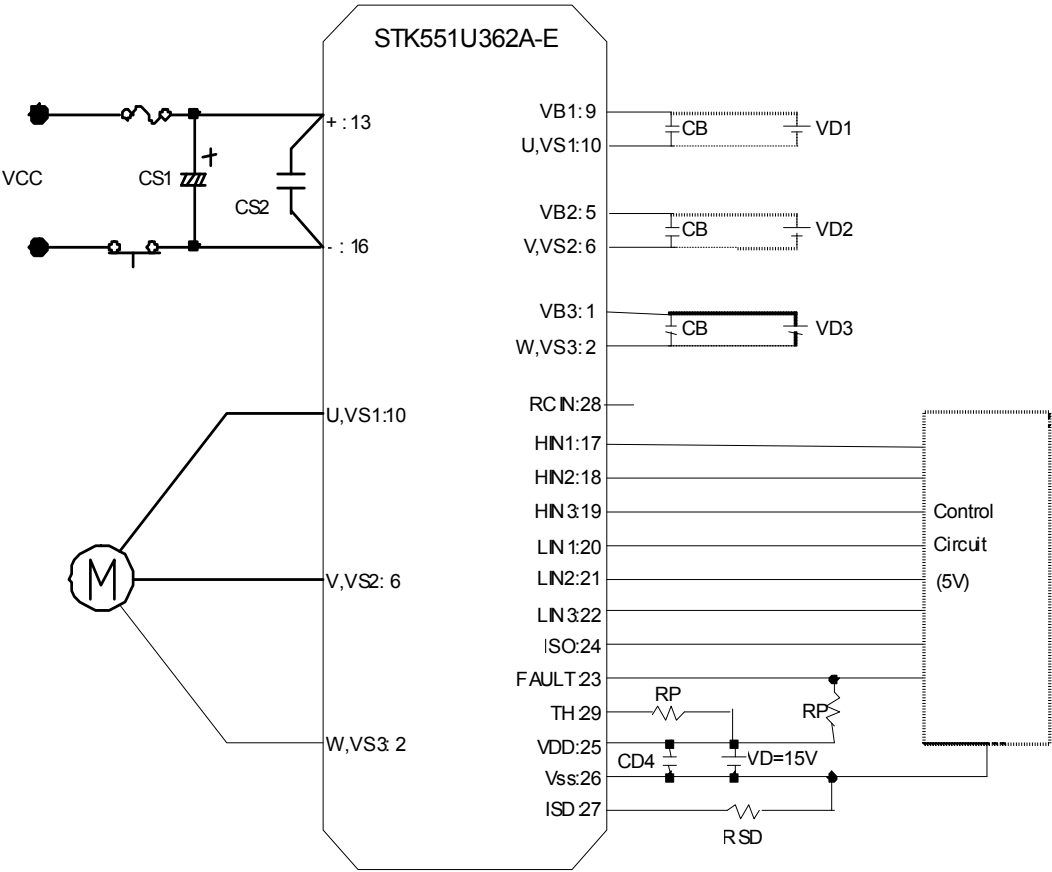


Fig. 9

**Recommended Operating Conditions** at T<sub>c</sub> = 25°C

| Item                        | Symbol                | Conditions                            | Ratings |     |      | Unit |
|-----------------------------|-----------------------|---------------------------------------|---------|-----|------|------|
|                             |                       |                                       | min     | typ | max  |      |
| Supply voltage              | V <sub>CC</sub>       | + to U-(V-,W-)                        | 0       | 280 | 450  | V    |
| Pre-driver supply voltage   | VD1,2,3               | VB1 to U, VB2 to V, VB3 to W          | 12.5    | 15  | 17.5 | V    |
|                             | VD4                   | V <sub>DD</sub> to V <sub>SS</sub> *1 | 13.5    | 15  | 16.5 |      |
| ON-state input voltage      | V <sub>IN</sub> (ON)  | HIN1, HIN2, HIN3,<br>LIN1, LIN2, LIN3 | 3.0     | -   | 5.0  | V    |
| OFF-state input voltage     | V <sub>IN</sub> (OFF) |                                       | 0       | -   | 0.3  |      |
| PWM frequency               | f <sub>PWM</sub>      |                                       | 1       | -   | 20   | kHz  |
| Dead time                   | DT                    | Turn-off to turn-on                   | 1.5     | -   | -    | μs   |
| Allowable input pulse width | P <sub>WIN</sub>      | ON and OFF                            | 1       | -   | -    | μs   |
| Tightening torque           |                       | 'M3' type screw                       | 0.6     | -   | 0.9  | Nm   |

\*1 : Pre-drive power supply (VD4 = 15 ±1.5 V) must be have the capacity of I<sub>o</sub> = 20 mA (DC), 0.5 A (Peak).

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

**Usage Precautions**

1. This IPM includes bootstrap diode and resistors. Therefore, by adding a capacitor "CB", a high side drive voltage is generated; each phase requires an individual bootstrap capacitor. The recommended value of CB is in the range of 1 to 47 μF, however this value needs to be verified prior to production. If selecting the capacitance more than 47 μF (±20%), connect a resistor (about 20 Ω) in series between each 3-phase upper side power supply terminals (VB1, 2, 3) and each bootstrap capacitor.  
When not using the bootstrap circuit, each upper side pre-drive power supply requires an external independent power supply.
2. It is essential that wiring length between terminals in the snubber circuit be kept as short as possible to reduce the effect of surge voltages. Recommended value of "CS" is in the range of 0.1 to 10 μF.
3. "ISO" (pin 24) is terminal for current monitor. When the pull-down resistor is used, please select it more than 5.6 kΩ
4. "FAULT" (pin 23) is open DRAIN output terminal. (Active Low). Pull up resistor is recommended more than 5.6 kΩ.
5. Inside the IPM, a thermistor used as the temperature monitor for internal substrate is connected between V<sub>SS</sub> terminal and TH terminal, therefore, an external pull up resistor connected between the TH terminal and an external power supply should be used. The temperature monitor example application is as follows, please refer the Fig.10, and Fig.11 below.
6. pull down resistor of 33 kΩ is provided internally at the signal input terminals. An external resistor of 2.2 k to 3.3 kΩ should be added to reduce the influence of external wiring noise.
7. The over-current protection feature is not intended to protect in exceptional fault condition. An external fuse is recommended for safety.
8. When "-" and "V<sub>SS</sub>" terminal are short-circuited on the outside, level that over-current protection (ISD) might be changed from designed value as IPM. Please check it in your set ("N" terminal and "V<sub>SS</sub>" terminal are connected in IPM).
9. The over-current protection function operates normally when an external resistor RSD is connected between ISD and V<sub>SS</sub> terminals. Be sure to connect this resistor. The level of the overcurrent protection can be changed according to the RSD value.
10. When input pulse width is less than 1.0 μs, an output may not react to the pulse. (Both ON signal and OFF signal)

This data shows the example of the application circuit, does not guarantee a design as the mass production set.

The characteristic of thermistor

| Parameter               | Symbol    | Condition                   | Min  | Typ. | Max  | Unit               |
|-------------------------|-----------|-----------------------------|------|------|------|--------------------|
| Resistance              | $R_{25}$  | $T_c = 25^{\circ}\text{C}$  | 97   | 100  | 103  | k $\Omega$         |
| Resistance              | $R_{100}$ | $T_c = 100^{\circ}\text{C}$ | 4.93 | 5.38 | 5.88 | k $\Omega$         |
| B-Constant (25 to 50°C) | B         |                             | 4165 | 4250 | 4335 | k                  |
| Temperature Range       |           |                             | -40  | -    | +125 | $^{\circ}\text{C}$ |

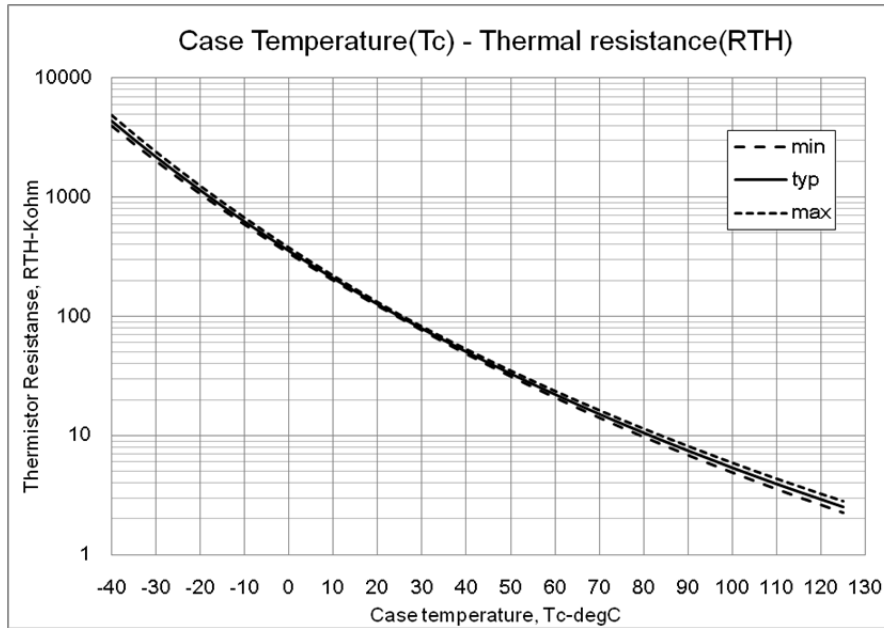


Fig. 10

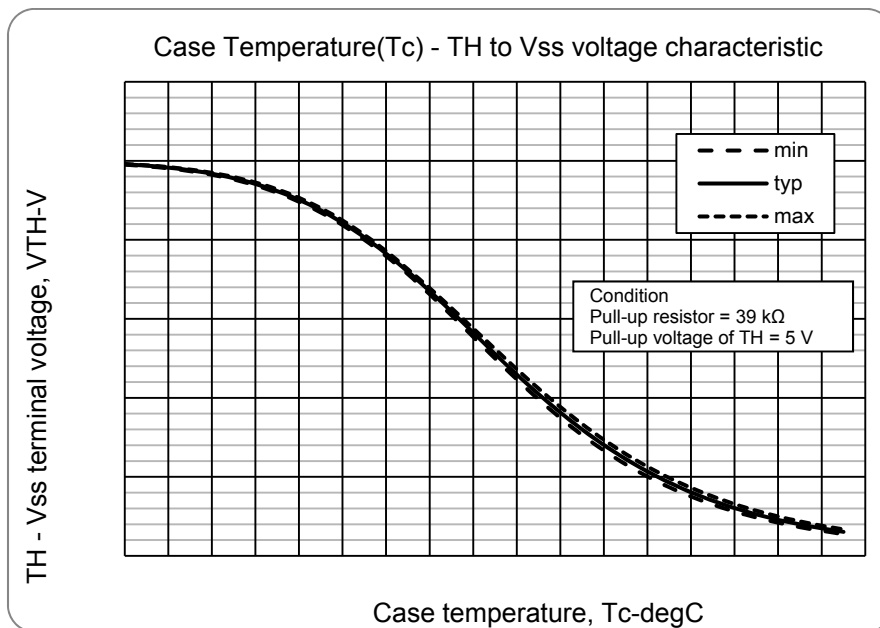


Fig. 11

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### The characteristic of PWM switching frequency

Maximum sinusoidal phase current as function of switching frequency ( $V_{BUS} = 400\text{ V}$ ,  $T_c = 100^\circ\text{C}$ )

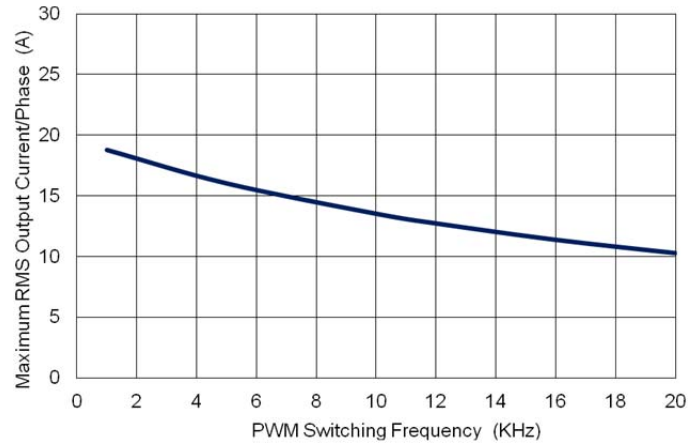


Fig.12

### Switching waveform

IGBT Turn-on. Typical turn-on waveform @ $T_c = 100^\circ\text{C}$ ,  $V_{BUS} = 400\text{ V}$

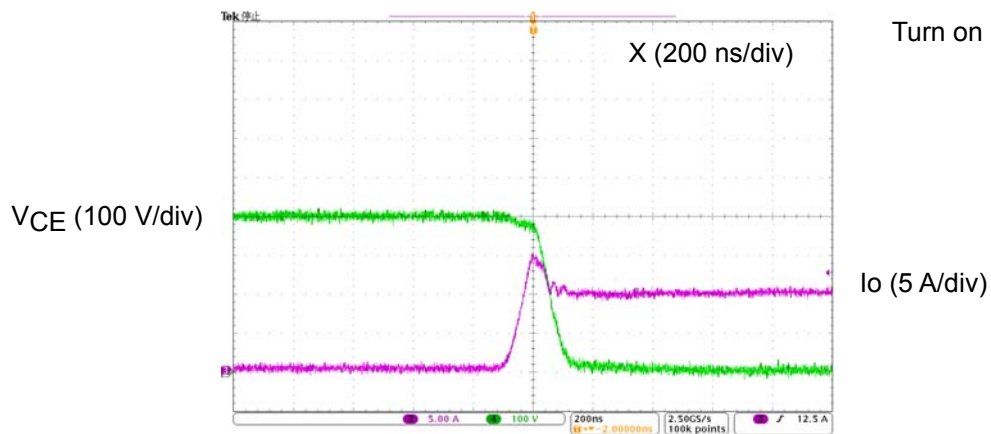


Fig. 13

IGBT Turn-off. Typical turn-off waveform @ $T_c = 100^\circ\text{C}$ ,  $V_{BUS} = 400\text{ V}$

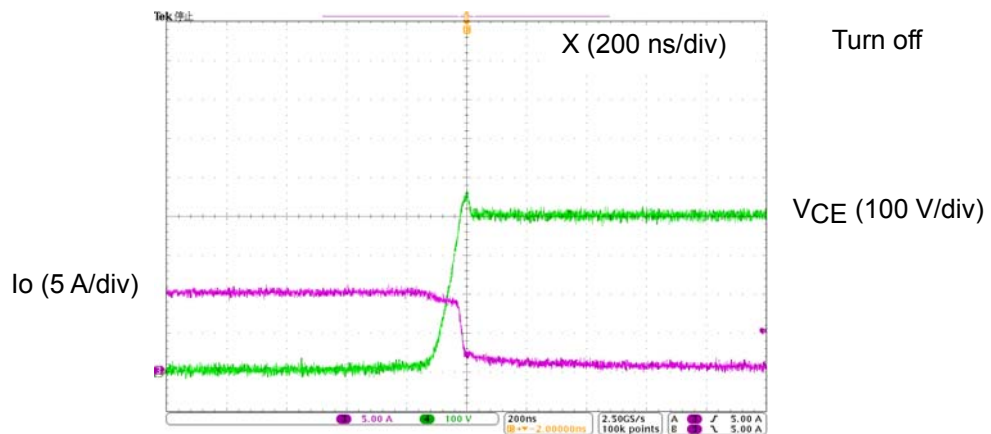


Fig. 14

## CB capacitor value calculation for bootstrap circuit

### Calculate condition

| Item                                                      | Symbol  | Value | Unit |
|-----------------------------------------------------------|---------|-------|------|
| Upper side power supply                                   | VBS     | 15    | V    |
| Total gate charge of output power IGBT at 15 V            | Qg      | 89    | nC   |
| Upper side power supply low voltage protection            | UVLO    | 12    | V    |
| Upper side power dissipation                              | IDmax   | 400   | μA   |
| ON time required for CB voltage to fall from 15 V to UVLO | Ton-max | -     | s    |

### Capacitance calculation formula

CB must not be discharged below to the upper limit of the UVLO - the maximum allowable on-time (Ton-max) of the upper side is calculated as follows:

$$VBS \times CB - Qg - IDmax \times Ton-max = UVLO \times CB$$

$$CB = (Qg + IDmax \times Ton-max) / (VBS - UVLO)$$

The relationship between Ton-max and CB becomes as follows. CB is recommended to be approximately 3 times the value calculated above. The recommended value of CB is in the range of 1 to 47 μF, however, the value needs to be verified prior to production.

### Tonmax-Cb characteristic

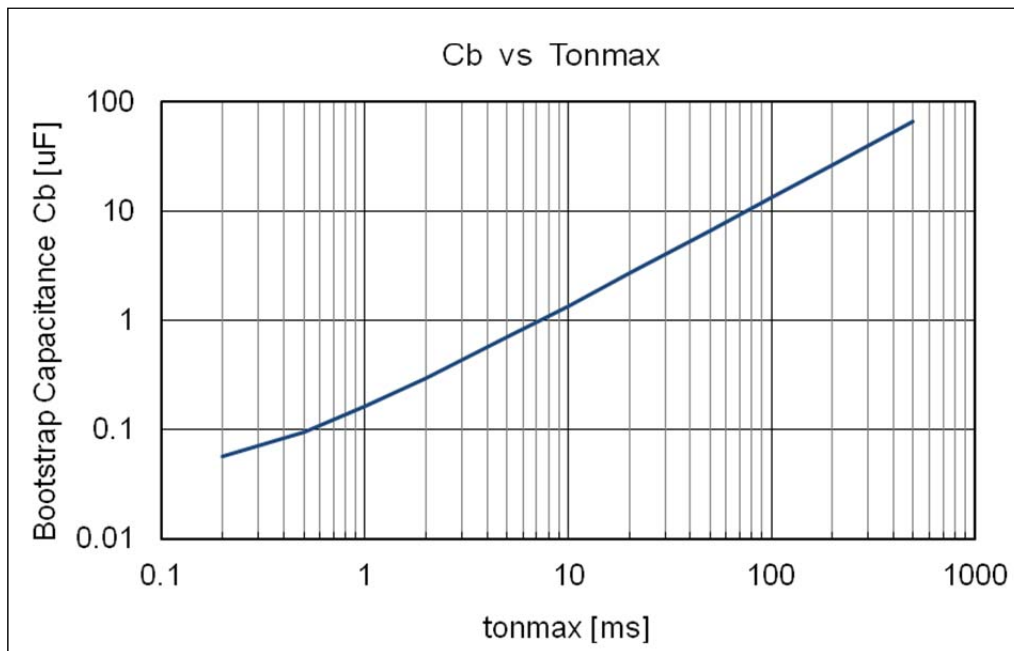


Fig. 15

# STK551U362A-E

## Package Dimensions

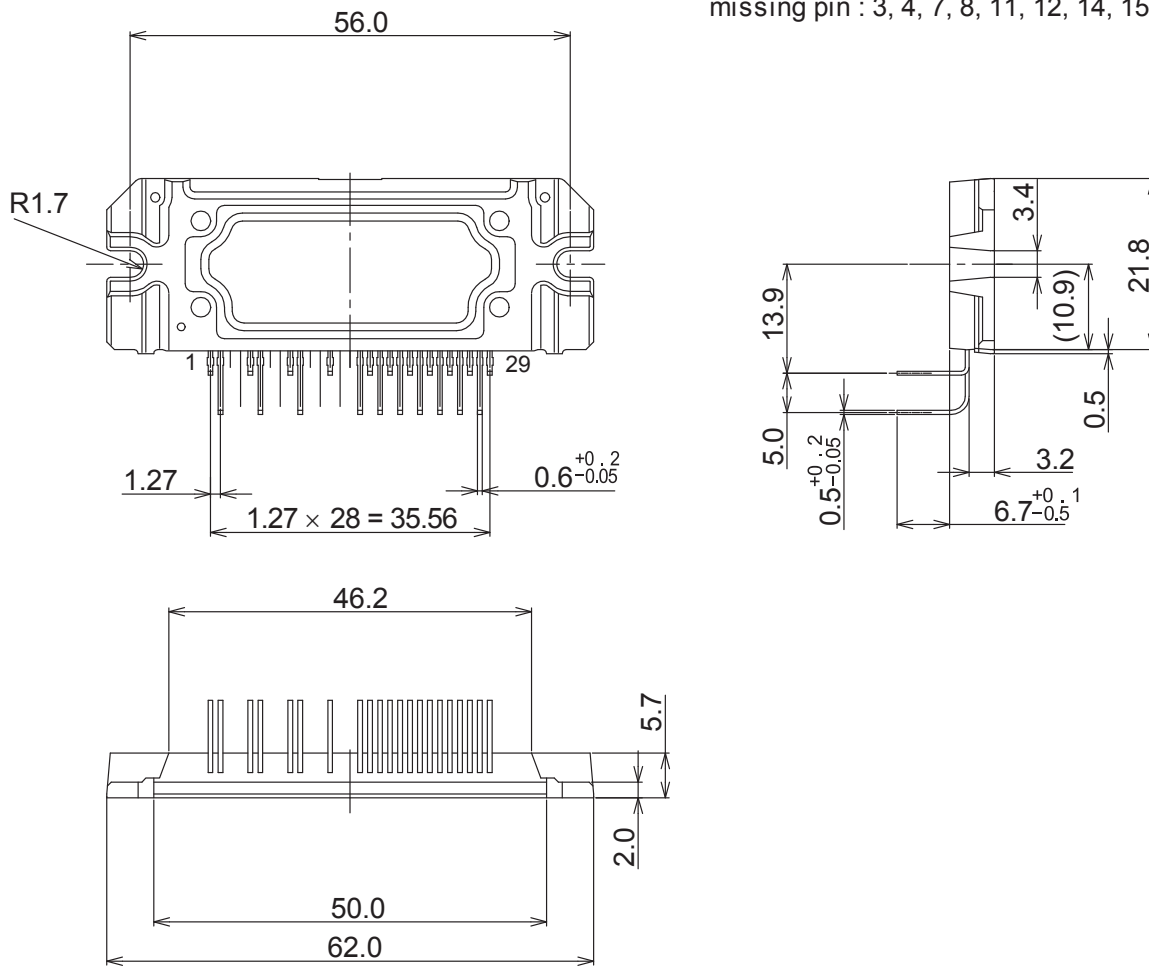
unit : mm

SIP29 56x21.8

CASE 127BW

ISSUE O

missing pin : 3, 4, 7, 8, 11, 12, 14, 15



## STK551U362A-E

### ORDERING INFORMATION

| Device        | Package                    | Shipping (Qty / Packing) |
|---------------|----------------------------|--------------------------|
| STK551U362A-E | SIP29 56x21.8<br>(Pb-Free) | 8 / Tube                 |

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