STK5Q4U340J-E

Advance Information

Intelligent Power Module (IPM) 600 V, 5 A

The STK5Q4U340J-E is a fully-integrated inverter power stage consisting of a high-voltage driver, six IGBT's and a thermistor, suitable for driving permanent magnet synchronous (PMSM) motors, brushless-DC (BLDC) motors and AC asynchronous motors. The IGBT's are configured in a 3-phase bridge with separate emitter connections for the lower legs for maximum flexibility in the choice of control algorithm.
The power stage has a full range of protection functions including cross-conduction protection, external shutdown and under-voltage lockout functions. An internal comparator and reference connected to the over-current protection circuit allows the designer to set the over-current protection level.

Features

- Three-phase 5 A / 600 V IGBT module with integrated drivers
- Typical values : $V_{CE}(sat)$ = 1.8 V, V_F = 1.8 V, E_{SW} = 270 μJ
- Compact 29.6 mm × 18.2 mm dual in-line package
- Cross-conduction protection
- Adjustable over-current protection level
- Integrated bootstrap diodes and resistors
- Enable pin
- Thermistor

Typical Applications

- Industrial Pumps
- Industrial Fans
- Industrial Automation
- Home Appliances

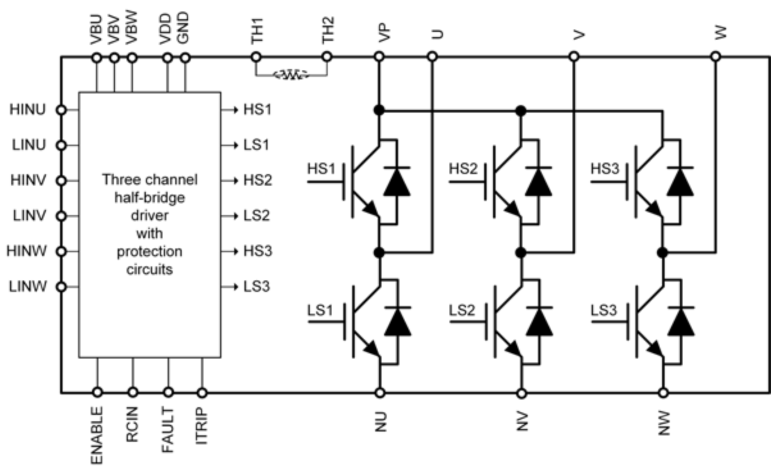

Figure 1. Functional Diagram

This document contains information on a new product. Specifications and information herein are subject to change without notice.

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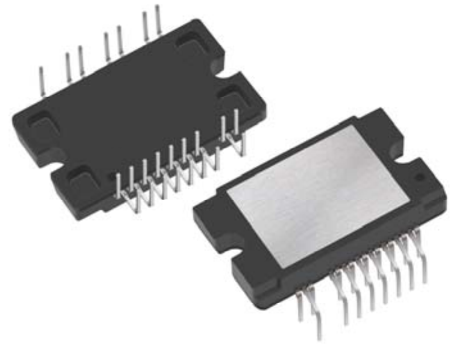
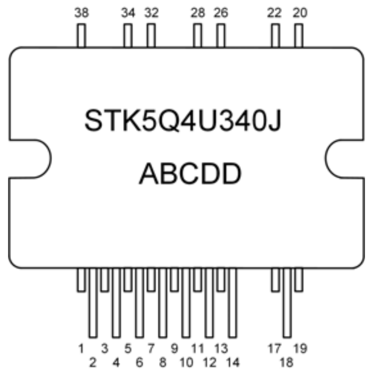
PACKAGE PICTURE



MODULE SPCM24 29.6x18.2 DIP S3

MARKING DIAGRAM



STK5Q4U340J = Specific Device Code
A = Year
B = Month
C = Production Site
DD = Factory Lot Code
Device marking is on package underside

ORDERING INFORMATION

Device	Package	Shipping (Qty / Packing)
STK5Q4U340J-E	MODULE SPCM24 29.6x18.2 DIP S3 (Pb-Free)	16 / Tube

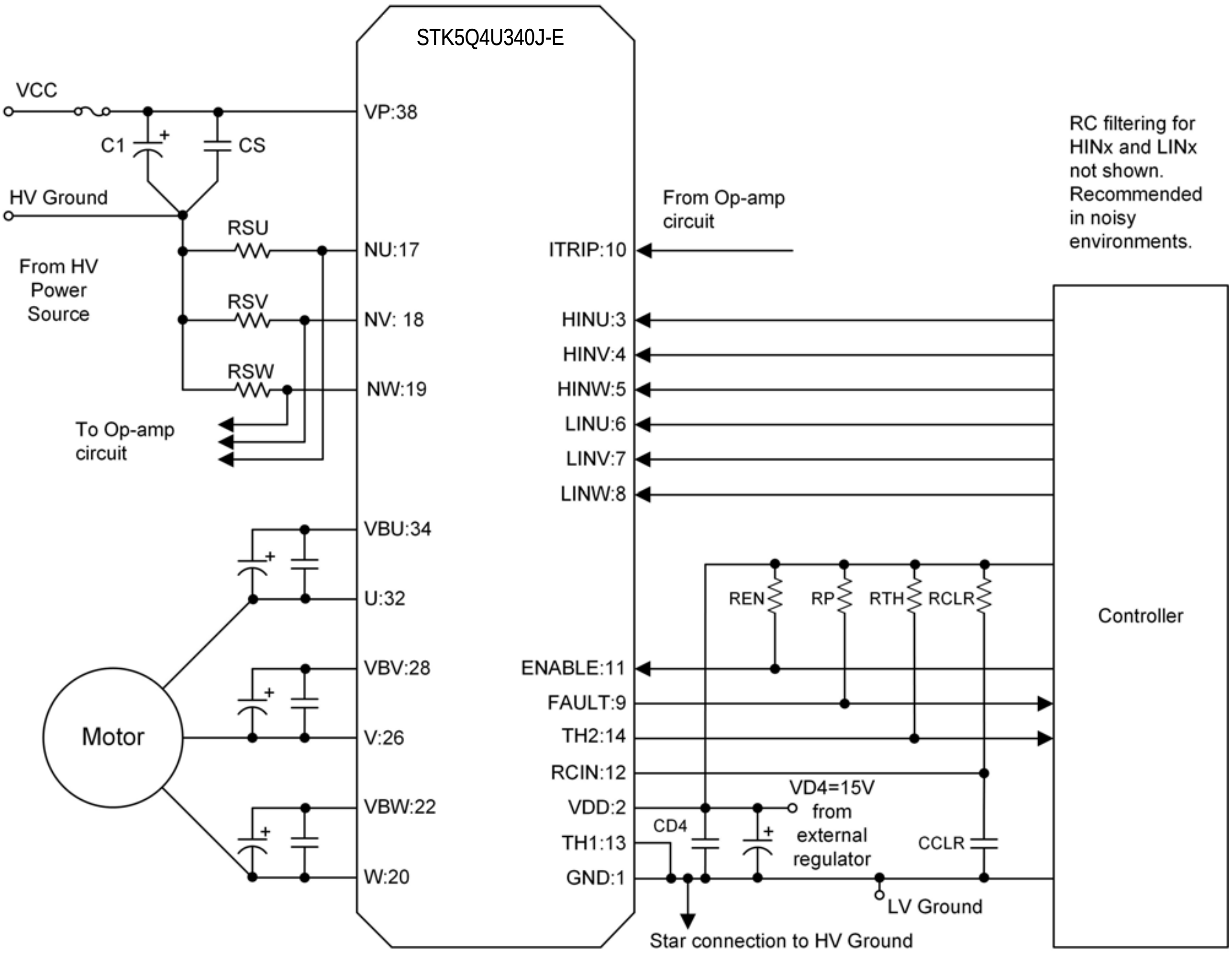


Figure 2. Application Schematic

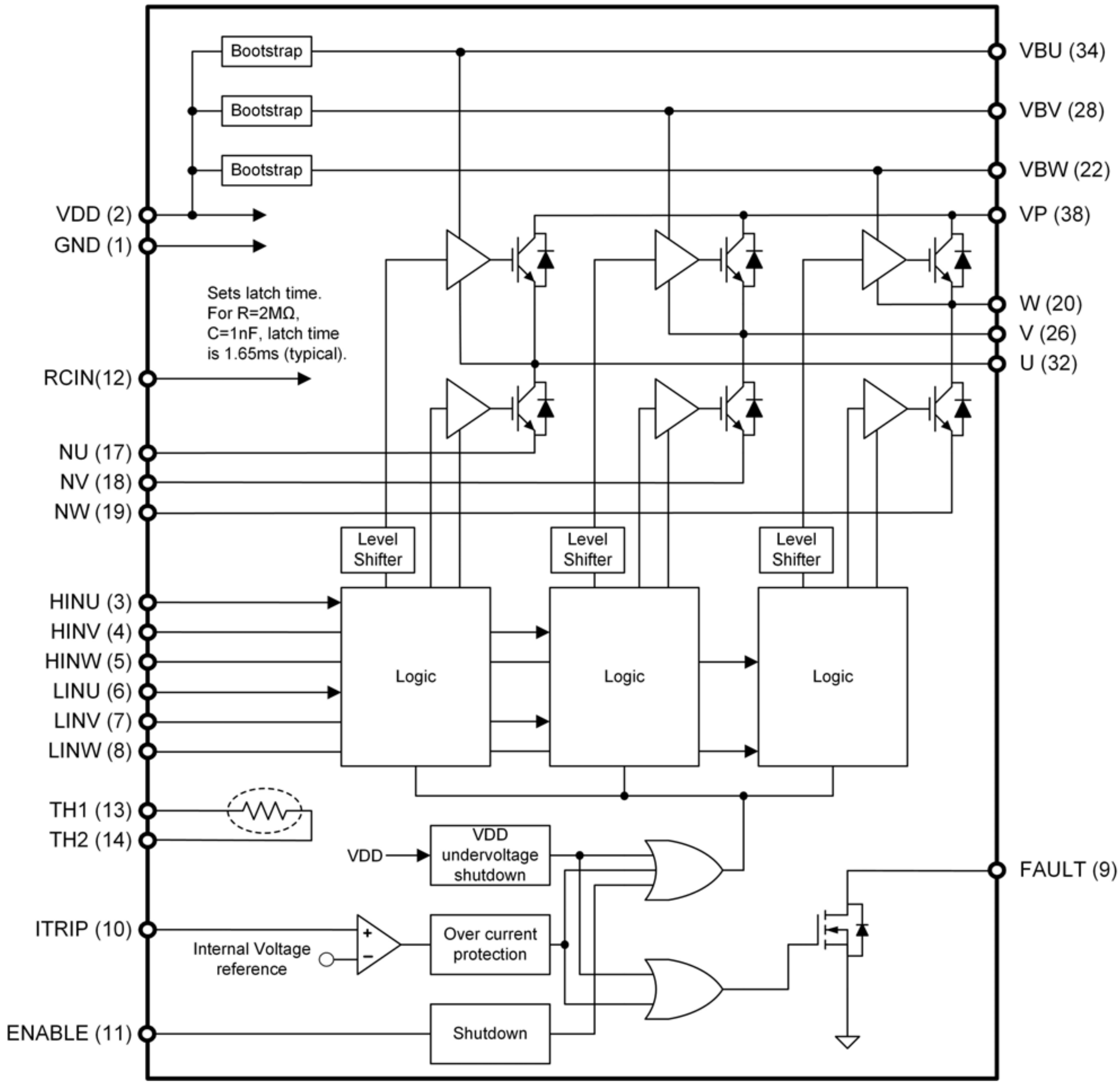


Figure 3. Simplified Block Diagram

PIN FUNCTION DESCRIPTION

Pin	Name	Description
1	GND	Negative Main Supply
2	VDD	+15 V Main Supply
3	HINU	Logic Input High Side Gate Driver - Phase U
4	HINV	Logic Input High Side Gate Driver - Phase V
5	HINW	Logic Input High Side Gate Driver - Phase W
6	LINU	Logic Input Low Side Gate Driver - Phase U
7	LINV	Logic Input Low Side Gate Driver - Phase V
8	LINW	Logic Input Low Side Gate Driver - Phase W
9	FAULT	Fault output
10	ITRIP	Current protection pin
11	ENABLE	Enable input
12	RCIN	R, C connection terminal for setting FAULT clear time
13	TH1	Thermistor output 1
14	TH2	Thermistor output 2
17	NU	Low Side Emitter Connection - Phase U
18	NV	Low Side Emitter Connection - Phase V
19	NW	Low Side Emitter Connection - Phase W
20	W	W phase output. Internally connected to W phase high side driver ground
22	VBW	High Side Floating Supply Voltage for W phase
26	V	V phase output. Internally connected to V phase high side driver ground
28	VBV	High Side Floating Supply voltage for V phase
32	U	U phase output. Internally connected to U phase high side driver ground
34	VBU	High Side Floating Supply voltage for U phase
38	VP	Positive Bus Input Voltage

Note : Pins 15, 16, 21, 23, 24, 25, 27, 29, 30, 31, 33, 35, 36, 37 are not present

ABSOLUTE MAXIMUM RATINGS (Notes 1, 2)

Rating	Symbol	Conditions	Value	Unit
Supply voltage	V_{CC}	VP to NU, NV, NW, surge < 500 V (Note 3)	450	V
Collector-emitter voltage	V_{CE} max	VP to U, V, W ; U to NU ; V to NV ; W to NW	600	V
Output current	Io	VP, U, V, W, NU, NV, NW terminal current	±5	A
		VP, U, V, W, NU, NV, NW terminal current, Tc = 100°C	±2.5	A
Output peak current	Iop	VP, U, V, W, NU, NV, NW terminal current, pulse width 1 ms	±10	A
Gate driver supply voltages	V_{DD},V_{BS}	VBU to U, VBV to V, VBW to W, V_{DD} to GND (Note 4)	−0.3 to +20.0	V
Input signal voltage	V_{IN}	HINU, HINV, HINW, LINU, LINV, LINW	−0.3 to V_{DD}	V
FAULT terminal voltage	VFAULT	FAULT terminal	−0.3 to V_{DD}	V
RCIN terminal voltage	VRCIN	RCIN terminal	−0.3 to V_{DD}	V
ITRIP terminal voltage	VITRIP	ITRIP terminal	−0.3 to +10.0	V
ENABLE terminal voltage	VENABLE	ENABLE terminal	−0.3 to V_{DD}	V
Maximum power dissipation	Pd	IGBT per 1 channel	(25)	W
Junction temperature	Tj	IGBT, Gate driver IC	150	°C
Storage temperature	Tstg		−40 to +125	°C
Operating case temperature	Tc	IPM case temperature	−20 to +100	°C
Package mounting torque		Case mounting screw	0.6	Nm
Isolation voltage	Vis	50 Hz sine wave AC 1 minute (Note 5)	2000	Vrms

1. Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.
2. Refer to ELECTRICAL CHARACTERISTICS, RECOMMENDED OPERATING RANGES and/or APPLICATION INFORMATION for Safe Operating parameters.
3. This surge voltage developed by the switching operation due to the wiring inductance between VP and NU,NV,NW terminals.
4. V_{BS} = VBU to U, VBV to V, VBW to W.
5. Test conditions : AC 2500 V, 1 s

RECOMMENDED OPERATING RANGES (Note 6)

Rating	Symbol		Min	Typ	Max	Unit
Supply voltage	V_{CC}	VP to NU, NV, NW	0	280	400	V
Gate driver supply voltage	V_{BS}	VBU to U, VBV to V, VBW to W	12.5	15	17.5	V
	V_{DD}	V_{DD} to GND (Note 4)	13.5	15	16.5	V
ON-state input voltage	V_{IN}(ON)	HINU, HINV, HINW, LINU, LINV, LINW	3.0		5.0	V
OFF-state input voltage	V_{IN}(OFF)		0		0.3	V
PWM frequency	fPWM		1		20	kHz
Dead time	DT	Turn-off to turn-on (external)	1			μs
Allowable input pulse width	PWIN	ON and OFF	1			μs
Package mounting torque		'M3' type screw	0.4		0.6	Nm

6. Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

ELECTRICAL CHARACTERISTICS at Tc = 25°C, V_{BS} = 15 V, V_{DD} = 15 V (Note 7)

Parameter	Test Conditions	Symbol	Min	Typ	Max	Unit
Power output section						
Collector-emitter leakage current	V_{CE} = 600 V	I_{CE}	-	-	100	μA
Collector to emitter saturation voltage	Ic = 5 A, Tj = 25°C	V_{CE}(sat)	-	(1.8)	(2.6)	V
	Ic = 2.5 A, Tj = 100°C		-	(1.5)	-	V
Diode forward voltage	IF = 5 A, Tj = 25°C	V_F	-	(1.8)	(2.6)	V
	IF = 2.5 A, Tj = 100°C		-	(1.5)	-	V
Junction to case thermal resistance	IGBT	θj-c(T)	-	-	5	°C/W
Switching time	Ic = 5 A, V_{CC} = 300 V, Tj = 25°C	t_{ON}	-	(0.5)	(1.3)	μs
		t_{OFF}	-	(0.6)	(1.5)	μs
Turn-on switching loss	Ic = 5 A, V_{CC} = 300 V, Tj = 25°C	E_{ON}	-	(250)	-	μJ
Turn-off switching loss		E_{OFF}	-	(20)	-	μJ
Total switching loss		E_{TOT}	-	(270)	-	μJ
Turn-on switching loss	Ic = 5 A, V_{CC} = 300 V, Tj = 25°C	E_{ON}	-	(300)	-	μJ
Turn-off switching loss		E_{OFF}	-	(30)	-	μJ
Total switching loss		E_{TOT}	-	(330)	-	μJ
Diode reverse recovery energy	Ic = 5 A, V_{CC} = 300 V, Tj = 25°C (di/dt set by internal driver)	E_{REC}	-	(100)	-	μJ
Diode reverse recovery time		trr	-	(200)	-	ns
Reverse bias safe operating area	Ic = 10 A, V_{CE} = 450 V	RBSOA	Full Square	-		
Short circuit safe operating area	V_{CE} = 400 V	SCSOA	4	-	-	μs
Allowable offset voltage slew rate	U to NU, V to NV, W to NW	dv/dt	−50	-	50	V/ns
Driver Section						
Gate driver consumption current	V_{BS} = 15 V (Note 4), per driver	ID	-	0.07	0.4	mA
	V_{DD} = 15 V, total	ID	-	0.95	3	mA
High level Input voltage	HINU, HINV, HINW, LINU, LINV, LINW to GND	VIN H	2.5	-	-	V
Low level Input voltage		VIN L	-	-	0.8	V
Logic 1 input current	V_{IN} = +3.3 V	I_{IN+}	-	660	900	μA
Logic 0 input current	V_{IN} = 0 V	I_{IN-}	-	-	3	μA
Bootstrap ON Resistance	IB = 1 mA	RB	-	110	-	Ω
FAULT terminal sink current	FAULT : ON / VFAULT = 0.1 V	IoSD	-	2	-	mA
FAULT clearance delay time	RCLR = 2 MΩ, CCLR = 1 nF	FLTCLR	1.1	1.65	2.2	ms
ENABLE ON/OFF voltage	VEN ON-state voltage	VEN(ON)	2.5	-	-	V
	VEN OFF-state voltage	VEN(OFF)	-	-	0.8	V
ITRIP threshold voltage	ITRIP to GND	VITRIP	0.44	0.49	0.54	V
ITRIP to shutdown propagation delay		t_{ITRIP}	-	1.1	-	μs
ITRIP blanking time		$t_{ITRIPBL}$	250	350	-	ns
V_{DD} and V_{BS} supply undervoltage positive going input threshold		V_{DDUV+} V_{BSUV+}	10.2	11.1	11.8	V
V_{DD} and V_{BS} supply undervoltage negative going input threshold		V_{DDUV-} V_{BSUV-}	10.0	10.9	11.6	V
V_{DD} and V_{BS} supply undervoltage $I_{lockout}$ hysteresis		V_{DDUVH} V_{BSUVH}	-	0.2	-	V

7. Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

TYPICAL CHARACTERISTICS

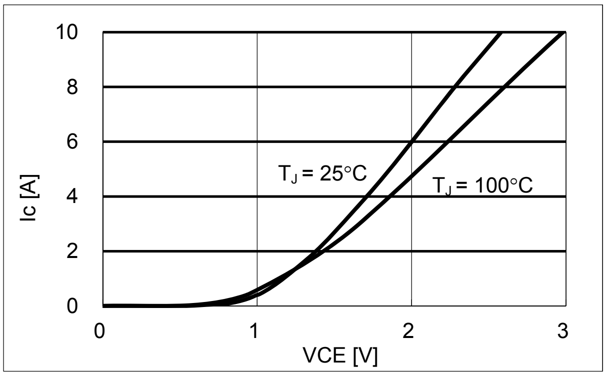


Figure 4. V_{CE} versus ID for different temperatures (V_{DD} = 15 V)

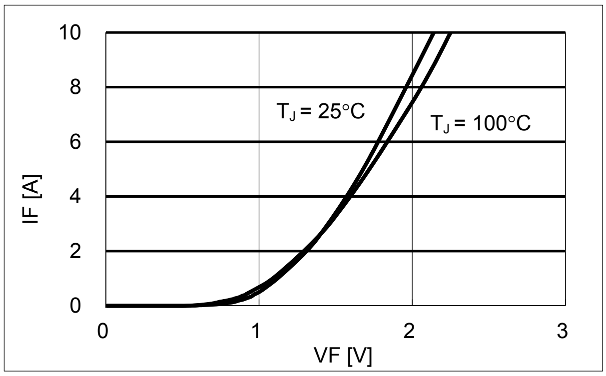


Figure 5. V_F versus ID for different temperatures

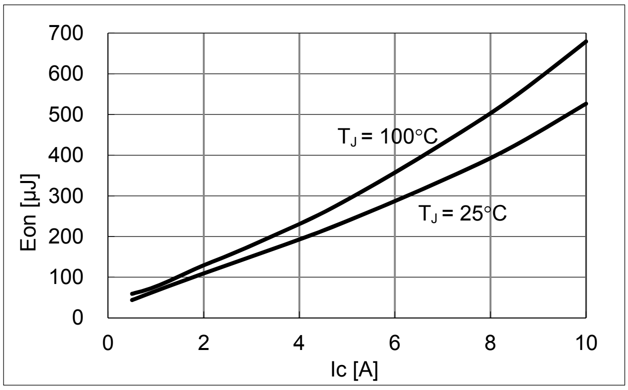


Figure 6. EON versus ID for different temperatures

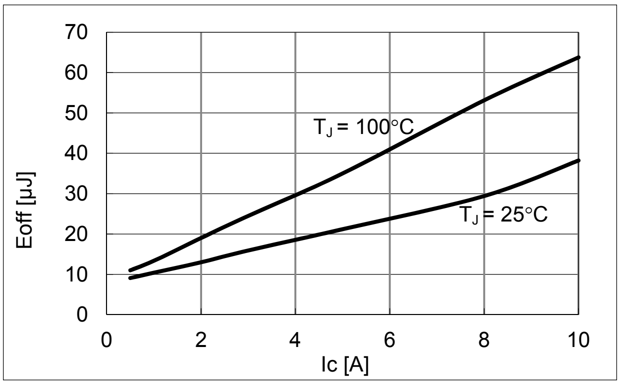


Figure 7. EOFF versus ID for different temperatures

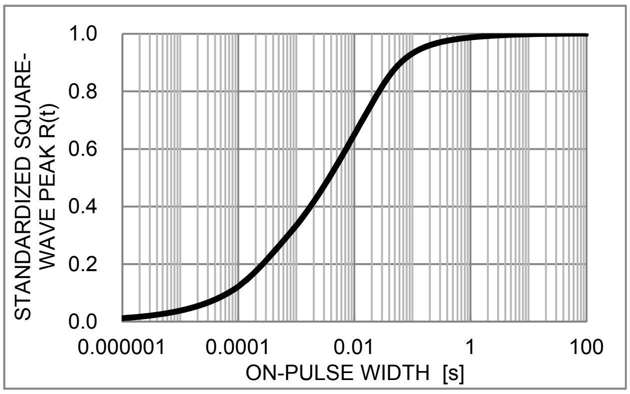


Figure 8. Thermal impedance plot

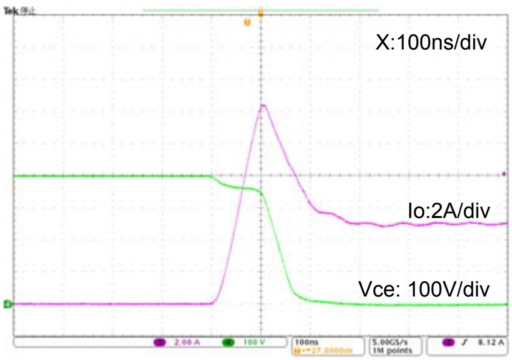


Figure 9. Turn-on waveform Tj = 100°C, V_{CC} = 400 V

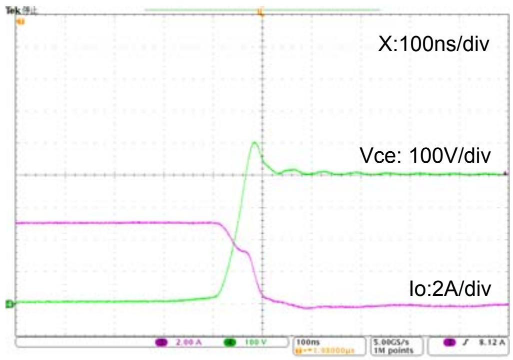


Figure 10. Turn-off waveform Tj = 100°C, V_{CC} = 400 V

APPLICATIONS INFORMATION

Input / Output Timing Chart

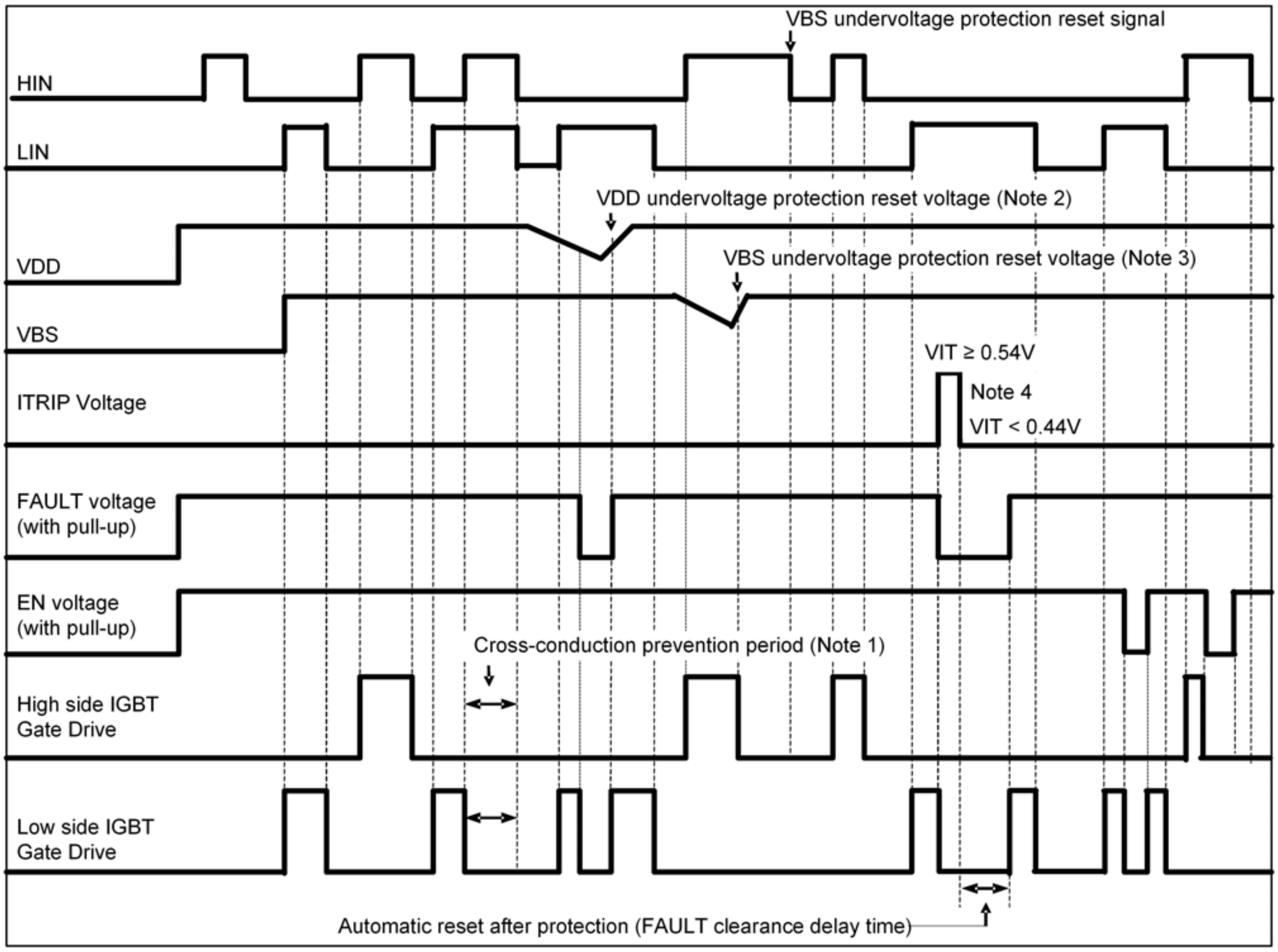


Figure 11. Input/Output Timing Chart

Notes

1. This section of the timing diagram shows the effect of cross-conduction prevention.
2. This section of the timing diagram shows that when the voltage on V_{DD} decreases sufficiently all gate output signals will go low, switching off all six IGBTs. When the voltage on V_{DD} rises sufficiently, normal operation will resume.
3. This section shows that when the bootstrap voltage V_{BS} drops, the corresponding high side output (U or V or W) is switched off. When V_{BS} rises sufficiently, normal operation will resume.
4. This section shows that when the voltage on ITRIP exceeds the threshold, all IGBT's are turned off. Normal operation resumes later after the over-current condition is removed.
5. After V_{DD} has risen above the threshold to enable normal operation, the driver waits to receive an input signal on the LIN input before enabling the driver for the HIN signal.

Input / Output Logic Table

INPUT				OUTPUT			
HIN	LIN	Itrip	Enable	High side IGBT	Low side IGBT	U, V, W	FAULT
H	L	L	H	ON (Note 5)	OFF	VP	OFF
L	H	L	H	OFF	ON	NU, NV, NW	OFF
L	L	L	H	OFF	OFF	High Impedance	OFF
H	H	L	H	OFF	OFF	High Impedance	OFF
X	X	H	H	OFF	OFF	High Impedance	ON
X	X	X	L	OFF	OFF	High Impedance	OFF

Thermistor characteristics

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Resistance	R_{25}	Tc = 25°C	99	100	101	kΩ
	R_{100}	Tc = 100°C	5.18	5.38	5.60	kΩ
B-Constant (25 to 50°C)	B		4208	4250	4293	K
Temperature Range			–40		+125	°C

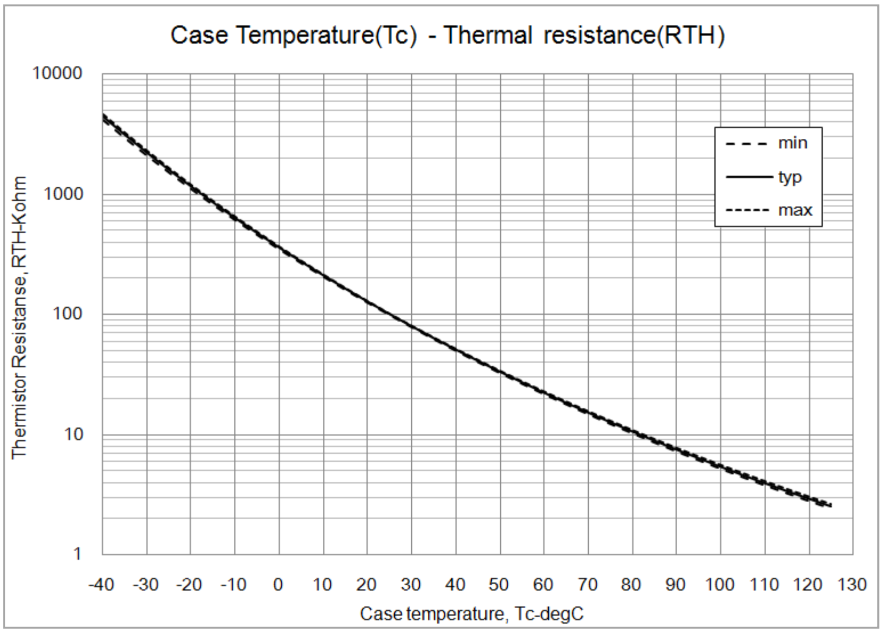


Figure 12. Thermistor Resistance versus Case Temperature

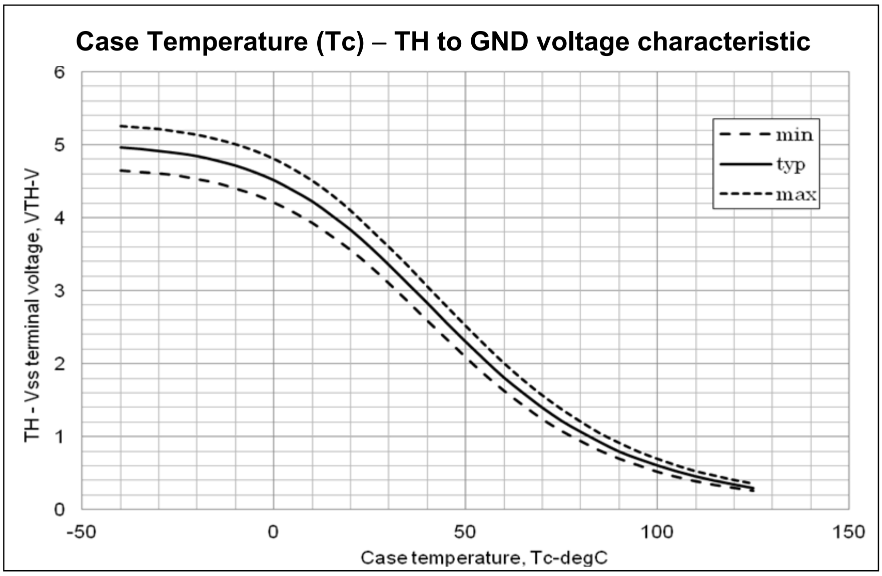


Figure 13. Thermistor Voltage versus Case Temperature
Conditions : RTH = 39 kΩ, pull-up voltage 5.0 V (see Figure 2)

Fault output

The FAULT output is an open drain output requiring a pull-up resistor. If the pull-up voltage is 5 V, use a pull-up resistor with a value of 6.8 kΩ or higher. If the pull-up voltage is 15 V, use a pull-up resistor with a value of 20 kΩ or higher. The FAULT output is triggered if there is a V_{DD} undervoltage or an overcurrent condition.

Undervoltage lockout protection

If V_{DD} goes below the V_{DD} supply undervoltage lockout falling threshold, the FAULT output is switched on. The FAULT output stays on until V_{DD} rises above the V_{DD} supply undervoltage lockout rising threshold. After V_{DD} has risen above the threshold to enable normal operation, the driver waits to receive an input signal on the LIN input before enabling the driver for the HIN signal.

Overcurrent protection

An over-current condition is detected if the voltage on the ITRIP pin is larger than the reference voltage. There is a blanking time of typically 350 ns to improve noise immunity. After a shutdown propagation delay of typically 1.1 μs, the FAULT output is switched on. The FAULT output is held on for a time determined by the resistor and capacitor connected to the RCIN pin. If RCLR = 2 MΩ and CCLR = 1 nF, the FAULT output is switched on for 1.65 ms (typical).

The over-current protection threshold should be set to be equal or lower to 2 times the module rated current (IO).

An additional fuse is recommended to protect against system level or abnormal over-current fault conditions.

Capacitors on High Voltage and V_{DD} supplies

Both the high voltage and V_{DD} supplies require an electrolytic capacitor and an additional high frequency capacitor.

Enable pin

The ENABLE terminal pin is used to enable or shut down the built-in driver. If the voltage on the ENABLE pin rises above the ENABLE ON-state voltage, the output drivers are enabled. If the voltage on the ENABLE pin falls below the ENABLE OFF-state voltage, the drivers are disabled.

Minimum input pulse width

When input pulse width is less than 1 μs, an output may not react to the pulse. (Both ON signal and OFF signal)

Calculation of bootstrap capacitor value

The bootstrap capacitor value CB is calculated using the following approach. The following parameters influence the choice of bootstrap capacitor:

- V_{BS} : Bootstrap power supply.
  15 V is recommended.
- QG : Total gate charge of IGBT at V_{BS} = 15 V.
  34 nC for the STK5Q4U340J
- UVLO : Falling threshold for UVLO.
  Specified as 12 V.
- ID_{MAX} : High side drive consumption current.
  Specified as 0.4 mA
- t_{ONMAX} : Maximum ON pulse width of high side IGBT.

Capacitance calculation formula:

$CB = (QG + ID_{MAX} * t_{ONMAX})/(VBS - UVLO)$

CB is recommended to be approximately 3 times the value calculated above. The recommended value of CB is in the range of 1 to 47 μF, however, the value needs to be verified prior to production. When not using the bootstrap circuit, each high side driver power supply requires an external independent power supply.

The internal bootstrap circuit uses a MOSFET. The turn on time of this MOSFET is synchronized with the turn on of the low side IGBT. The bootstrap capacitor is charged by turning on the low side IGBT.

If the low side IGBT is held on for a long period of time (more than one second for example), the bootstrap voltage on the high side MOSFET will slowly discharge.

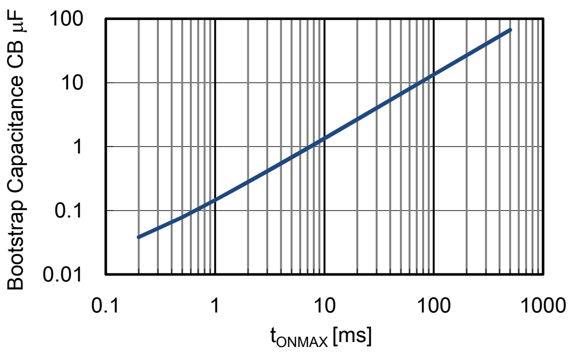


Figure 14. Bootstrap capacitance versus t_{ONMAX}

Mounting Instructions

Item	Recommended Condition
Pitch	26.0 ±0.1 mm (Please refer to Package Outline Diagram)
Screw	Diameter : M3 Screw head types : pan head, truss head, binding head
Washer	Plane washer dimensions (Figure 15) D = 7 mm, d = 3.2 mm and t = 0.5 mm JIS B 1256
Heat sink	Material : Aluminum or Copper Warpage (the surface that contacts IPM) : −50 to 50 μm Screw holes must be countersunk. No contamination on the heat sink surface that contacts IPM.
Torque	Temporary tightening : 50 to 60% of final tightening on first screw Temporary tightening : 50 to 60% of final tightening on second screw Final tightening : 0.4 to 0.6 Nm on first screw Final tightening : 0.4 to 0.6 Nm on second screw
Grease	Silicone grease. Thickness : 50 to 100 μm Uniformly apply silicone grease to whole back. Thermal foils are only recommended after careful evaluation. Thickness, stiffness and compressibility parameters have a strong influence on performance.

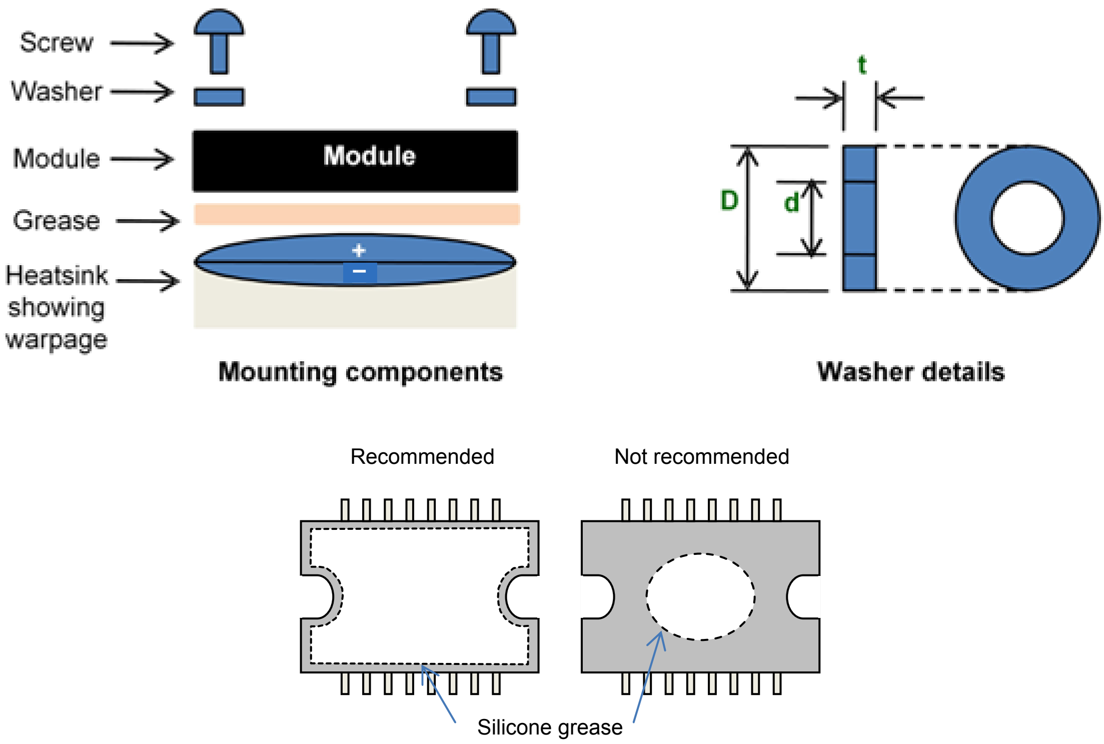


Figure 15. Module Mounting details: components; washer drawing; need for even spreading of thermal grease

TEST CIRCUITS

■ I_{CE}

	U+	V+	W+	U-	V-	W-
M	38	38	38	32	26	20
N	32	26	20	17	18	19

U+,V+,W+ : High side phase
U-,V-,W- : Low side phase

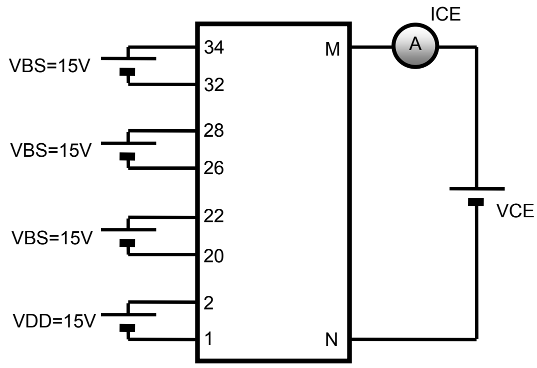


Figure 16. Test Circuit for I_{CE}

■ V_{CE}(sat) (Test by pulse)

	U+	V+	W+	U-	V-	W-
M	38	38	38	32	26	20
N	32	26	20	17	18	19
m	3	4	5	6	7	8

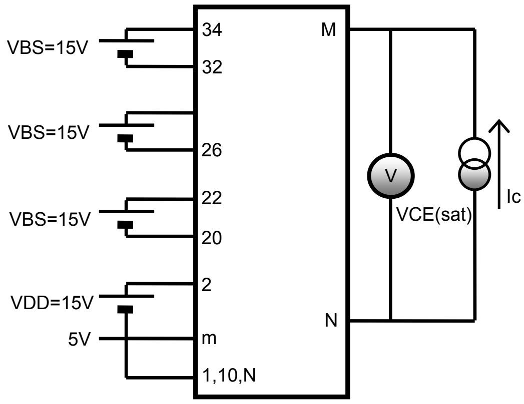


Figure 17. Test circuit for V_{CE}(sat)

■ VF (Test by pulse)

	U+	V+	W+	U-	V-	W-
M	38	38	38	32	26	20
N	32	26	20	17	18	19

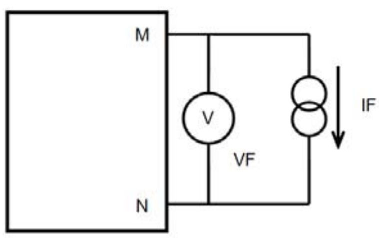


Figure 18. Test circuit for VF

■ RB (Test by pulse)

	U+	V+	W+
M	2	2	2
N	34	28	22

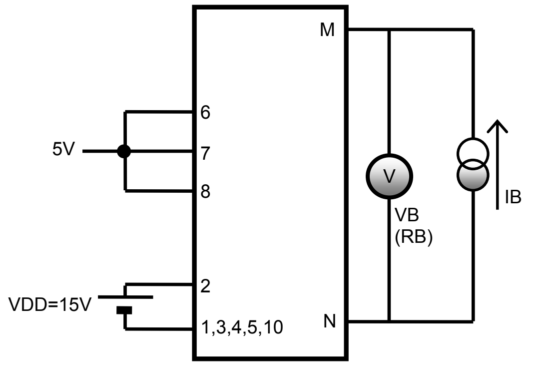


Figure 19. Test circuit for RB

■ ID

	VBS U+	VBS V+	VBS W+	V_{DD}
M	34	28	22	2
N	32	26	20	1

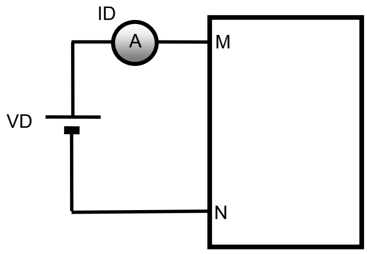
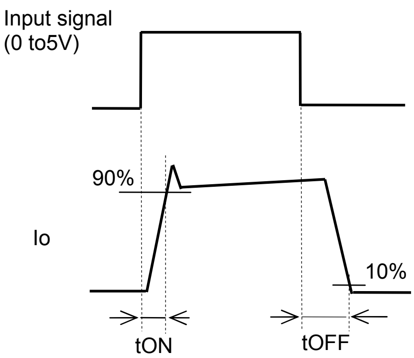


Figure 20. Test circuit for ID

■ Switching time (The circuit is a representative example of the low side U phase.)



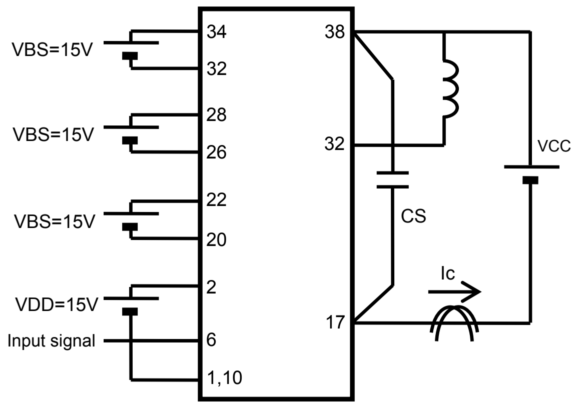
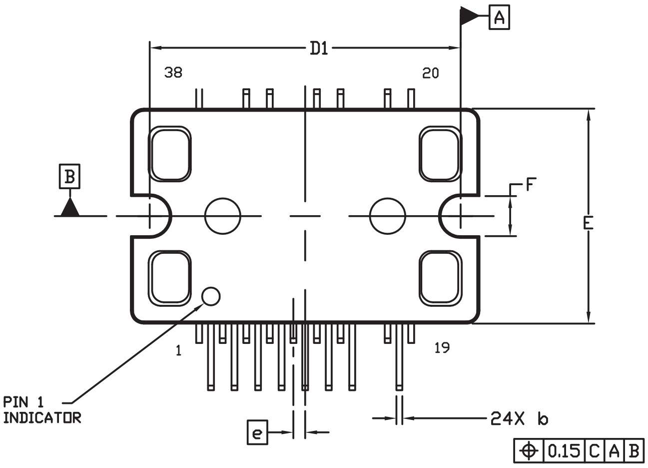


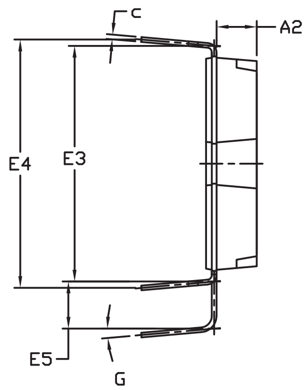
Figure 21. Switching time test circuit

PACKAGE DIMENSIONS

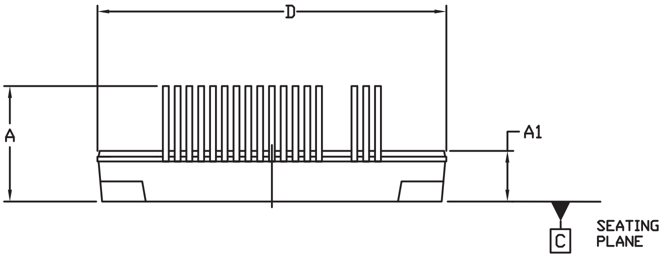
unit : mm



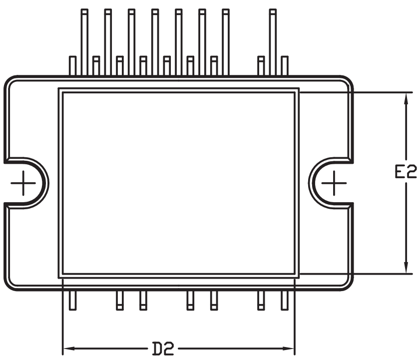
TOP VIEW



END VIEW



SIDE VIEW



BOTTOM VIEW

NOTES:

1. DIMENSIONING AND TOLERANCING PER. ASME Y14.5M, 2009.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSION b APPLIES TO THE PLATED LEAD AND IS MEASURED BETWEEN 0.10 AND 0.25 FROM THE LEAD TIP.
4. PACKAGE IS MISSING PINS: 15, 16, 21, 23, 24, 25, 27, 29, 30, 31, 33, 35, 36, AND 37.

	MILLIMETERS	
DIM	MIN.	MAX.
A	9.30	10.30
A1	3.80	4.80
A2	2.90	3.90
b	0.45	0.70
c	0.35	0.60
D	29.10	30.10
D1	26.30	26.50
D2	19.20	20.20
E	17.70	18.70
E2	14.90	15.90
E3	19.50	20.50
E4	21.10 REF	
E5	3.50	4.50
e	1.00 BSC	
F	2.90	3.90
G	4°	6°