DATA SHEET

by

SYNTEK®

==========STK6011==========

8051 Embedded Microcontroller

Version 1.0

DESIGN CENTER

6F, YU FENG BLDG. 317 SUNG-CHANG RD., TAIPEI, TAIWAN, R.O.C.

TEL: 886-2-25056383

FAX: 886-2-25064323

HEADQUARTER

3F, NO.24-2, INDUSTRY E.RD., IV, SCIENCE-BASED INDUSTRIAL PARK, HSINCHU, TAIWAN, R.O.C.

TEL: 886-3-5773181

FAX: 886-3-5778010

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STK6011 Data Sheet

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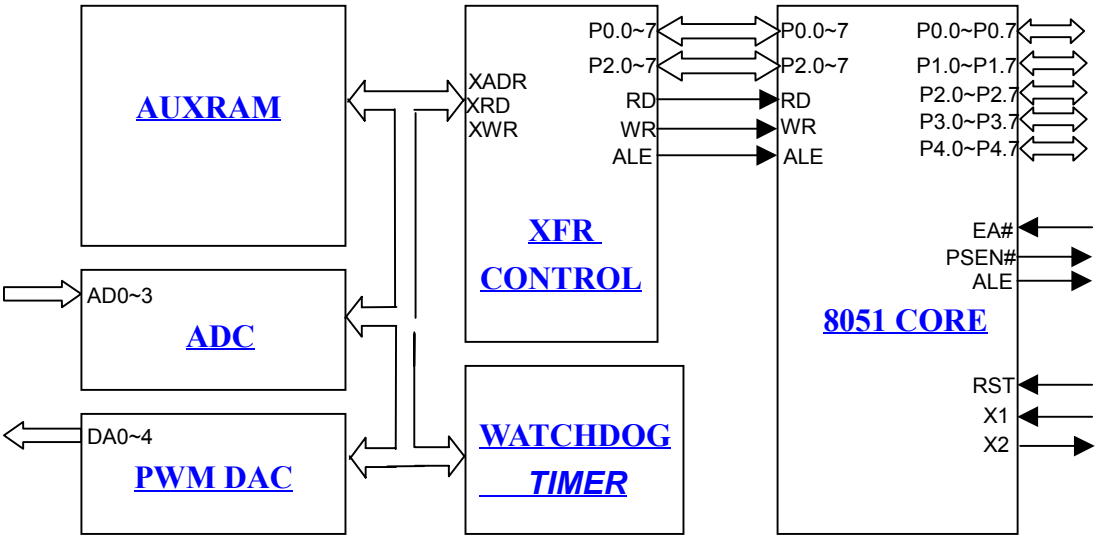
1. GENERAL DESCRIPTION

The STK6011 is an 8-bit micro-controller, which is compatible with the industry standard 8051 CPU. It consists of an 8051 CPU core, a 64k-byte internal program Flash ROM support to ISP function, a 1024-byte SRAM, four 8-bit I/O ports, an extra 4-bit I/O port, two 16-bit timer/counter, an UART serial port, five interrupt source, a watchdog timer, 5 built PWM DACs, and a 4-channel A/D converter.

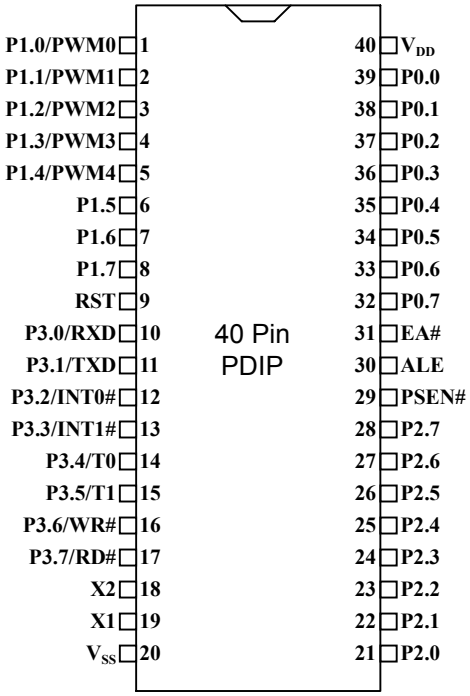
2. FEATURES

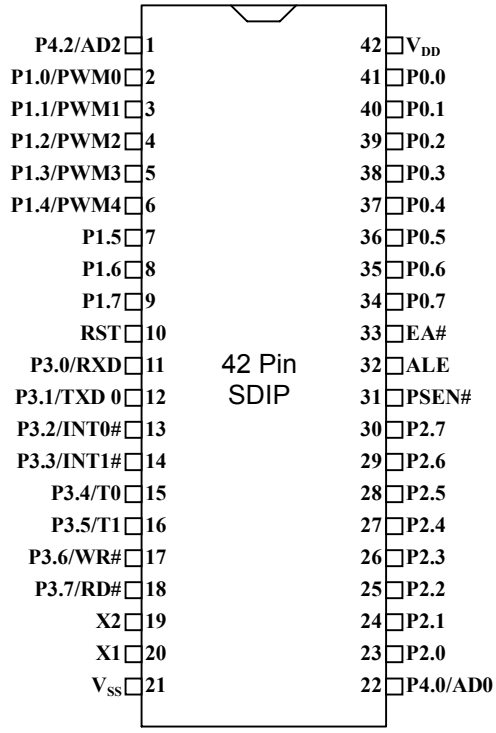
- Industry 8051 core
- 36 bi-directional I/O pins (max.)
- 5 channels of PWM DAC (max.)
- 4 channels of 6-bit ADC (max.)
- 64K bytes of program Flash ROM support to In-System Programming (ISP)
- 1024 bytes of SRAM
- Watchdog timer featuring programmable interval
- Built-in lower power reset circuit
- Power-down wakeup by interrupt (INT0# or INT1#)
- Flash ROM program code protection
- 5V/3.3V power supply with bonding option
- Package designed with 40-pin DIP, 42-pin SDIP, 44-pin PLCC, 44-pin QFP, or 48-pin LQFP

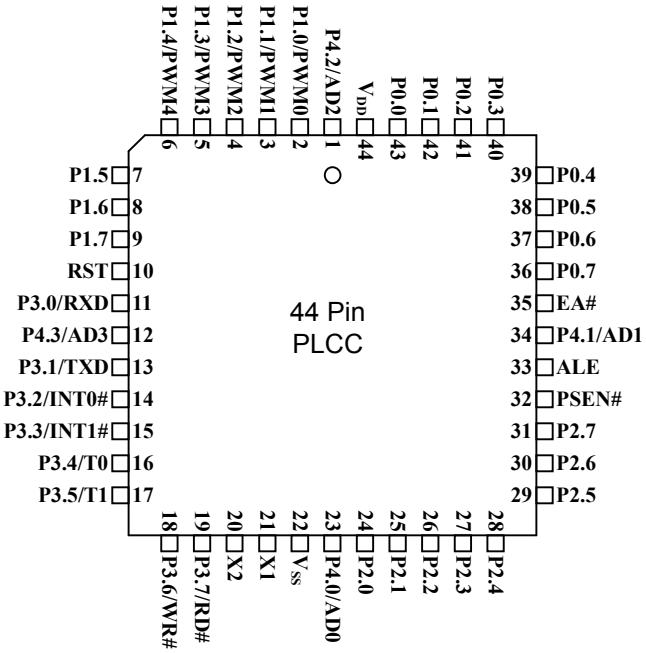
3. BLOCK DIAGRAM

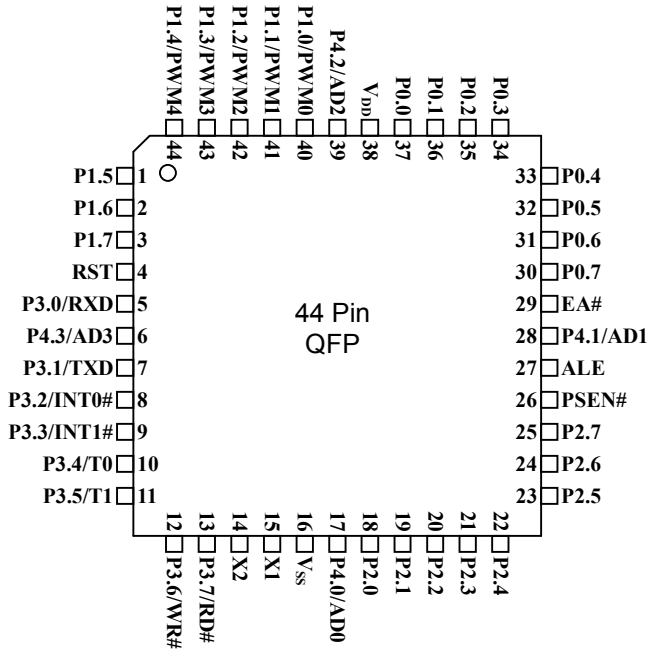


4. PIN CONNECTION








P1.4/PWM4 44
P1.3/PWM3 43
P1.2/PWM2 42
P1.1/PWM1 41
P1.0/PWM0 40
P4.2/AD2 39
VDD 38
P0.0 37
P0.1 36
P0.2 35
P0.3 34
P1.5 1
P1.6 2
P1.7 3
RST 4
P3.0/RXD 5
P4.3/AD3 6
P3.1/TXD 7
P3.2/INT0# 8
P3.3/INT1# 9
P3.4/T0 10
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33 P0.4
32 P0.5
31 P0.6
30 P0.7
29 EA#
28 P4.1/AD1
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24 P2.6
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12 P3.6/WR#
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14 X2
15 X1
16 VSS
17 P4.0/AD0
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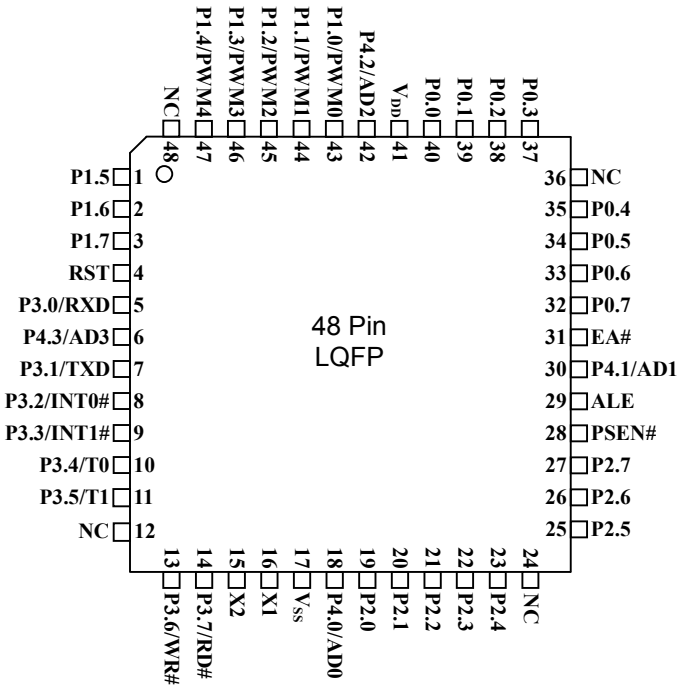
19 P2.1
20 P2.2
21 P2.3
22 P2.4


NC 48
P1.4/PWM4 47
P1.3/PWM3 46
P1.2/PWM2 45
P1.1/PWM1 44
P1.0/PWM0 43
P4.2/AD2 42
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P3.1/TXD 7
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P3.3/INT1# 9
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33 P0.6
32 P0.7
31 EA#
30 P4.1/AD1
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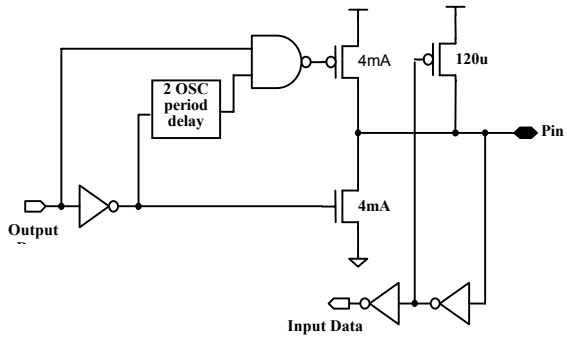
28 PSEN#
27 P2.7
26 P2.6
25 P2.5
48 Pin
LQFP
13 P3.6/WR#
14 P3.7/RD#
15 X2
16 X1
17 VSS
18 P4.0/AD0
19 P2.0
20 P2.1
21 P2.2
22 P2.3
23 P2.4
24 NC

5. PIN CONFIGURATION

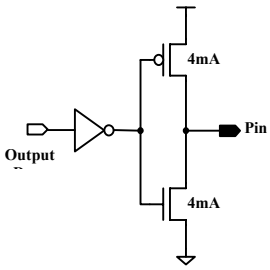
"Open drain pin" means the pin may sink at least 4mA current but drive only 10~20uA to V_{DD}. It may be used as input or output function and needs an external pull-up resistor.

"CMOS output" means the pin may sink at least 4mA and drive. It is not preferred to use such a pin as input function.

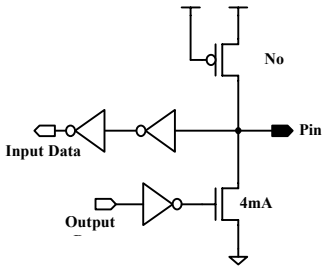
"8051 standard pin" is a pseudo-open drain pin. It may sink at least 4mA current when output stays at a low level, and drives at least 4mA current for 2 X'tal period when output changes from a low level to a high level, and then drives at 120μA for a high level. It can be used as input or output function and needs an external pull-up resistor when driving a device with heavy load.



8051 Standard Pin



CMOS Output Pin



Open Drain Pin

6. POWER CONFIGURATION

The STK6011 works in a system with a 5V or 3.3V power supply by bonding option.

In a 5V-power option, the V_{DD} pin is connected to a 5V power supply, all output pins changes from 0 to 5V, and input pins can accept a voltage ranging from 0 to 5V. The voltage range of ADC conversion is 5V. However, the X1 and X2 pins operate below 3.3V.

In a 3.3V power option, V_{DD} pin is connected to 3.3V power, all output pins change from 0 to 3.3V, and all input pins only allow input ranging from 0 to 3.3V. The voltage range of ADC conversion is 3.3V.

7. PINS DESCRIPTION

Name	I/O Type	Description
P0.0	I/O	General purpose I/O (open drain)
P0.1	I/O	General purpose I/O (open drain)
P0.2	I/O	General purpose I/O (open drain)
P0.3	I/O	General purpose I/O (open drain)
P0.4	I/O	General purpose I/O (open drain)
P0.5	I/O	General purpose I/O (open drain)
P0.6	I/O	General purpose I/O (open drain)
P0.7	I/O	General purpose I/O (open drain)
P1.0/PWM0	I/O	General purpose I/O (8051 standard) / PWM DAC output (CMOS)
P1.1/PWM1	I/O	General purpose I/O (8051 standard) / PWM DAC output (CMOS)
P1.2/PWM2	I/O	General purpose I/O (8051 standard) / PWM DAC output (CMOS)
P1.3/PWM3	I/O	General purpose I/O (8051 standard) / PWM DAC output (CMOS)
P1.4/PWM4	I/O	General purpose I/O (8051 standard) / PWM DAC output (CMOS)
P1.5	I/O	General purpose I/O (8051 standard)
P1.6	I/O	General purpose I/O (8051 standard)
P1.7	I/O	General purpose I/O (8051 standard)
P2.0	I/O	General purpose I/O (8051 standard)
P2.1	I/O	General purpose I/O (8051 standard)
P2.2	I/O	General purpose I/O (8051 standard)
P2.3	I/O	General purpose I/O (8051 standard)
P2.4	I/O	General purpose I/O (8051 standard)
P2.5	I/O	General purpose I/O (8051 standard)
P2.6	I/O	General purpose I/O (8051 standard)
P2.7	I/O	General purpose I/O (8051 standard)
P3.0/RXD	I/O	General purpose I/O / RXD (8051 standard)
P3.1/TXD	I/O	General purpose I/O / TXD (8051 standard)
P3.2/INT0#	I/O	General purpose I/O / INT0# (8051 standard)
P3.3/INT1#	I/O	General purpose I/O / INT0# (8051 standard)
P3.4/T0	I/O	General purpose I/O / T0 (8051 standard)
P3.5/T1	I/O	General purpose I/O / T1 (8051 standard)
P3.6/WR#	I/O	General purpose I/O / WR# (8051 standard)
P3.7/RD#	I/O	General purpose I/O / RD# (8051 standard)
P4.0/AD0	I/O	General purpose I/O (8051 standard) / ADC Input
P4.1/AD1	I/O	General purpose I/O (8051 standard) / ADC Input
P4.2/AD2	I/O	General purpose I/O (8051 standard) / ADC Input
P4.3/AD3	I/O	General purpose I/O (8051 standard) / ADC Input
V_{DD}	-	Power Supply
V_{SS}	-	Ground
X2	O	Oscillator output
X1	I	Oscillator input
RST	I	Active-high reset
ALE	O	Address Latch Enable
PSEN#	O	Program Store Enable
EA#	I	External Access Enable

Ps: See “5. PIN CONFIGURATION” for detail description of different pin output type.

8. FUNCTIONAL DESCRIPTIONS

8.1 8051 CPU Core

The CPU core of STK6011 is compatible to industry 8051 standard, and it consists of 256 bytes of RAM, special function registers (SFR), two timers, five interrupt sources, and a serial interface. The CPU core catches its program code from a 64K-byte Flash in STK6011.

When CPUclk is set, the CPU core can work at a double rate. And then the CPU operates as if a double-frequency crystal is applied to STK6011.

Note: Listed in this data sheet, all registers are collected in the external RAM area of 8051. You may refer to the 8051 specifications for an internal RAM memory map in detail.

8.2 Allocation of Memory

8.2.1 Internal Special Function Registers (SFR)

The SFR are the same as that of 8051 standard, except the P4 (D8h) and CHIPCON (BFh) registers.

STK6011 Special Function Registers

F8									FF
F0	B								F7
E8									EF
E0	ACC								E7
D8	**P4**								DF
D0	PSW								D7
C8									CF
C0									C7
B8	IP							**CHIPCON**	BF
B0	P3								B7
A8	IE								AF
A0	P2								A7
98	SCON	SBUF							9F
90	P1								97
88	TCON	TMOD	TL0	TL1	TH0	TH1			8F
80	P0	SP	DPL	DPH				PCON	87

Reg. Name	Addr.	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
P4	D8h(r/w)					P43	P42	P41	P40
CHIPCON	BFh(w)				XRAMen	ALEdis	CPUclk		

P4 (r/w) : Port4 is a bit addressable I/O port. Its usage is similar to other ports', all standing for "1" in Chip

Reset.

CHIPCON (w): Chip Configuration Register, all standing for "0" in Chip Reset

XRAMen = 1 → To enable the on-chip AUXRAM

= 0 → To disable the on-chip AUXRAM

ALEdis = 1 → To disable pin ALE output for low EMI

= 0 → To enable pin ALE output

CPUclk = 1 → CPU working at a double rate

= 0 → CPU working at a normal rate

8.2.2 Internal RAM (256 Bytes)

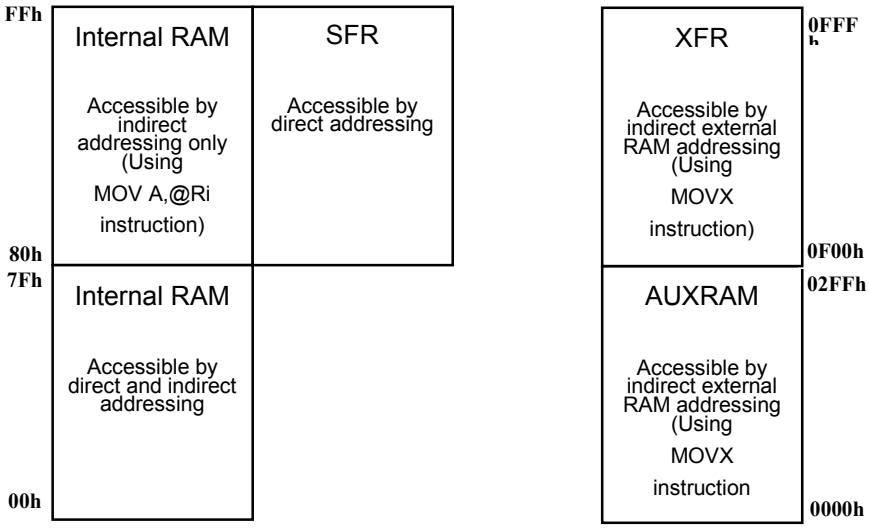
256 bytes of the internal RAM kept in STK6011 are the same as that of 8052 standard.

8.2.3 Auxiliary RAM (AUXRAM, 768 Bytes)

Total 768 bytes of the auxiliary RAM is configured in the 8051 external data memory area 0000h – 02FFh. Programs can use the "**MOVX @Ri**" instruction to access the AUXRAM memory area 0000h – 00FFh, or "**MOVX @DPTR**" instruction to access the AUXRAM full memory area 0000h – 02FFh. The AUXRAM is disabled after a reset. Setting the "XRAMen" bit in CHIPCON register will enable the access to AUXRAM. When AUXRAM is enabled, the "MOVX" instruction will always access to on-chip AUXRAM. At the time of execution from internal program memory, an access to AUXRAM will not affect the Port0, Port2, WR# and RD#.

8.2.4 External Special Function Registers (XFR)

The XFR is a group of registers configured in the 8051 external RAM area 0F00h – 0FFFh for the special functions. Programs can use the "MOVX " instruction to access these registers.



8.3 Pad Function Control

The Chip Configuration registers explain the chip configuration and the pin function.

Reg. Name	Addr.	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PADOPT	0F50h(w)					AD3E	AD2E	AD1E	AD0E
PADOPT	0F51h(w)	PWMf	PWMd		PWM4E	PWM3E	PWM2E	PWM1E	PWM0E

PADOPT (w): control registers in a pad mode, all standing for “0” in Chip Reset

AD3E = 1 → Pin “P4.3/AD3” for AD3

= 0 → Pin “P4.3/AD3” for P4.3

AD2E = 1 → Pin “P4.2/AD2” for AD2

= 0 → Pin “P4.2/AD2” for P4.2

AD1E = 1 → Pin “P4.1/AD1” for AD1

= 0 → Pin “P4.1/AD1” for P4.1

AD0E = 1 → Pin “P4.0/AD0” for AD0

= 0 → Pin “P4.0/AD0” for P4.0

PWMf = 1 → Selection of 94KHz PWM frequency

= 0 → Selection of 47KHz PWM frequency

PWMd = 1 → PWM pulse width for 253-step resolution

= 0 → PWM pulse width for 256-step resolution

PWM4E = 1 → Pin “P1.4/PWM4” for PWM4

= 0 → Pin “P1.4/PWM4” for P1.4

PWM3E = 1 → Pin “P1.3/PWM3” for PWM3

= 0 → Pin “P1.3/PWM3” for P1.3

PWM2E = 1 → Pin “P1.2/PWM2” for PWM2

= 0 → Pin “P1.2/PWM2” for P1.2

PWM1E = 1 → Pin “P1.1/PWM1” for PWM1

= 0 → Pin “P1.1/PWM1” for P1.1

PWM0E = 1 → Pin “P1.0/PWM0” for PWM0

= 0 → Pin “P1.0/PWM0” for P1.0

8.4 I/O Port

8.4.1 Port 0, 1, 2, 3

Port0 is a group of open drain pins, which is the same as that of 8051 standard.

Port1 is a group of pseudo-open drain pins, which is the same as that of 8051 standard if general-

purpose I/O port function is selected, or as CMOS output pins if PWM function is selected.

Port2, 3 are groups of pseudo-open drain pins, which is the same as that of 8051 standard.

8.4.2 Port 4

Port4 is a bit addressable I/O port. Its usage is similar to other ports'.

8.5 PWM DAC

Each 8-bit PWMDA register in XFR controls each output pulse width of PWM DAC converter. PWMf selects the frequency of PWM clock as 47KHz or 94KHz (for X'tal frequency = 12MHz), and PWMd selects the total duty cycle step of these DAC outputs as 253 or 256. In case of PWMd=1, writing FDH/FEH/FFH to DAC register makes output stably high. Writing 00H to DAC register makes the output stably low.

Reg. Name	Addr.	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PWMDA	0F20h(r/w)	Pulse width of PWM DAC 0							
PWMDA	0F21h(r/w)	Pulse width of PWM DAC 1							
PWMDA	0F22h(r/w)	Pulse width of PWM DAC 2							
PWMDA	0F23h(r/w)	Pulse width of PWM DAC 3							
PWMDA	0F24h(r/w)	Pulse width of PWM DAC 4							

PWMDA (r/w): The mentioned-above output pulse width control is used for DA0-4.

All of PWM DAC converters, after powered on, center on value 80h.

8.6 A/D converter

The STK6011 is installed with four 6-bit A/D converters in V_{DD} ranges. Software can choose a current converting channel by setting the SAD3/SAD2/SAD1/SAD0 bits. The refresh rate of the ADC may be gained by OSC freq./1536 (128μs for 12MHz crystal).

The voltage on the input pin is compared with the voltage on the internal V_{DD} x N / 64, where N=0-63, by the ADC. The ADC output value is N when pin voltage is higher than V_{DD} x N / 64 and lower than V_{DD} x (N+1) / 64.

Reg. Name	Addr.	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
ADC	0F10h ®			ADC converting result					
ADC	0F10h (w)	EADC				SAD3	SAD2	SAD1	SAD0

ADC (w): ADC control.

ENADC = 1→ To enable the ADC

SADC0 = 1→ To select the ADC0 pin input

SADC1 = 1→ To select the ADC1 pin input

SADC2 = 1→ To select the ADC2 pin input

SADC3 = 1→ To select the ADC3 pin input

ADC (r): ADC converting result

8.7 Low Power Reset (LVR)

The Low Power Reset has a chip reset signal increase when the voltage level of power supply goes below 75% of VDD in a specific period of time. After the voltage level of power supply rises above 75% of VDD, LVR stays at a reset state for 414 crystal cycles and make sure the chip exits from reset condition with a stable crystal oscillation.

8.8 Watchdog Timer

When Watchdog Timer overflows, it automatically ensures a device reset. The overflow interval is gained by 0.25 sec x N, in which N is a number ranging from 1 to 8, and it can be programmed by way of register WDT2-0. Since the timer function is disabled after power-on reset, users may enable this function by setting EWDT and clear the timer by setting WDTclr.

Reg. Name	Addr.	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
WDT	0F18h (w)	EWDT	WDTclr				WDT2	WDT1	WDT0

WDT (w): Watchdog Timer control register.

EWDT = 1 → To enable the Watchdog Timer

WDTclr = 1 → To clear the Watchdog Timer

WDT2: WDT0 = 0 → Overflow interval = 8 x 0.25 sec.

= 1 → Overflow interval = 1 x 0.25 sec.

= 2 → Overflow interval = 2 x 0.25 sec.

= 3 → Overflow interval = 3 x 0.25 sec.

= 4 → Overflow interval = 4 x 0.25 sec.

= 5 → Overflow interval = 5 x 0.25 sec.

= 6 → Overflow interval = 6 x 0.25 sec.

= 7 → Overflow interval = 7 x 0.25 sec.

(The list above is based on X'tal frequency = 12MHz)

8.9 Power Management

8.9.1 Idle Mode

Setting the IDL bit in the PCON register enters the idle mode. In the idle mode, the internal clock to the 8051 CPU core is stopped. The peripherals and the interrupt logic continue to be clocked. The CPU core will exit from the idle mode when either an interrupt or a reset occurs.

8.9.2 Power-down Mode

When the PD bit in the PCON register is set, the 8051 CPU core enters the power-down mode. In this mode, all of the clocks, including the X'tal oscillator, are stopped. To exit from the power-down mode, use a hardware reset or external interrupts INT0# to INT1# when enabled and set to level triggered.

If the external interrupt signal is longer than the X'tal oscillator stable time, the program will execute the interrupt service routine. If the external interrupts signal is shorter than the X'tal oscillator stable time, the program will execute the next PC.

8.9.3 Reduce EMI Emission (Disable ALE output)

The STK6011 allows users to reduce the EMI emission by setting the ALEdis bit in the CHIPCON register. This function will disable the clock signal in Fosc/6 Hz output to the ALE pin.

8.10 In-System Programming Function (ISP)

The STK6011 uses 8051 UART ports (P3.0/RXD, P3.1/TXD) to execute ISP function. The P3.0/RXD pin works as SCL pin of I^2C slave device, and the P3.1/TXD pin works as SDA pin of I^2C slave device.

The features of ISP are outlined below:

1. Block Erase: 128 Byte, 10ms
2. Whole Flash erase: 100ms
3. Byte programming Cycle time: 40 μs per byte
4. Whole 64K-byte Flash programming within 6 sec.
5. CRC check.

After Power On/Reset, The STK6011 runs the original Program Code. Once the S/W detects an ISP request, S/W can accept the request following the steps below:

1. Clear watchdog and disable all interrupts.
2. Write ISP control block slave address to ISPSLV.
3. Write 93h to the ISP enable register (ISPEN) to enable ISP.
4. Enter 8051 idle mode immediately.

When ISP is enabled, the STK6011 enters into ISP mode for 15-22.5 μs. In the mode, PWM DACs and I/O pins keep running at their former status.

Reg. Name	Addr.	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
ISPSLV	0F0Bh(w)	ISP Control Block Slave Address							
ISPEN	0F0Ch(w)	Write 93h to enable the ISP mode							

8.10.1 ISP Control Block

STK6011 built in an ISP control block that is an I^2C slave device. By this block, users can treat the 64K-

byte Flash as 32 EEPROM (like 24C16, called “EEPROM_like” in this data sheet). There are two types of I^2C bus transfer in this block:

Write: S-ttttttt0k-000000wwk-ddddddddk-P

Read: S-ttttttt1k-CCCCCCCCK-cccccccK-P

Where

S = start — P = stop

tttttt = ISP Control Block Slave Address — ww = word address

k = ack by slave — K = ack by host (0 or 1)

dddddddd = data

CCCCCCCC = crc_register[15:8] — cccccccc = crc_register[7:0]

Addr.	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
00h(w)	SDP	SDUP	ERASE	BLANK			CRCclr	CPUclr
01h(w)				BANK4	BANK3	BANK2	BANK1	BANK0
02h(w)	EPSadr							

00h(w):

SDP = 1 → To enable the S/W data protection of Flash. User needs to set this bit at the end of ISP mode

SDUP = 1 → To disable the S/W data protection of Flash. User needs to set this bit at the start of ISP mode

ERASE = 1 → To erase one page (128-byte) of Flash

BLANK = 1 → To erase whole Flash

CRCclr = 1 → To clear CRC register

CPUclr = 1 → To reset STK6011

Above 6 bits will be cleared by I^2C STOP condition. And only one bit can be set to 1 at the same time.

01h(w):

BANK4 - 0: EEPROM_like bank selection. Choice any one of EEPROM_like to access.

02h(w):

EPSladr : EEPROM_like slave address

8.10.2 Start to ISP Data Write/Read

In STK6011, the ISP function works following the steps below:

1. Define EEPROM_like slave address.
2. Set SDUP bit to disable Flash software data protection.
3. Set CRCclr bit to reset CRC_register.
4. Define the bank of EEOPRM_like.
5. Set ERASE/BLANK bit to block-erase/chip-erase Flash.
6. Access EEOPRM_like as standard EEPROM.
7. Check CRC_register.
8. Set SDP bit to enable Flash software data protection.

9. Set CPUclr bit to reset STK6011.

The steps between 4 and 6 are recycled until all data are written into Flash.

There are four types of I^2C bus transfer in EEPROM_like:

Byte Write: S-ttttAAA0-k-wwwwwwww-k-dddddddd-k-P

Page Write: S-ttttAAA0-k-wwwwwwww-k-dddddddd-k-dddddddd-k- … -P

Random Read: S-ttttAAA0-k-wwwwwwww-k(-P)-S-ttttAAA1-k-dddddddd-K-P

Sequential Read: S-ttttAAA0-k-wwwwwwww-k(-P)-S-ttttAAA1-k-dddddddd-K-dddddddd-K- … -P

Where

S = start or re-start
P = stop

tttt = EEPROM_like Slave Address

AAA = page block address
wwwwwwww = word address

k = ack by slave
K = ack by host (0 or 1)

dddddddd = data

The word address automatically increases every time when data byte is transferred. The page size is 256-byte.

In STK6011 Flash memory, the program cycle time is 40 μs. If the ISP slave is not able to complete the program cycle in time, it returns non-ack to the following data byte. In the meantime, the word address does not increase and the CRC does not count the non-acked data byte.

8.10.3 Cyclic Redundancy Check (CRC)

The ISP Host is able to read the ISP Control Block directly to get the CRC value, instead of reading each byte in Flash. The CRC register counts each data byte acknowledged by the ISP slave during data program period. All bits “1” will be loaded into 16 bits of the CRC register by setting CRCclr bit. MSB is the data byte first shifted into the CRC register.

```
CRCin = CRC[15]^DATAin;
CRC[15:0] = {CRC[14]^CRCin, CRC[13:2], CRC[1]^CRCin, CRC[0], CRCin};
```

Where^ = XOR

example:

data_byte	CRC_register_remainder
	FFFFH
F6H	FF36H
28H	34F2H
C3H	7031H

9. MEMORY MAP of XFR

Reg. Name	Addr.	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
ISPSLV	0F0Bh(w)	ISP Control Block Slave Address							
ISPEN	0F0Ch(w)	Write 93h to enable the ISP mode.							
ADC	0F10h (w)	ENADC				SADC3	SADC2	SADC1	SADC0
ADC	0F10h (r)	ADC Converting Result							
WDT	0F18h (w)	EWDT	WDTclr				WDT2	WDT1	WDT0
PWMDA	0F20h(r/w)	Pulse width of PWM DAC 0							
PWMDA	0F21h(r/w)	Pulse width of PWM DAC 1							
PWMDA	0F22h(r/w)	Pulse width of PWM DAC 2							
PWMDA	0F23h(r/w)	Pulse width of PWM DAC 3							
PWMDA	0F24h(r/w)	Pulse width of PWM DAC 4							
PADOPT	0F50h(w)					AD3E	AD2E	AD1E	AD0E
PADOPT	0F51h(w)	PWMf	PWMd		PWM4E	PWM3E	PWM2E	PWM1E	PWM0E

10. ELECTRICAL PARAMETERS

10.1 DC Characteristics

Conditions at: Ta=0 ~ 70 °C, V_{DD}=5.0V/3.3V, V_{SS}=0V

Name	Symbol	Conditions	Min.	Max.	Unit
Output "L" Voltage	Vol	Iol=5mA		0.45	V
Output "H" Voltage on 8051 I/O port pin	Voh1	V_{DD}=5V, Ioh=-50μA	4		V
	Voh2	V_{DD}=3.3V, Ioh=-50μA	2.65		V
Output "H" Voltage on CMOS output	Voh3	V_{DD}=5V, Ioh=-4mA	4		V
	Voh4	V_{DD}=3.3V, Ioh=-4mA	2.65		V
Input "L" Voltage	Vil1	V_{DD}=5V	-0.3	0.2 x V_{DD}	V
	Vil2	V_{DD}=3.3V	-0.3	0.3 x V_{DD}	V
Input "H" Voltage	Vih1	V_{DD}=5V	0.4 x V_{DD}	V_{DD} +0.3	V
	Vih2	V_{DD}=3.3V	0.6 x V_{DD}	V_{DD} +0.3	V
RST Pull-down Resistor	Rrst	V_{DD}=5V	150	250	Kohm
Pin Capacitance	Cio			15	pF

10.2 AC Characteristics

Conditions at: Ta=0 ~ 70 °C, V_{DD}=5.0V/3.3V, V_{SS}=0V

Name	Symbol	Conditions	Min.	Typ.	Max.	Unit
Crystal Frequency	fXtal			12		MHz
PWM DAC Frequency	fDA	fXtal=12MHz	46.875		94.86	KHz

10.3 Absolute Maximum Ratings

Conditions at: Ta= 0 ~ 70 °C, V_{SS}=0V

Name	Symbol	Range	Unit
Operating Temperature	Topg	0 ~ +70	°C
Storage Temperature	Tstg	-25 ~ +125	°C
Output Voltage	Vout	-0.3 ~ V_{DD}+0.3	V
Input Voltage	Vin	-0.3 ~ V_{DD}+0.3	V
Supply Voltage	V_{DD}5	-0.3 ~ +6.0	V
	V_{DD}3	-0.3 ~ +4.0	V

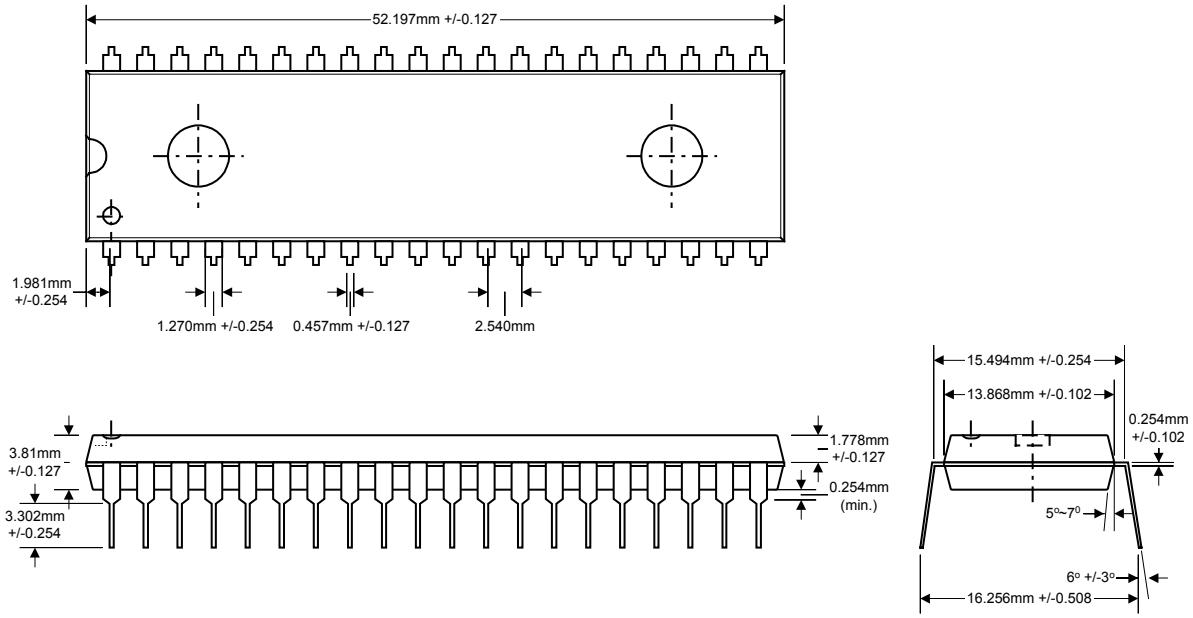
10.4 Operating Conditions Allowable

Conditions at: Ta= 0 ~ 70 °C, V_{SS}=0V

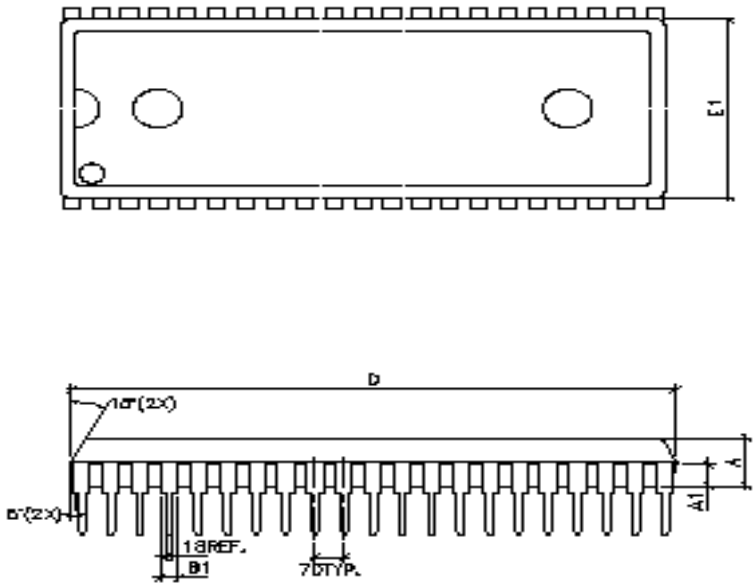
Name	Symbol	Conditions	Min.	Max.	Unit
Supply Voltage	V_{DD}	5V system	4.5	5.5	V
		3.3V system	3.0	3.6	V
Operating Freq.	Fopg		-	15	MHz

11. PACKAGE DIMENSION

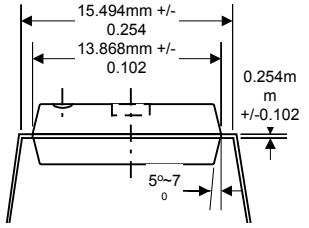
11.1 40-Pin PDIP 600 Mil



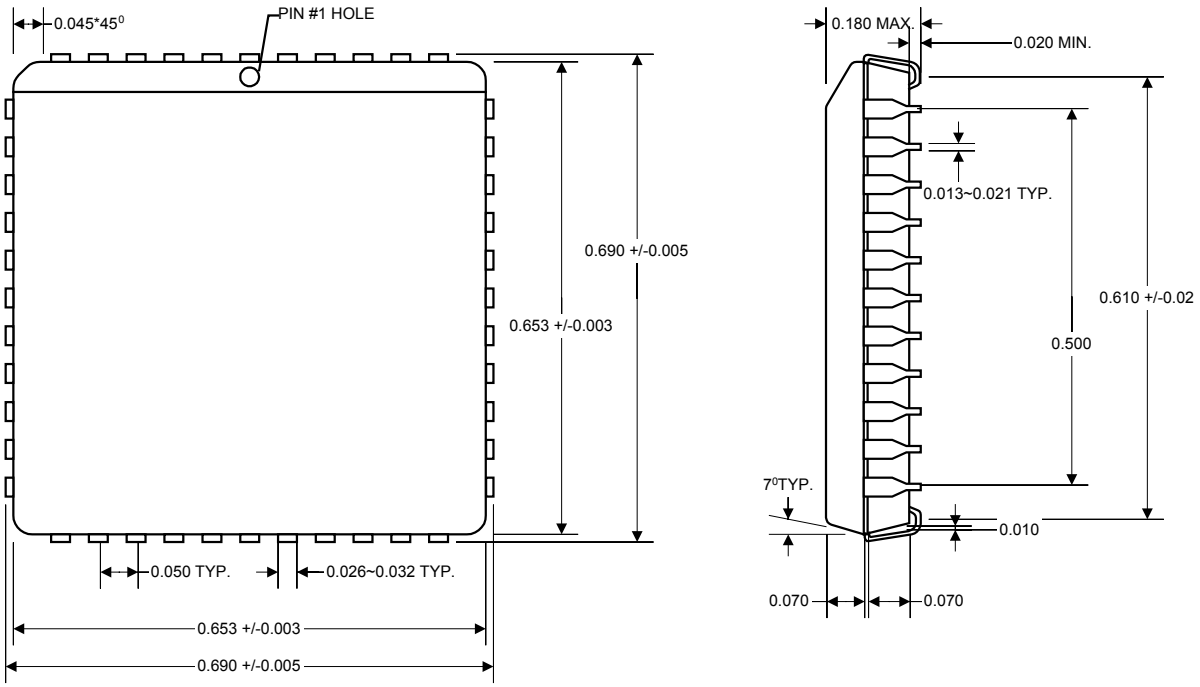
11.2 42-Pin SDIP Unit: mm



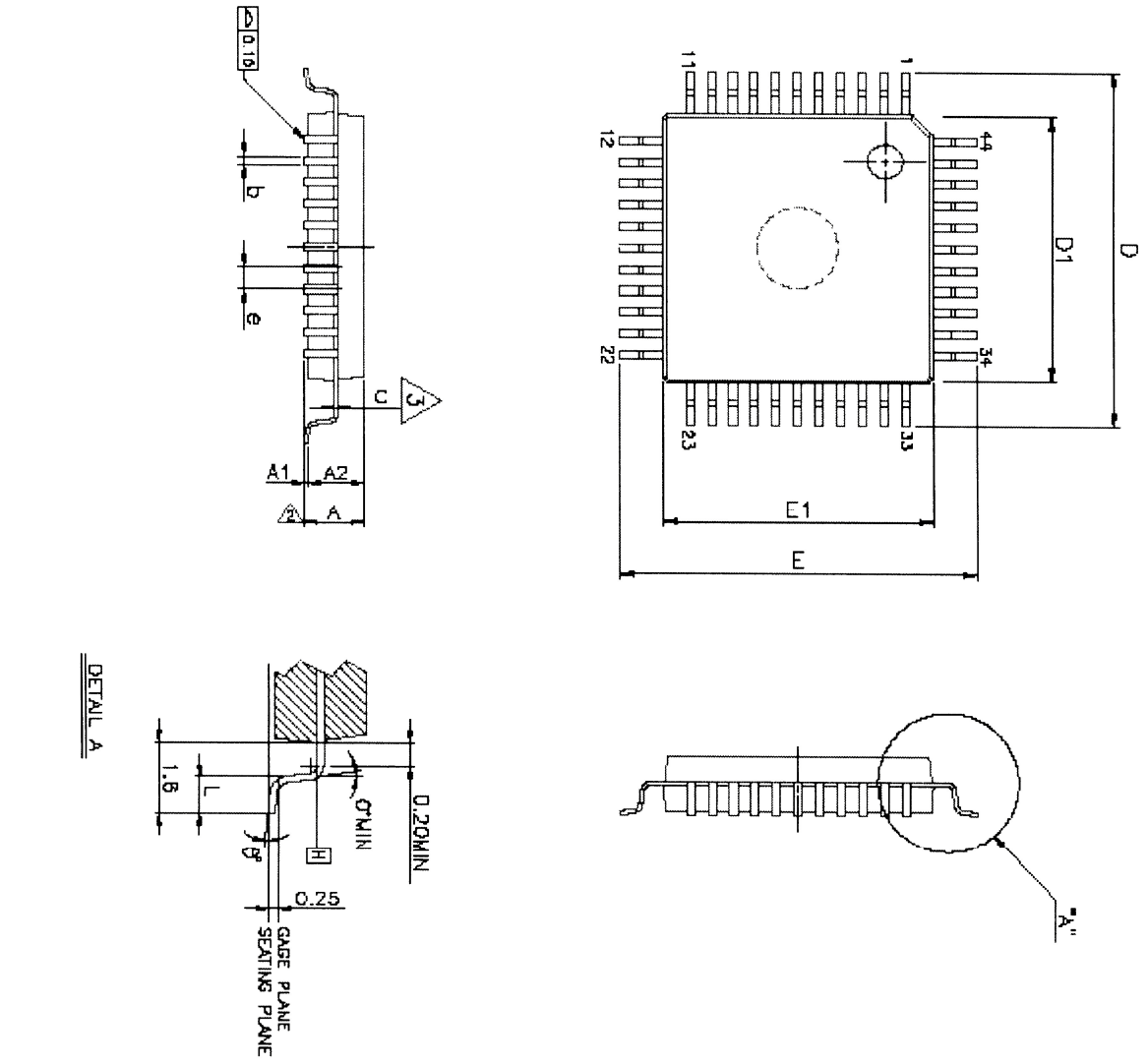
Symbol	Dimension in mm		
	Min	Nom	Max
A	3.937	4.064	4.2
A1	1.78	1.842	1.88
B1	0.914	1.270	1.118
D	36.78	36.83	36.88
E1	13.945	13.970	13.995
F	15.19	15.240	15.29
eB	15.24	16.510	17.78
θ	0°	7.5°	15°



11.3 44-Pin PLCC Unit:



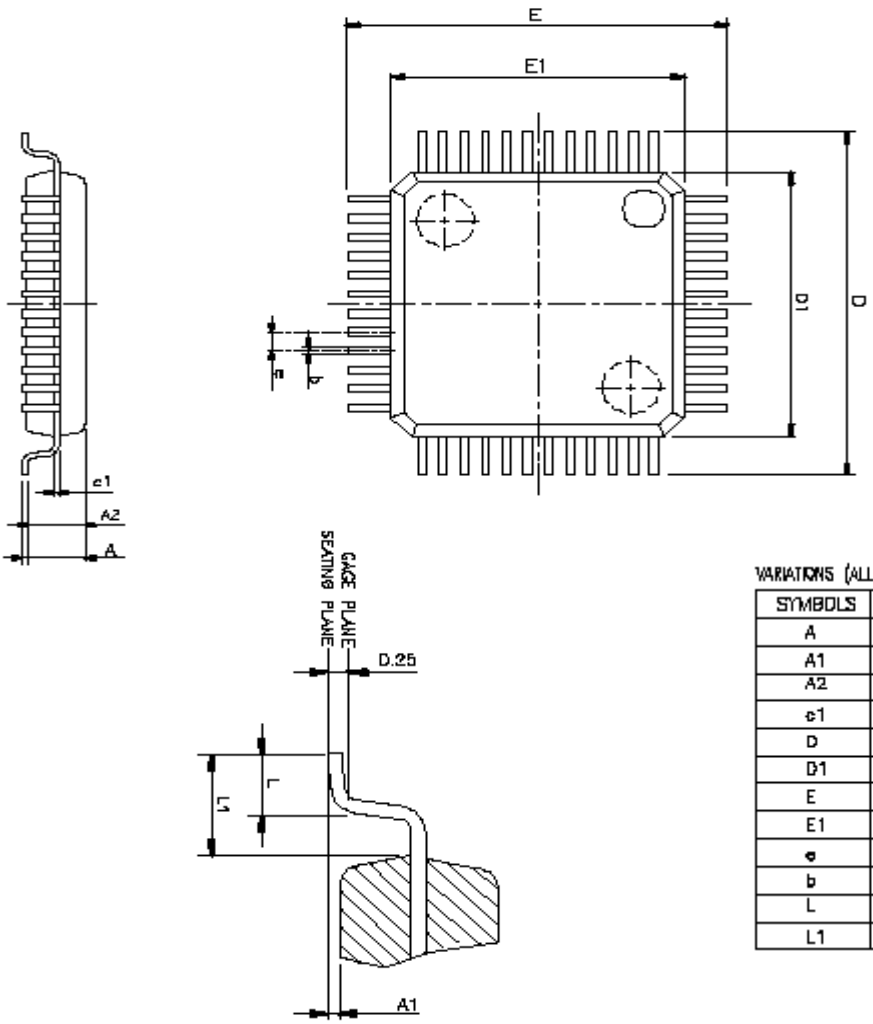
11.4 44-Pin QFP Unit:



SYMBOLS	MIN.	NOM	MAX.
A	–	–	2.7
A1	0.25	0.30	0.35
A2	1.9	2.0	2.2
b		0.3 (TYP.)	
D	13.00	13.20	13.40
D1	9.8	10.00	10.10
E	13.00	13.20	13.40
E1	9.8	10.00	10.10
L	0.73	0.88	0.93
e		0.80 (TYP.)	
θ	0	–	7
C	0.1	0.15	0.2

UNIT : mm

11.5 48-Pin LQFP Unit:



VARIATIONS (ALL DIMENSIONS SHOWN IN MM)

SYMBOLS	MIN.	MAX.
A	---	1.6
A1	0.05	0.15
A2	1.35	1.45
c1	0.09	0.16
D	9.00 BSC	
D1	7.00 BSC	
E	9.00 BSC	
E1	7.00 BSC	
e	0.5 BSC	
b	0.17	0.27
L	0.45	0.75
L1	1 REF	

12 ORDER INFORMATION

Part No.	Pin Count	Package	Marking
STK6011-P1	40	DIP	Syntek Logo STK6011-P1 Manu. No
STK6011-P2	42	SDIP	Syntek Logo STK6011-P2 Manu. No
STK6011-P3	44	PLCC	Syntek Logo STK6011-P3 Manu. No
STK6011-P4	44	PQFP	Syntek Logo STK6011-P4 Manu. No
STK6011-P5	48	LQFP	Syntek Logo STK6011-P5 Manu. No

13 CONTACT INFORMATION

If you need more detailed information or samples, PLS. contact the next window and then we will make a response to your request as best as we can.

太欣半導體股份有限公司 / **Syntek Semiconductor Co., Ltd.**
市場行銷部 / **Marketing & Sales Dept.**
經理 / **Marketing Manager**
劉政杰 / **Kevin Liu**
電話 **: 886 - 3-577-3181** 分機**: 528** / **Tel : 886 - 3-577-3181 Ext:528**
傳真**: 886 – 3-577-8010** / **Fax : 886 - 3-577-8010**
E-mail: cjliu@syntekt.com.tw
Mobile: 0936-060871