Ordering number : EN*A0483

Preliminary

SANYO Semiconductors
DATA SHEET

STK621-041, STK621-041A-E

Thick-Film Hybrid IC

Air Conditioner Three-Phase Compressor Motor Driver IMST Inverter Power Hybrid IC

Overview

The STK621-041 and STK621-041A-E are STK621-000 series products that use a miniature SIP package. These three-phase motor driver hybrid ICs integrate the power main circuit block and peripheral circuits needed for inverter control into a single package. The upper-side control power supply can be provided by a bootstrap circuit, making it possible to configure the control power supply with a single power supply (VD4 = 15V). This device also has a built-in high voltage-level shifter circuit for upper-side device drive signal transmission, and six input signals can be input from the same voltage potential (V_{SS}) as the control circuit. This enables direct connection from a control circuit such as a microcontroller without using a photo coupler or other insulating circuit.
A basic system configuration example is shown on page 2 (Figure: Inverter System Configuration Example).

Applications

- Air conditioner three-phase compressor motor driver.

Features

- Integrates the IGBT, FRD, pre-driver and protection circuits.
- Built-in thermal protection, overcurrent protection (bus line) and pre-driver supply under voltage protection.
- Allows CMOS-level input of control signals without an insulating circuit.
- Use of an upper-side power supply bootstrap circuit (externally set) enables single power supply drive.
- Built-in circuit for preventing short circuits when both upper and lower inputs are ON at the same time.
  This prevents arm short circuits due to simultaneous upper and lower phase ON inputs.
  (A dead time is needed to prevent short circuits due to switching delay.)
- Transfer full mold structure SIP. (Single Inline Package.)
- Integrates the three-phase power main circuit, pre-driver circuit, protection circuit and level shifter circuit needed for the inverter control circuit.
- IGBT and FRD used for the power main circuit devices.
- Built-in device protection circuits include an overcurrent protection circuit that detects and protects against minus bus line currents with an internal shunt resistor, an thermal protection circuit, and a control supply under voltage protection circuit. These circuits cut off the gates inside the IC and output an error signal (FAULT) when an abnormality occurs.

SANYO Semiconductor Co., Ltd.
TOKYO OFFICE Tokyo Bldg., 1-10, 1 Chome, Ueno, Taito-ku, TOKYO, 110-8534 JAPAN

- Built-in level shifter circuit allows CMOS-level input of upper-side device control signals from the same voltage potential as the lower-side device control signals. This enables direct input of six signals from the control circuit.
- The upper-side pre-driver circuit has reduced power consumption, so the upper-side control power supply can be configured using a bootstrap circuit (CB, Di). This makes it possible to configure the external control power supply using only a single lower-side power supply.
- Compact, easy-to-mount single inline (SIP) package.
- Analog signal output pin detects the minus bus line current with a shunt resistor.

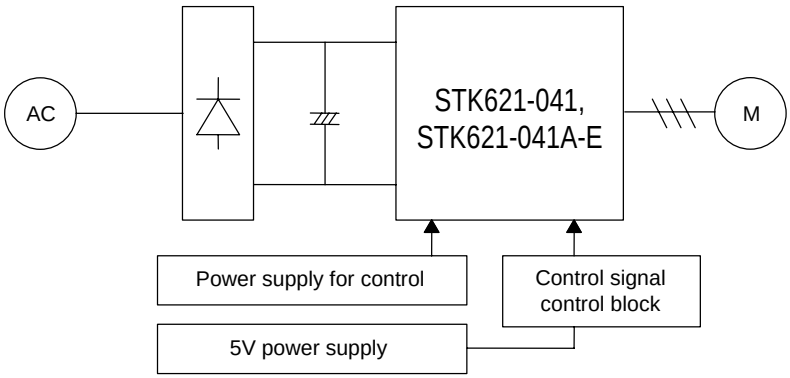


Figure Inverter System Configuration

Specifications

Maximum Ratings at Tc = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Supply voltage	V_{CC}	+ to - pins, surge < 500V *1	450	V
Collector-to-Emitter voltage	V_{CE}	+ to U (V, W) or U (V, W) to -	600	V
Output current	I_O	+, -, U, V, W pin current	±20	A
Output peak current	Iop	+, -, U, V, W pin current PW=100μs	±25	A
Control supply voltage	VD1, 2, 3, 4	VB1 - U, VB2 - V, VB3 - W, and $V_{DD} - V_{SS}$ *2	20	V
Input signal voltage	V_{IN}	HIN1, 2, 3, LIN1, 2, 3 pins	0 to 7	V
FAULT pin voltage	VFAULT	FAULT pin	20	V
Maximum power dissipation	Pd	IGBT, per 1 channel	34	W
Junction temperature	Tj	IGBT, FRD junction temperature	150	°C
Storage temperature	Tstg		-40 to+125	°C
Operating temperature	Tc	HIC case temperature	-20 to +100	°C
Tightening torque	MT	A screw portion *3	1.17	N•m
Insulation breakdown voltage	Vis	Sine wave 50Hz AC 1min	2000	VRMS

Unless otherwise specified, the voltage reference for - pins is the V_{SS} pin voltage.

*1 Surge voltage generated by switching operation due to the effects of wiring inductance between + and -.

*2 VD1 = voltage between VB1 and U; VD2 = voltage between VB2 and V; VD3 = voltage between VB3 and W; VD4 = voltage between V_{DD} and V_{SS}

*3 Heat sink plate-mounting flatness: 0.25mm or less

*4 Test conditions: AC 2500V for 1second

Electrical Characteristics at Tc=25°C, VD=15V

Parameters	Symbols	Conditions		min	typ	max	unit	Test circuit
Power output block								
Collector-to-emitter cut-off current	I_{CE}	V_{CE}=600V				2.0	mA	Fig.1
Collector-to-emitter saturation voltage	V_{CE}(SAT)	I_O=10A	Upper side		1.6	2.2	V	Fig.2
			Lower side		1.8	2.4		
Diode forward voltage	V_F	I_O=-10A	Upper side		1.7	2.3	V	Fig.3
			Lower side		1.9	2.5		
Junction-to-substrate thermal resistance	Rthj-c(T)	IGBT			3.0		°C/W	
	Rthj-c(D)	FWD			3.6			
Control (Pre-driver) block								
Control circuit current dissipation	I_D	VD1, 2, 3=15V			0.05		mA	Fig.4
		VD4=15V			10			
ON input signal voltage	V_{IH}	Output ON				0.8	V	
OFF input signal voltage	V_{IL}	Output OFF		2.2			V	
Protection block								
Thermal protection temperature	TSD	Substrate surface		100		120	°C	
Overcurrent protection current	ISD	P.W.=100μs		28		40	A	Fig.5
Control supply under voltage protection	UVLO			9		12	V	
FAULT pin intake current	IOSD	When FAULT operating (Low), VFAULT=1V			2		mA	
Switching time	TON	I_O=10A, Inductive load			1.0		μs	Fig.6
	TOFF				1.2			
Current output signal level	ISO	I_O=10A			0.167		V	

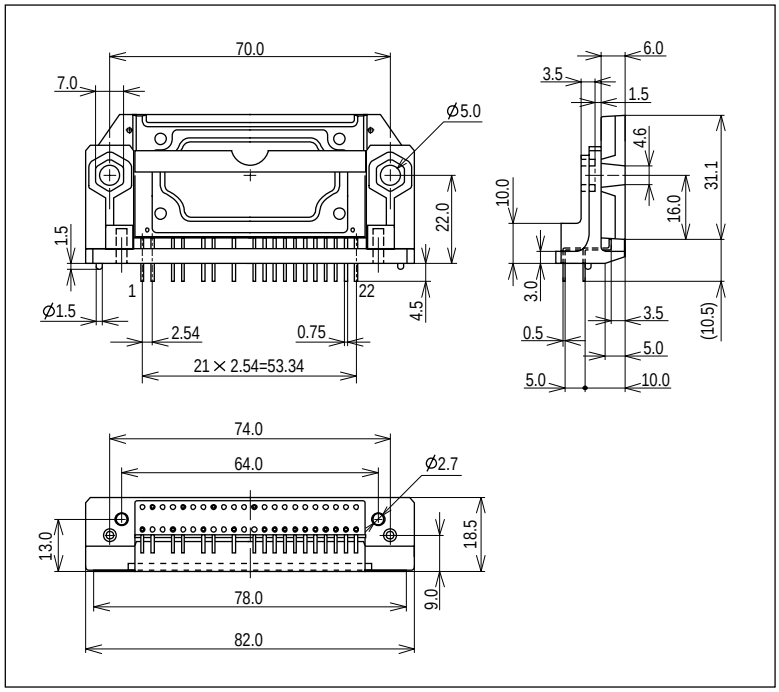
Unless otherwise specified, the voltage reference for - pins is the V_{SS} pin voltage.

Notes

1. The ON input signal voltage prescribes the input signal voltage at which the output stage IGBT turns ON, and the OFF input signal voltage prescribes the input signal voltage at which the output stage IGBT turns OFF.
   Apply a voltage between 0 and V_{IH} (max) when output is ON, and a voltage between V_{IL} (min) and V_{DD} when output is OFF.
2. After the internal protection circuit operates and the FAULT signal (Low = FAULT ON: open drain output) goes ON, the latch status continues as long as any of the six input signals is ON (Low). The latch status is reset after all six input signals are OFF (High) continuously for approximately 10μs.
   However, control supply under voltage protection (UVLO) operation is as follows.
   - Upper arm → The FAULT signal is not output, but the corresponding gate signal turns OFF.
     Note that even if the voltage recovers to normal, the latch status continues while the input signal is ON (Low).
   - Lower arm → The gate signal goes OFF and FAULT signal is output.
     However, unlike protection operation for the upper arm, operation returns to normal when the voltage recovers to normal. (Protection operation is not latched by the input signal.)
3. When using M4 screws to mount the IC to a heat sink plate, apply a tightening torque of 0.79 to 1.17 N•m. The heat sink plate-mounting flatness should be 0.25mm or less.
4. The control supply voltage-drop protection function protects the devices when the control supply voltage drops due to some abnormality during operation. Control supply voltage drop at the start of operation and other cases should be confirmed in the set-mounted condition.

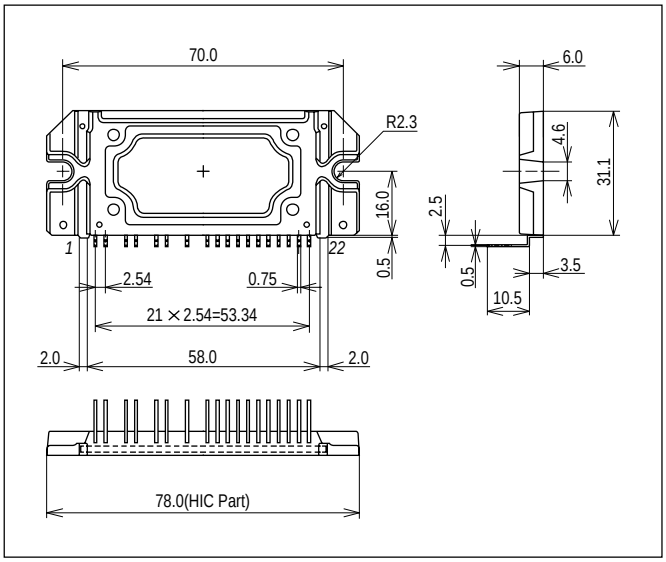
Package Dimensions

unit:mm (typ) [STK621-041]



Package Dimensions

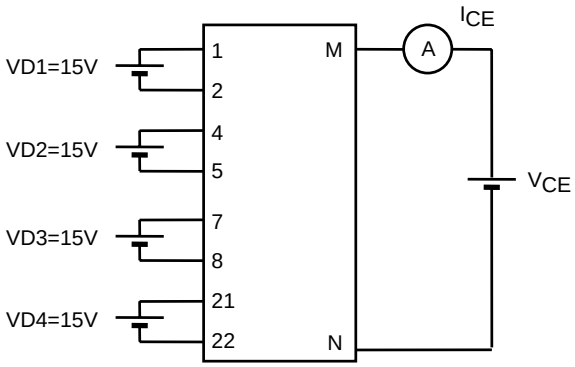
unit:mm (typ) [STK621-041A-E]



Test Circuit (Measured phase U+: upper U phase, U-: lower U phase)

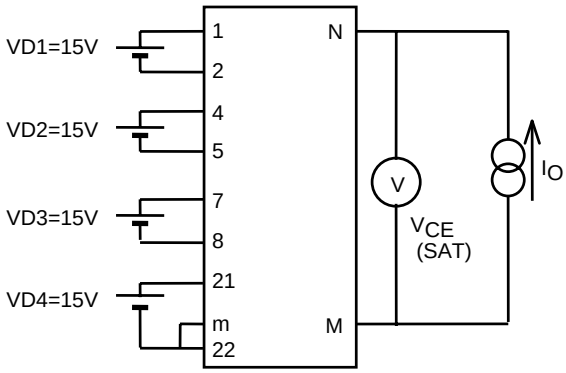
1: ICE

Measured phase	U+	V+	W+	U-	V-	W-
M	10	10	10	2	5	8
N	2	5	8	12	12	12



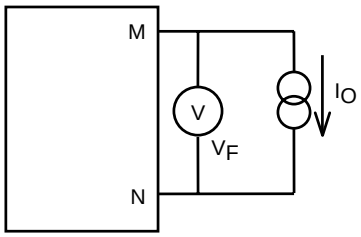
2: VCE (SAT) (Pulse measurement)

Measured phase	U+	V+	W+	U-	V-	W-
M	10	10	10	2	5	8
N	2	5	8	12	12	12
m	13	14	15	16	17	18



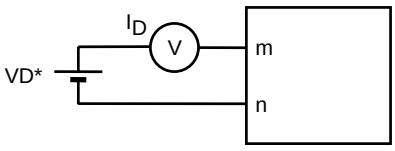
3: VF (Pulse measurement)

Measured phase	U+	V+	W+	U-	V-	W-
M	10	10	10	2	5	8
N	2	5	8	12	12	12

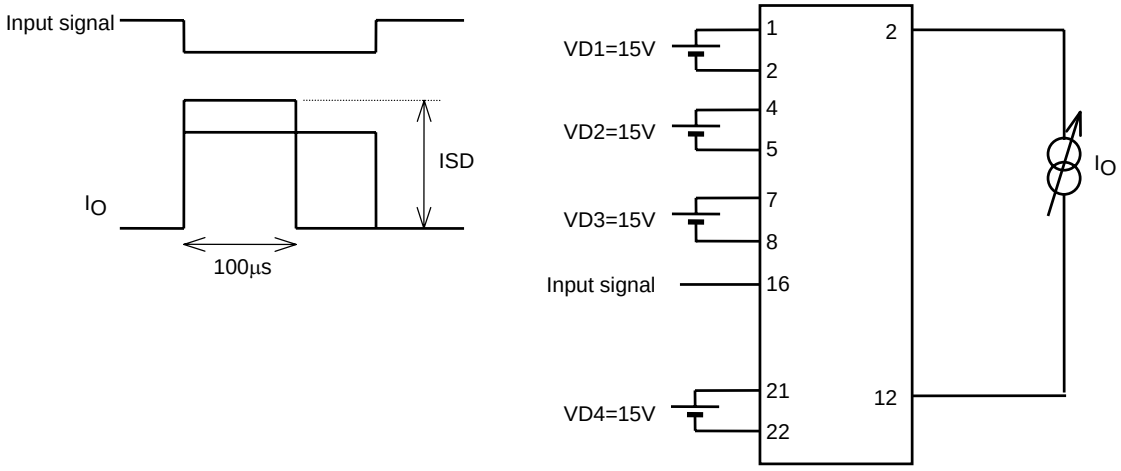


4: ID

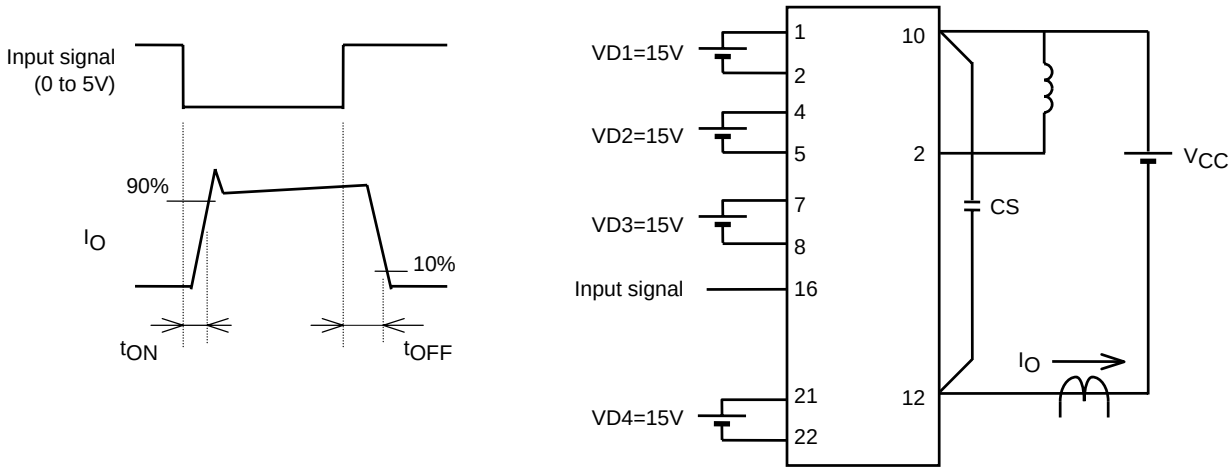
Measured phase	VD1	VD2	VD3	VD4
m	1	4	7	21
n	2	5	8	22



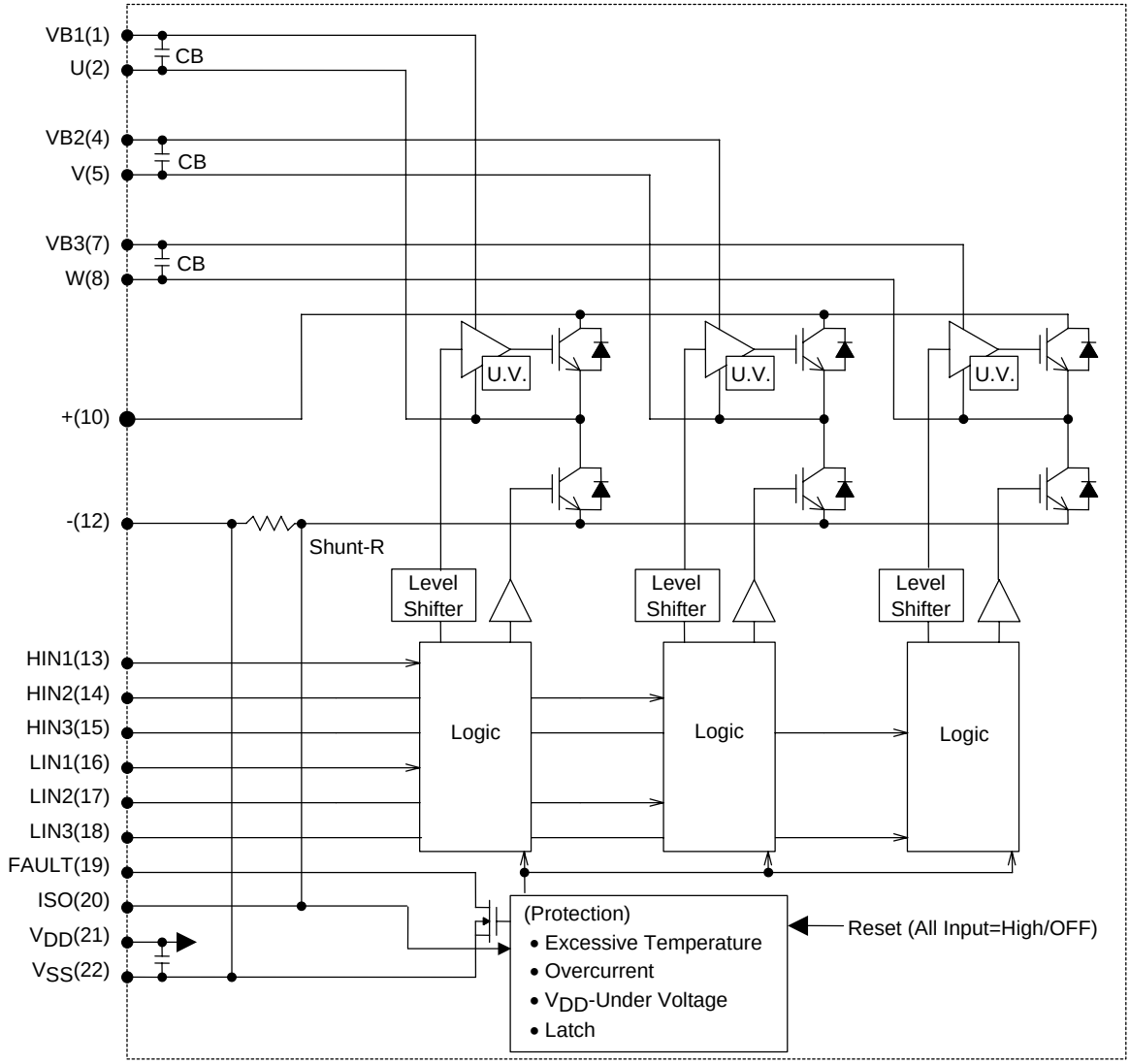
5: ISD



6: Switching time (Lower figure shows typical example of lower U phase.)



Block Diagram and Pin Description



Numbers in parentheses indicate the pin numbers.

(1) + and - pins (main circuit power supply input pins)

These pins are connected to the main DC power supply. Voltage up to V_{CC} can be applied. Spike voltage may be generated during switching operation and result in overvoltage due to the effects of the floating inductance of the connection wiring. Therefore, use a short wiring length to reduce the wiring inductance, and take measures to suppress surge voltage and voltage fluctuation such as connecting a snubber circuit for absorbing voltage surges as close as possible between the + and - pins.

(2) U, V and W pins

These output pins are connected to the three-phase motor. Note that these pins have the same voltage potential as the minus-side reference voltage potential of each upper-side control power supply, and are connected to the minus pins of the capacitors for each upper-side control power supply. Therefore, connect the capacitors as close to these pins as possible.

(3) V_{DD} and V_{SS} pins

These connect the pre-driver circuits for the lower-side power devices with the internal protection circuits and the external control power supplies for the logic circuits. The voltage over this section is monitored by the undervoltage protection circuit. (Operation stops when the voltage is insufficient.) In addition, the V_{SS} pin is the reference voltage potential for the control input signals, the FAULT signal and the ISO signal. Note that the V_{SS} pin is connected internally with the minus (-) pins. (The main circuit current cannot be taken from the V_{SS} pin.)

(4) VB1, VB2 and VB3 pins

These pins connect the positive power supplies for the upper-side power device pre-driver circuits. The three control power supplies each require an electrically insulated floating power supply. In addition to the method that uses three independent power supplies, this power supply can also be configured using the bootstrap circuit shown in Fig. 3. As shown in this figure, CB has a path (1) that is charged when the lower-side device is ON, and a path (2) for motor regeneration mode. The CB section voltage fluctuates according to the switching frequency and duty ratio of the external control circuit. Therefore, the CB capacitance value must be set in consideration of the voltage fluctuation. DB should use a high-speed type FRD with a fast t_{rr} and VR = 600V. RB is used to limit the rush charging current during CB initial charging. Note that a large rush charging current may cause the internal circuits to malfunction. CB can also be charged before startup by connecting high-value resistors to the output pins and minus pins. (Care must be taken for the withstand voltage and the power.)

The upper-side control power supply voltage is monitored by the under voltage protection circuit, and the respective phase output stops when the voltage is insufficient.)

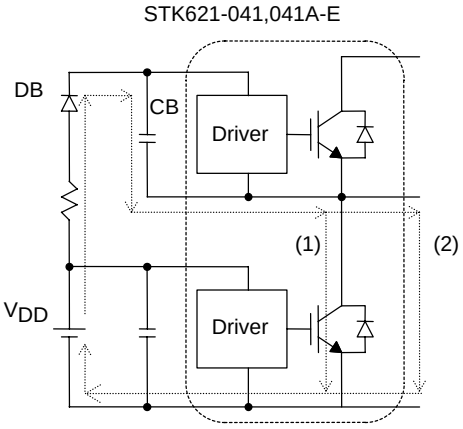


Figure 3 Bootstrap circuit and charge path

(5) Input (HIN1, HIN2, HIN3, LIN1, LIN2, LIN3) pins

Fig. 4 shows the input pin internal circuit. In the input block, the V_{DD} pin is pulled up internally by a 50kΩ resistor. The input signal is low active, and output is ON at a voltage of V_{IH} (max) or less, and OFF at a voltage of V_{IL} (min) or more. This allows direct input to the input pin from a 5V control circuit. When using direct connection from the control circuit, the connection block on the control circuit side is pulled up by a 50kΩ resistor, so the voltage potential may be higher than 5V. In cases when this voltage may exceed the withstand voltage of the connection block, an effective measure is to connect an external resistor of several kΩ between the external 5V power supply and the input pin. Note that this external resistor also effectively absorbs input pin noise when the pin is susceptible to noise in an actual set. HIN1, HIN2 and HIN3 are the inputs for the U, V and W upper-side power devices, and LIN1, LIN2 and LIN3 are the inputs for the lower-side power devices. An anti-simultaneous ON circuit is built-in to prevent arm short-circuits when both the upper and lower inputs for each phase are ON at the same time. However, a dead time must always be provided between signals to prevent arm short-circuits due to the power device switching response delay.

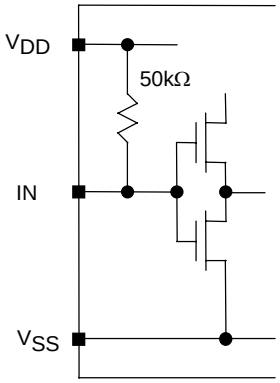


Figure 4 Input circuit block

(6) FAULT pin

The FAULT pin is an open drain output as shown in Fig. 5. When protection operation starts, the MOSFET turns ON and the FAULT pin goes Low. At this time, the intake current IOSD is 2mA (at voltage of 1V). This should be taken into account when connecting an external circuit. When pulling up the pin with a resistor, connect 5.6kΩ or more.

The protection circuits that operate the FAULT pin are the overcurrent protection circuit and the lower-side drive supply voltage (V_{DD} - V_{SS}) under-voltage protection circuit. The FAULT pin does not operate during upper-side power supply under-voltage protection. All power devices are OFF while the FAULT pin is Low. FAULT is latched when any of the inputs are ON (except VDUV), and is reset by turning all six inputs OFF.

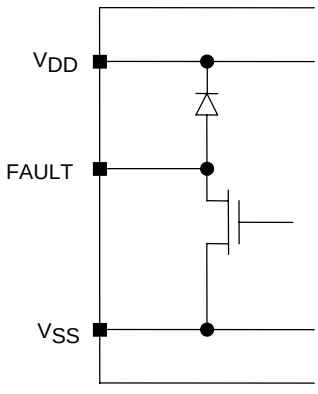


Figure 5 FAULT output block

(7) ISO pin

This is the current monitor pin. This pin outputs the positive direction current flowing to the shunt resistor inserted into the - (minus) pin line as a voltage signal. (Negative direction current is not output.) Note that overcurrent protection is disabled when this pin is shorted with V_{SS}. When connecting an external circuit to this pin, the external circuit impedance should be 5.6kΩ or more.

Protection Circuits

The STK621-041 and STK621-041A-E have the following built-in protection functions.

(1) Thermal protection (TSD)

When the HIC internal board temperature rises to the set temperature or higher, the thermal protection circuit operates to cut off all six device outputs and latch the FAULT pin Low. The TSD temperature is prescribed by the heat sink board temperature when the FAULT pin inverts in the condition with the HIC externally warmed.

(2) Overcurrent protection (ISD)

This function detects the bus line current using a shunt resistor provided on the minus pin side. When the set current is exceeded, all six device outputs are cut off and the FAULT pin is latched Low. A dead zone is provided so that the circuit does not respond to pulse currents with a width less than several μs in order to prevent malfunction due to the diode recovery current or noise. Therefore, note that the overcurrent protection circuit may not operate when large pulse currents shorter than that width flow repeatedly.

(3) V_{DD} under voltage protection (VDUV)

When V_{DD} drops below the prescribed voltage (10.5V, typ.), all six device outputs are cut off and the FAULT pin is latched Low. Operation returns to normal when the voltage recovers.

(4) VBS under voltage protection (VBSUV)

When the upper-side control supply voltage VBS drops below the prescribed voltage (10.5V, typ.), the output of that channel is cut off and the channel is latched until the corresponding input signal goes OFF. (The channel is automatically reset when the input signal goes OFF.)

(5) Arm short circuit input protection function

When the upper and lower channel ON signals are input at the same time, this status is judged by the internal logic circuit and both gate signal outputs are turned OFF to prevent an arm short circuit. Operation returns to normal when either of the signals goes OFF.

(6) Latch reset

The latch states established by (2) and (3) above are canceled when all six inputs are OFF (10μs or more).

Application Circuit Example

A typical application circuit is shown below.
The STK621-041 and STK621-041A-E can configure the pre-driver power supply with a single power supply. In addition, the control signals can be input directly from the control circuit (microcontroller or other 5V system circuit). Note that the pre-driver power supply can also use a conventional four power supply configuration, so the appropriate configuration can be selected according to the applied set.

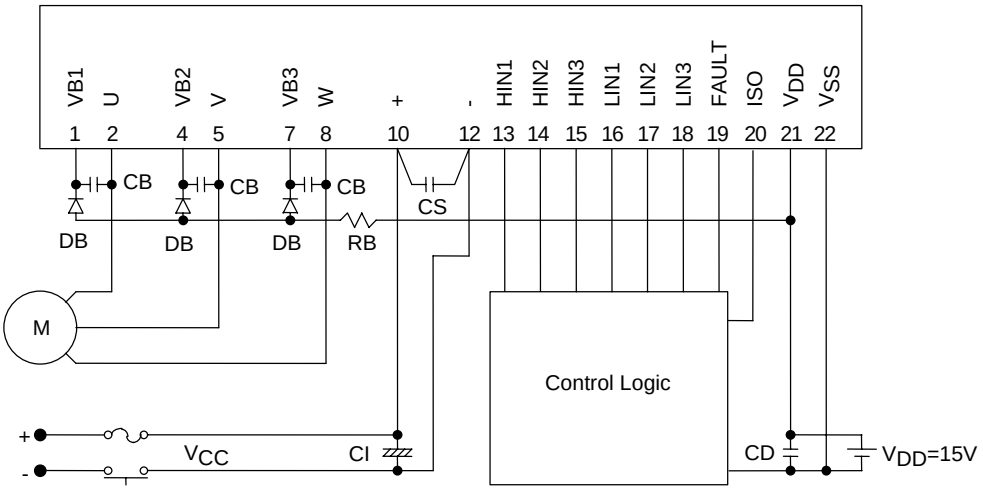


Figure 6 Sample Application Circuit (when power/control signal are directly supplied)

Recommended Operating Conditions

Parameters	Symbol	Conditions	min	typ	max	unit
Supply voltage	V_{CC}	+ to - pins	0	280	400	V
Control supply voltage	VD1, 2, 3	VB1-U, VB2-V, VB3-W	12.5	15	17.5	V
	VD4	V_{DD}-V_{SS} *1	13.5	15	16.5	
ON input signal voltage	V_{IN}(ON)	HIN1, HIN2, HIN3, LIN1, LIN2, LIN3 pins	0		1	V
OFF input signal voltage	V_{IN}(OFF)		4	5	V_{DD}	V
PWM frequency	fPWM		1		10	kHz
Dead time	DT	Upper/lower phase input signal downtime	2			μs
Tightening torque		'M4' type screw	0.79		1.17	N•m

*1 Control power supply (VD4=15±1.5V) must have the capacity of I_O=20mA(DC) and 0.5A (Peak).

Precautions

1. The control power supply can be driven by a single power supply by connecting a bootstrap diode: DB (use a high-speed diode with a short t_{rr} and a withstand voltage of 600V or more) and a capacitor: CB (approximately 1 to 47μF). In this case, CB is charged by setting the lower-side device to ON (Low output). Note that a large charging current flows during startup and in other cases when the CB voltage is low, and may cause adverse effects such as noise. Be sure to connect a limiting resistor: RB (approximately several Ω to several tens of Ω).
   (When not using the bootstrap method, each upper-side control power supply should be externally supplied by an independent power supply.)
   In addition, the upper-side control voltage may be insufficient depending on the control signal input status, so this should be checked.

2. Fluctuating spike voltage may be generated during switching operation due to the effects of the floating inductance of the + and - pin power supply external wiring or other factors. Therefore, use a short wiring length (between CI and each pin) to reduce the wiring inductance, and take measures to suppress surge voltage such as connecting a snubber circuit (capacitor: CS, approximately 0.1 to 10μF) for absorbing voltage surges as close as possible between the + and - pins.

3. The ISO pin (pin 20) is the current monitor pin. Note that overcurrent protection is disabled when the ISO pin and the V_{SS} pin are shorted.

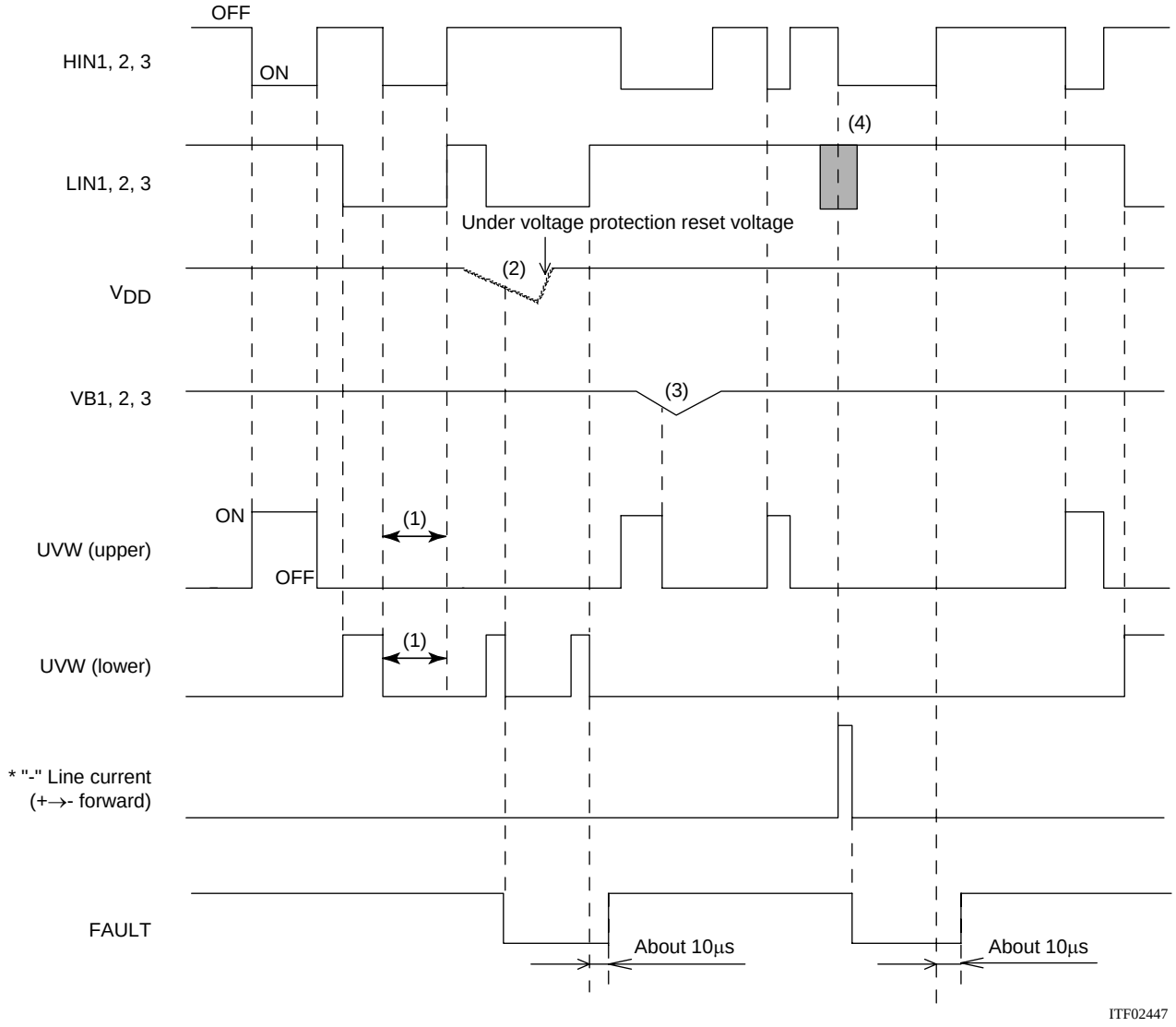
4. The FAULT pin is an open drain output (FAULT operation when Low). When pulling up the FAULT pin, use 5.6kΩ or more.

5. A 5V (5.0 to 5.4V) Zener diode is connected inside the signal input pins. When inputting voltage in excess of 5V, connect a resistor between the power supply side and the signal input pin so that the input current to the signal input pin is 0.5mA or less. This resistor is also effective for absorbing noise.

6. The overcurrent protection function is valid only when circuit control can be performed normally. Be sure to provide a fuse in the V_{CC} line or otherwise ensure safety in the set design.

7. The IC may become damaged or rupture if the motor connection pins (pins 2, 5 and 8) are open during motor rotation. Take special care for the connections (soldered condition) of these pins.

STK621-041, 041A-E Logical Timing Chart



* The ‘‘-’’ line current shows only the short circuit current in order to explain overcurrent protection operation.

Notes

1. (1) is the timing chart when the anti-simultaneous ON circuit in the signal input block has operated.
   (Note that a dead time must be externally set to prevent a short circuit due to switching delay.)

2. When the lower phase V_{DD} is insufficient, all gate output signals is set to OFF and the FAULT output is set Low. However, unlike the upper phase protection operation, the latch state is canceled and the FAULT output is set High approximately 10μs after the voltage recovers to normal and all six phase inputs go OFF. (2)

3. When the upper phases VB1, VB2 and VB3 are insufficient (3), only the upper phase outputs of the corresponding phases are set to OFF, and FAULT output is not performed. However, the output OFF latch status continues while the input signals are ON. After VB1, VB2 and VB3 recover, the outputs are returned to operating status by re-inputting the signals to the upper phases.

4. Overcurrent protection operation is as follows. (This describes the case when a load short circuit occurs only during the gray portion (4).) When an overcurrent flows, the HIC internal overcurrent protection circuit operates and performs control to set the IGBT for all phases to OFF. In addition, the FAULT output is also set Low at this time. After protection operation ends, the latch status is canceled and the FAULT output is set High approximately 10μs after all six inputs go OFF.