Ordering number : ENN7441A

Thick-Film Hybrid IC

STK672-060

Stepping Motor Driver (Sine Wave Drive) Output Current: 1.2 A (No Heat Sink*)

Unipolar constant-current chopper (external excitation PWM) circuit with built- in microstepping controller

Overview

The STK672-060 is a stepping motor driver hybrid IC that adopts power MOSFETs in its output stage. It features a built-in microstepping controller that implements unipolar constant current PWM drive. Since this IC includes a 4-phase distribution controller for stepping motors, it can contribute not only to system simplification but to circuit standardization as well.

The STK672-060 supports the 2 phase, 1-2 phase, W1-2 phase, 2W1-2 phase, and 4W1-2 phase excitation (drive) methods and can control the motor with the basic stepping angle of the stepping motor divided into up to 16 divisions. Motor rotation can also be controlled with just the clock signal.

This hybrid IC can implement highly efficient drive with high motor torque, low vibration, low noise, and fast response. As compared to the earlier Sanyo STK672-010 series, the STK672-060 features a smaller package, fewer required external components, and improvements to the controller for high functionality high performance microstepping drive.

Applications

- Facsimile unit stepping motor drive for both transmission and reception
- Paper feed and optical system stepping motor drive in copiers
- Laser printer drum drive
- Printer carriage stepping motor drive
- X/Y plotter pen drive
- Other stepping motor applications

Features

- The STK672-060 can implement a stepping motor drive system with just the provision of a DC power supply and a clock pulse generator.

<Control Block Features>

The excitation mode settings (M1, M2, and M3) select one of five excitation methods.

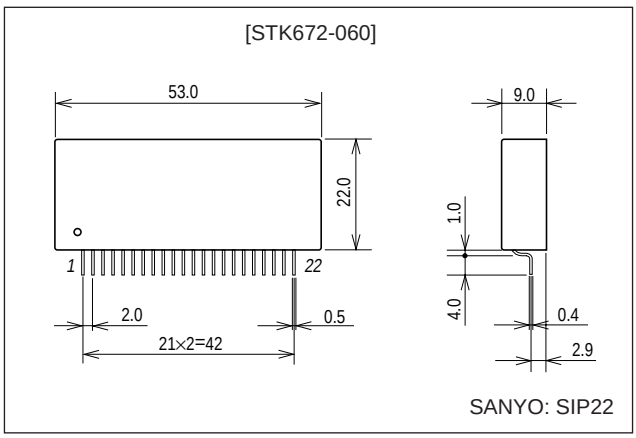
- 2 phase excitation
- 1-2 phase excitation
- W1-2 phase excitation
- 2W1-2 phase excitation
- 4W1-2 phase excitation

Continued on next page.

Package Dimensions

unit: mm

4161-SIP22



Notes*: Conditions: $V_{CC}1$ = 24 V, I_{OH} = 1.2 A, 2W1-2 excitation mode

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22004TN (OT) No. 7441-1/19

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- To match the motor characteristics, the vector locus during microstepping drive can be selected to be any one of four modes: circular mode, one inside mode, and two outside modes.
- The phase is retained if excitation is switched during operation.
- The excitation phase state can be verified in real time using the MO1, MO2, and MOI signal output pins.
- The clock input counter block supports two signalsense modes selected by the high or low state of the M3 pin.
  —Rising edges only
  —Both rising and falling edges
- The CLK and RETURN input pins have built-in circuits that prevent malfunctions due to external noise pulses.
- Both an ENABLE and a $\overline{\text{RESET}}$ pin are provided as Schmitt trigger inputs with built-in 20 kΩ (typical) pull-up resistors.
- No audible noise is generated by the differences in the time constant between phases A and B when the motor position is held fixed due to the adoption of external excitation.
- The reference voltage Vref can be set to any level between 0 and 1/2 $V_{CC}2$. This allows the STK672-060 to provide microstepping operation even for small motor currents.

<Drive Block>

- Provides a wide range of operating supply voltage required for external excitation PWM drive ($V_{CC}1$ = 10 to 45 V).
- Current detection resistor (0.22 Ω) built-in the hybrid IC itself.
- Power MOSFETs adopted for low drive loss.
- Provides a motor output drive current of I_{OH} = 1.2 A.

Specifications

Absolute Maximum Ratings at Tc = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage 1	$V_{CC}1$ max	No signal	52	V
Maximum supply voltage 2	$V_{CC}2$ max	No signal	–0.3 to +7.0	V
Input voltage	V_{IN} max	Logic input pins	–0.3 to +7.0	V
Phase output current	I_{OH} max	0.5 s, 1 pulse, when $V_{CC}1$ applied	1.6	A
Repeated avalanche resistance	Ear max		25	mJ
Power dissipation	Pd max	θc-a = 0	7	W
Operating IC substrate temperature	Tc max		105	°C
Junction temperature	Tj max		150	°C
Storage temperature	Tstg		–40 to +125	°C

Allowable Operating Ranges at Ta = 25°C

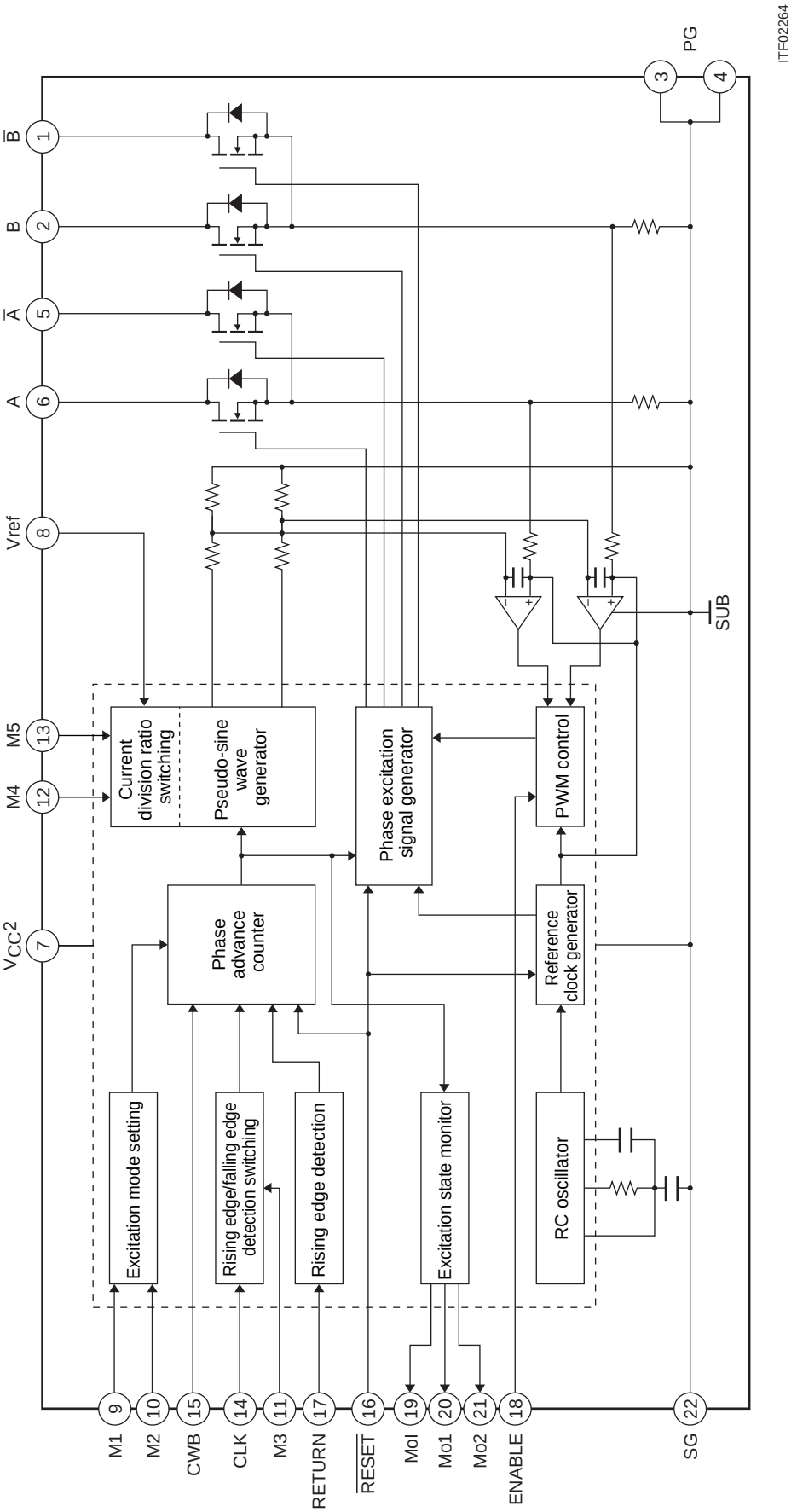
Parameter	Symbol	Conditions	Ratings	Unit
Supply voltage 1	$V_{CC}1$	When the input signal is present	10 to 45	V
Supply voltage 2	$V_{CC}2$	When the input signal is present	5 ±5%	V
Input voltage	V_{IH}		0 to $V_{CC}2$	V
Phase drive voltage handling capacity	V_{DSS}	Transistors 1, 2, 3, and 4 (outputs A, $\overline{\text{A}}$, B, and $\overline{\text{B}}$)	100 (min)	V
Phase current	I_{OH} max	Duty 50%	1.2 (max)	A

Electrical Characteristics at Tc = 25°C, $V_{CC}1$ = 24 V, $V_{CC}2$ = 5 V

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Control power supply current	I_{CC}	The hybrid IC pin 7 input, ENABLE = low		2.5	14	mA
Output saturation voltage	Vsat	R_L = 23 Ω (I ≈ 1A)		0.8	1.1	V
Average output current	Io ave	Load: R = 3.5 Ω. L = 3.8 mH per phase, Vref ≈ 1.69 V	0.470	0.524	0.580	A
FET diode forward voltage	Vdf	If = 1 A		1.2	1.8	V
[Control Input Pins]						
Input voltage	V_{IH}	Except for the Vref pin	4			V
	V_{IL}	Except for the Vref pin			1	V
Input current	I_{IH}	Except for the Vref pin	0	1	10	μA
	I_{IL}	Except for the Vref pin	125	250	510	μA
[Vref Input Pin]						
Input voltage	V_I	H-IC pin 8	0		2.5	V
Input current	I_I	H-IC pin 8, V_I = 2.5 V	330	415	545	μA
[Control Output Pins]						
Output voltage	V_{OH}	I = –3 mA, MoI, Mo1, Mo2 pins	2.4			V
	V_{OL}	I = +3 mA, MoI, Mo1, Mo2 pins			0.4	V
[Current Division Ratio (A • B)]						
2W1-2, W1-2, 1-2	Vref	θ = 1/8		100		%
2W1-2, W1-2	Vref	θ = 2/8		92		%
2W1-2	Vref	θ = 3/8		83		%
2W1-2, W1-2, 1-2	Vref	θ = 4/8		71		%
2W1-2	Vref	θ = 5/8		55		%
2W1-2, W1-2	Vref	θ = 6/8		40		%
2W1-2	Vref	θ = 7/8		21		%
2	Vref			100		%
PWM frequency	fc		37	47	57	kHz

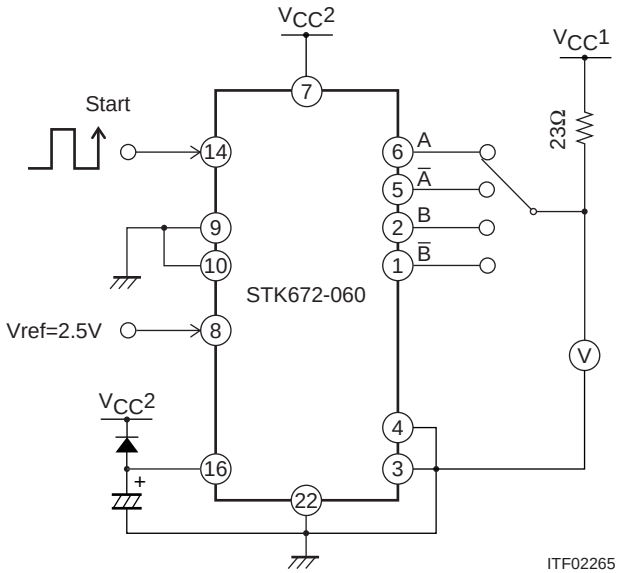
Notes: A constant voltage power supply must be used.
Design target values are shown for the current division ratios.

Block Diagram

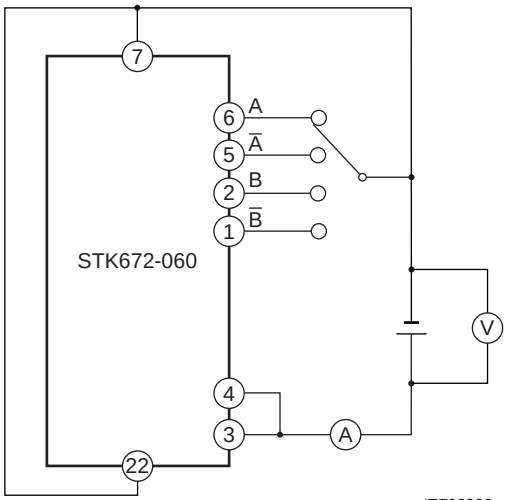


Test Circuit Diagrams

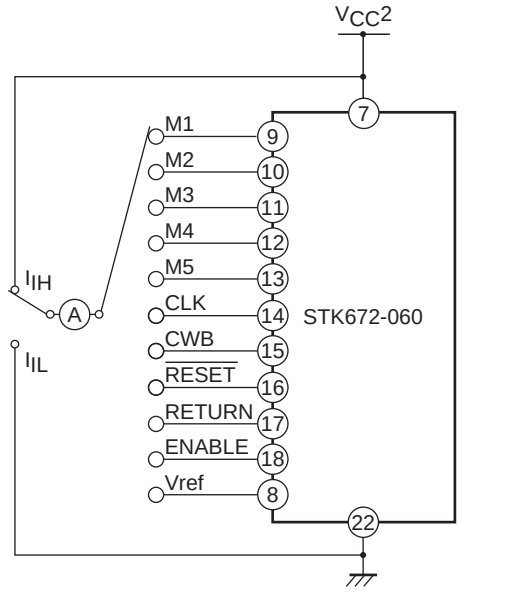
Vsat



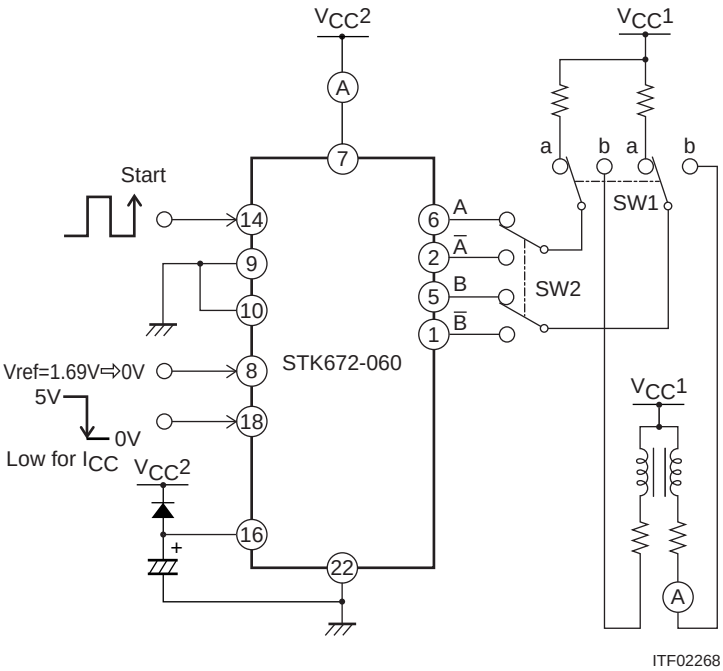
Vdf



I_{IH}, I_{IL}



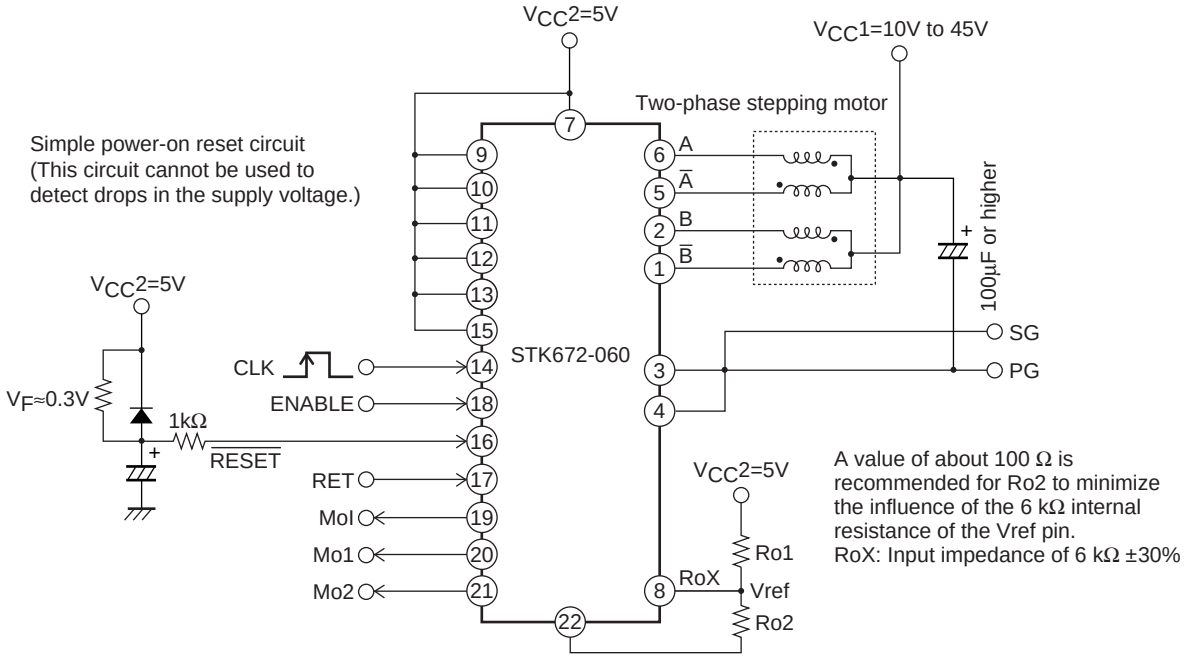
Ioave, Icc, fc



When measuring Ioave: Set switch SW1 to the b position, set Vref = 1.69 V
When measuring fc: Set switch SW1 to the a position, set Vref = 0 V
When measuring I_{CC}: Set ENABLE low.

Power-on reset

The application must perform a power-on reset operation when $V_{CC}2$ power is first applied to this hybrid IC.
Application circuit that used 2W1-2 phase excitation (microstepping operation) mode



Motor Current Setting Procedure

The motor current I_{OH} is set by the voltage on pin 8, Vref. The following formulas show the relationship between I_{OH} and Vref:

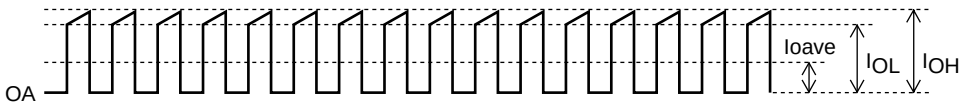
$RoX = (Ro2 \times 6\ k\Omega) \div (Ro2 + 6\ k\Omega)$.....(1)

$Vref = V_{CC}2 \times RoX \div (Ro1 + RoX)$.....(2)

$$I_{OH} = \frac{1}{K} \times \frac{Vref}{Rs}$$.....(3)

K: 7.66 (voltage divider ratio),
Rs: 0.22 Ω (This is the hybrid IC's internal current detection resistor. It has a tolerance of ±3%.)

Motor currents range from the setting current (0.05 to 0.1 A) due to the frequency of the duty cycle set by the oscillator to the current given in the allowable operating ranges (I_{OH} = 1.2 A).



Motor Current Waveform

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Function Table

M2	0	0	1	1	Phase switching CLK edge timing
M1 / M3	0	1	0	1	
1	2 phase excitation	1-2 phase excitation	W1-2 phase excitation	2W1-2 phase excitation	Rising edge only
0	1-2 phase excitation	W1-2 phase excitation	2W1-2 phase excitation	4W1-2 phase excitation	Both rising and falling edges

	Forward	Reverse
CWB	0	1

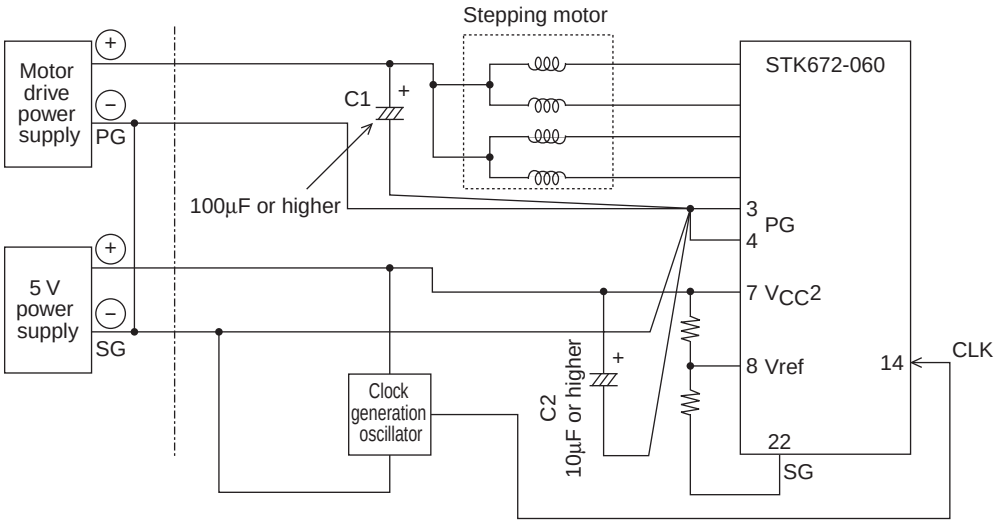
ENABLE	The motor current is cut when this pin is set to the low level.
$\overline{RESET}$	Active low

	A	$\overline{A}$	B	$\overline{B}$
Mo1	1	0	0	1
Mo2	0	0	1	1

Recommendations for PCB Designs

This hybrid IC has three ground pins: the PG pins (pins 3 and 4) and the SG pin (pin 22). These pins are connected internally.
Two power supplies are required: one power supply for motor drive and another for the hybrid IC 5 V control system. If there are problems with the ground connections for these power supplies, that can in turn cause the motor current waveform to become unstable, an increase in audible motor noise, or increased motor vibration. The ground lines must be designed appropriately.
This section describes two ground connection methods.

- When the grounds for the motor drive power supply and the hybrid IC 5 V power supply are connected close to the power supplies
  a) If PG and SG are shorted at the power supply side, connect only the PG line to pins 3 and 4 on the hybrid IC. Verify that voltage drops due to common line impedances do not occur. Note that $V_{CC}2$ is required to be within ±5% in the specifications.
  b) Connecting the Vref ground to pin 22 provides more stable current waveforms.
  c) For initial values, use 100 µF or higher for C1 and 10 µF or higher for C2.
  C1 must be located close to the hybrid IC and the capacitor ground line must be as short as possible.



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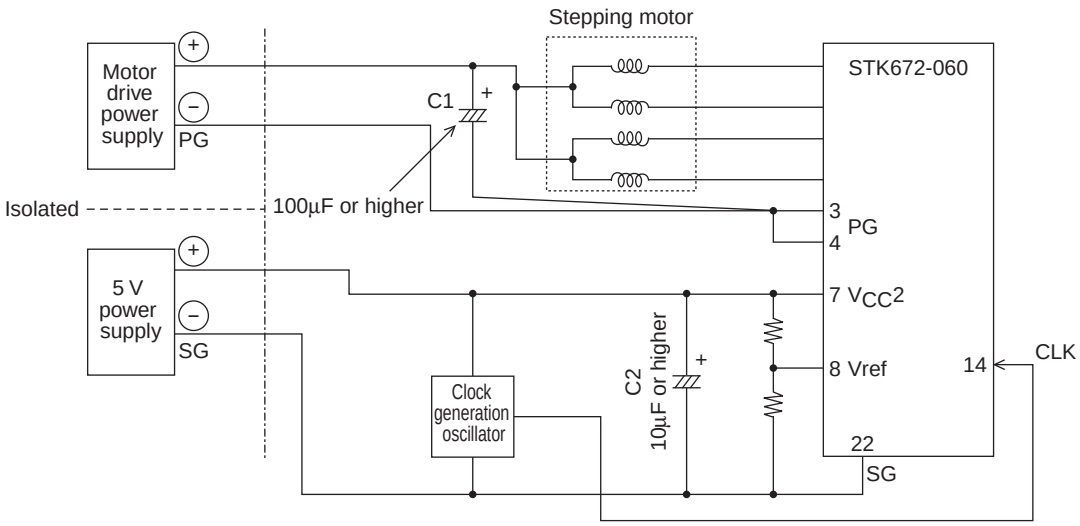
- When the grounds for the motor drive power supply and the hybrid IC 5 V power supply are separated
  a) Place the capacitor C1 (100 µF or higher) as close to the hybrid IC as possible. This capacitor's ground line must be as short as possible.
  Connect the capacitor C2 of an appropriate value if required. It's ground line must be as short as possible.



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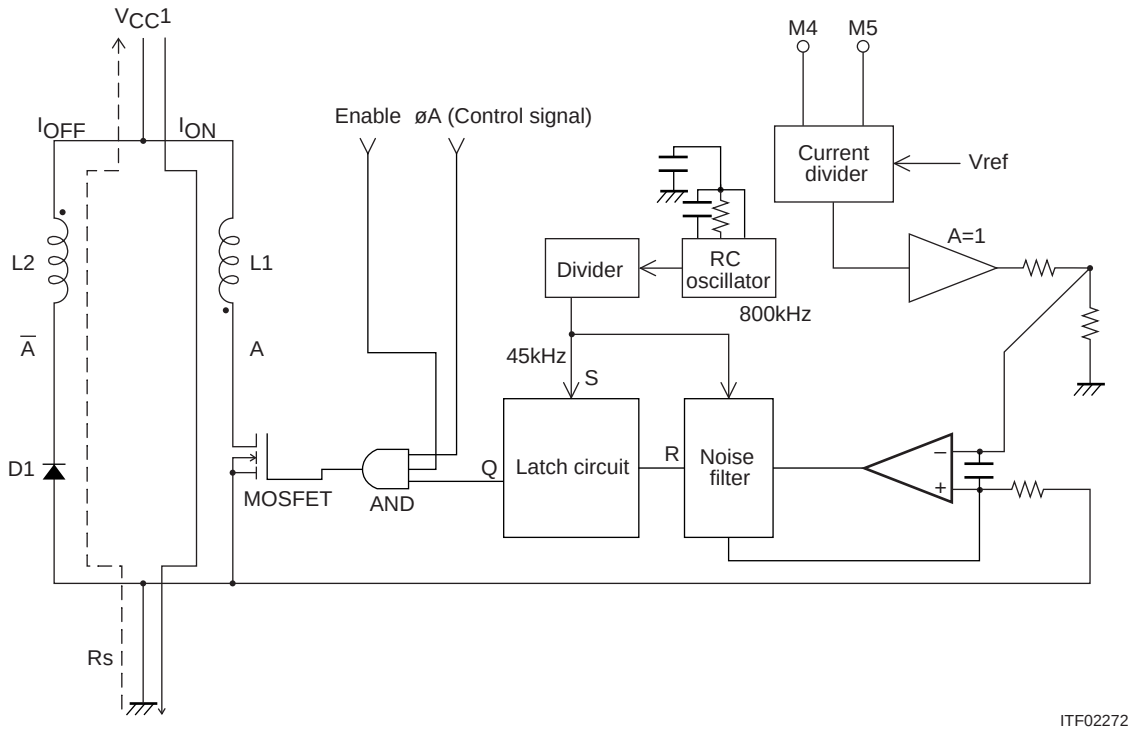
IC Operation

External Excitation Chopping Driver Block



Driver Block Basic Circuit Structure

Since this hybrid IC adopts an external excitation method, no external oscillator circuit is required.
If a high level is input on the øA line in the driver block basic circuit in the figure and the MOSFET is turned on, the comparator + input will go to the low level and the comparator output will go to the low level. Meanwhile, since the set signal is input during the PMW period, the Q output will go to the high level and the initial state of the MOSFET will be the on state.
The current I_{ON} that flows in the MOSFET will pass through L1 generating a potential difference across Rs. Then, when the Rs potential becomes the same as the Vref potential, the comparator output will invert, the reset signal will be generated, and the Q output will invert, into the low level. This turns the MOSFET off and the energy stored in L1 is induced in L2, and I_{OFF} is regenerated to the power supply. This state is maintained for the time that the set signal is input to the latch circuit.
The Q output is turned on and off repeatedly by the set and reset signals in this manner, which implements constant current control. The resistor and capacitor connected at the comparator input synchronize with the PWM period of the spike absorption circuit.
Because of the fixed period due to the external excitation method adopted and synchronized PWM system, this circuit can minimize hold noise generated when the motor position is locked.

Input Pin Description

Pin No.	Pin	Function	Pin circuit type
14	CLK	Phase switching clock	CMOS Schmitt trigger circuit with built-in pull-up resistor
15	CWB	Rotation direction setting (CW/CCW)	CMOS Schmitt trigger circuit with built-in pull-up resistor
17	RETURN	Forcible return to phase origin	CMOS Schmitt trigger circuit with built-in pull-up resistor
18	ENABLE	Output cutoff	CMOS Schmitt trigger circuit with built-in pull-up resistor
9, 10, 11	M1, M2, M3	Excitation mode setting	CMOS Schmitt trigger circuit with built-in pull-up resistor
12, 13	M4, M5	Vector locus setting	CMOS Schmitt trigger circuit with built-in pull-up resistor
16	$\overline{\text{RESET}}$	System reset	CMOS Schmitt trigger circuit with built-in pull-up resistor
8	Vref	Current value setting	Operational amplifier input

• Input Signal Functions and Timing

CLK (Phase switching clock)

Input frequency range: DC to 50 kHz

Minimum pulse width: 10 μs

Duty: 40 to 60% (The minimum pulse width takes precedence when M3 is high)

Pin circuit type: CMOS Schmitt trigger with built-in pull-up resistor (20 kΩ typical)

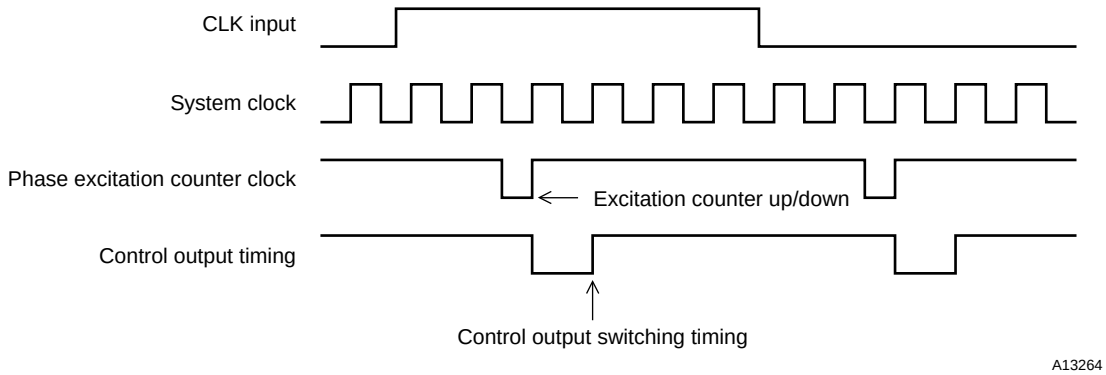
A multi-stage noise filter is built in.

Function

When M3 is high or open: The excited phase is advanced by one step on each rising edge of CLK signal.

When M3 is low: The phase is advanced 2 steps on the rising and falling edges of the CLK signal.

CLK Input Acquisition Timing (when M3 is low)



CWB (Rotation setting procedure)

Pin circuit type: CMOS Schmitt trigger with built-in pull-up resistor (20 kΩ typical)

Function

When CWB is low: Rotation in the clockwise direction.

When CWB is high: Rotation in the counterclockwise direction

Note: When M3 is low, the CWB input must not be changed within ±6.25 μs of a rising or falling edge on the CLK input.

RETURN (Forcible return to the origin point for the current phase)

Pin circuit type: CMOS Schmitt trigger with built-in pull-up resistor (20 kΩ typical)

Built-in noise filter

Note: The motor is forcibly moved to the origin point for the current phase by changing the input level on this pin from low to high. When unused, this pin must normallyr be left open or connected to the $V_{CC}2$.

ENABLE (On/off control of the A, $\overline{A}$, B, and $\overline{B}$ excitation drive outputs and selection of the internal operate or hold state of the hybrid IC itself)

Pin circuit type: CMOS Schmitt trigger with built-in pull-up resistor (20 kΩ typical)

Function

When ENABLE is high or open: Normal operating state

When ENABLE is low: The hybrid IC goes to the hold state, and the excitation drive output (motor current) is forcibly turned off (the output current is cut off). In this state, the hybrid IC system clock is stopped, and the hybrid IC is not affected by any changes in the state of the input pins other than the reset input.

M1, M2, and M3 (Excitation mode and CLK input edge timing selection)

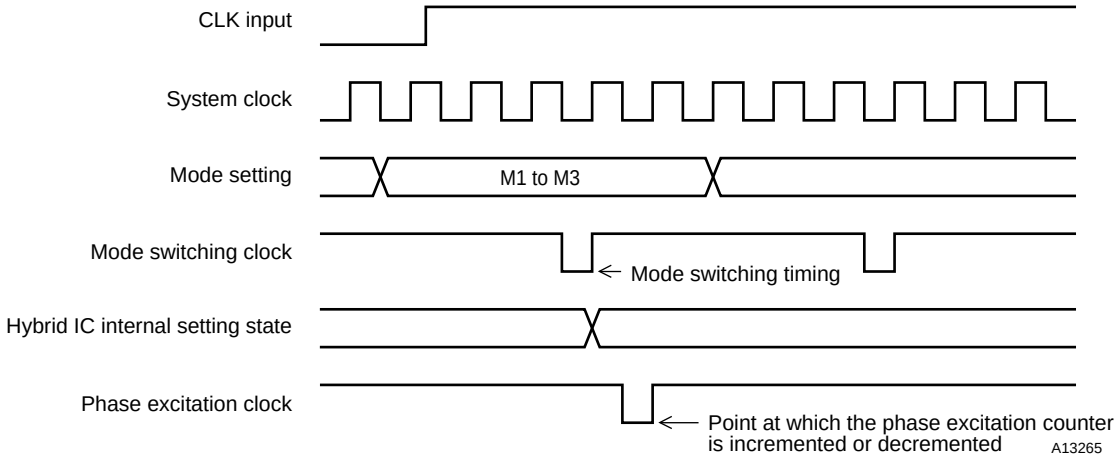
Pin circuit type: CMOS Schmitt trigger with built-in pull-up resistor (20 kΩ typical)

Function

M2	0	0	1	1	Phase switching CLK edge timing
M1 / M3	0	1	0	1	
1	2 phase excitation	1-2 phase excitation	W1-2 phase excitation	2W1-2 phase excitation	Rising edge only
0	1-2 phase excitation	W1-2 phase excitation	2W1-2 phase excitation	4W1-2 phase excitation	Both rising and falling edges

Timing when mode setting is enabled: Do not change the mode within ±5 μs of a CLK signal rising or falling edge.

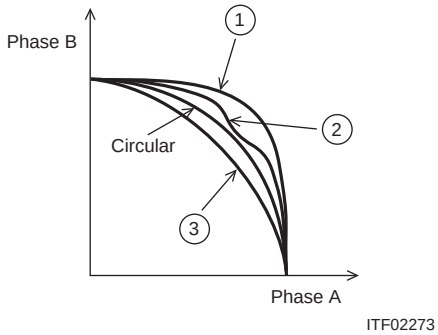
Mode Setting Acquisition Timing



M4 and M5 (Rotation vector locus setting for microstepping mode)

M4	1	0	1	0
M5	1	0	0	1
Mode	Circular	①	②	③

See the table on the following page for details on the current division ratio.



$\overline{\text{RESET}}$ (Resets the whole system)

Pin circuit type: CMOS Schmitt trigger with built-in pull-up resistor (20 kΩ typical)

Function: The circuit states are all set to their initial values by applying a low level (with a pulse width of 10 μs or longer) to the $\overline{\text{RESET}}$ pin. At this time, the A and $\overline{\text{B}}$ phases are set to their origin points, regardless of the excitation mode. The output current becomes about 71% after the reset is cleared.

Note: The Vref voltage is established by applying a reset after power is first applied. Applications must perform a power-on reset operation after the $V_{CC}2$ power is applied.

Vref (Sets the current value used as the reference for constant-current output)

Pin circuit type: Analog input circuit

Function: Applications can implement constant-current control of the motor excitation current at 100% of the rated current value by applying a voltage lower than the control system power supply voltage $V_{CC}2$ minus 2.5 V. This IC supports constant current control proportional to the Vref voltage with an upper limit of 2.5 V.

Output Pin Description

Pin No.	Pin	Function	Pin circuit type
19	MoI	Phase excitation origin point monitor	Standard CMOS output
20, 21	Mo1, Mo2	Phase excitation status monitor	Standard CMOS output

Output Signal Functions and Timings

A, $\overline{A}$, B, and $\overline{B}$ (Motor phase excitation outputs)

Function: In 4 phase and 2 phase excitation modes, an interval of about 3.75 μs (typical) is set up when the A and $\overline{A}$, and B and $\overline{B}$ output signals change their state.

MO1, MO2, and MOI (Motor phase excitation state monitoring)

Pin circuit type: Standard CMOS output

Function: These pins output the current phase excitation output state.

Phase coordinate	Phase A	Phase B	Phase $\overline{A}$	Phase $\overline{B}$
Mo1	1	0	0	1
Mo2	0	1	0	1

MoI outputs a 0 when the corresponding phase is at its origin, and a 1 at all other positions.

Current Division Ratios as Set by M3, M4, and M5 ····· Values provided for reference purposes

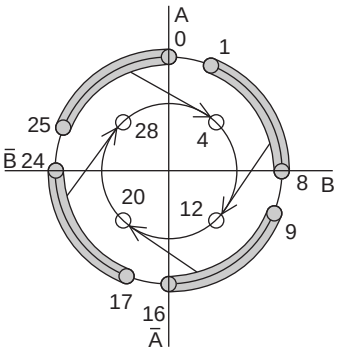
Mode			Circular	①	②	③	Unit	Number of steps	
Setting	M3 = 0	M3 = 1	M4 = 1	M4 = 0	M4 = 1	M4 = 0			
			M5 = 1	M5 = 0	M5 = 0	M5 = 1			
Current division ratio	4W1-2		15	16	16	15	%		1/16
		2W1-2	21	25	24	20		1/8	2/16
			31	34	33	28			3/16
		2W1-2	40	44	41	38		2/8	4/16
			47	50	49	44			5/16
		2W1-2	55	59	56	53		3/8	6/16
			63	67	63	60			7/16
		2W1-2	71	75	70	67		4/8	8/16
			76	81	76	73			9/16
		2W1-2	83	87	84	81		5/8	10/16
			87	92	88	84			11/16
		2W1-2	92	95	95	91		6/8	12/16
			96	98	98	93			13/16
		2W1-2	100	100	100	100		7/8	14/16

Load conditions: $V_{CC}1$ = 24 V, $V_{CC}2$ = 5 V, R/L = 3.5 Ω/3.8 mH

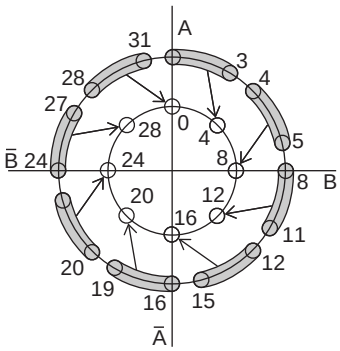
Phase States at Excitation Switching

Excitation Phases Before and After Switching Excitation Modes <Clockwise direction>

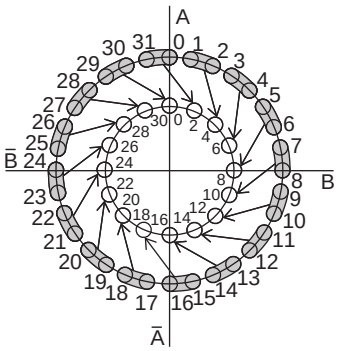
2W1-2 phase → 2 phase



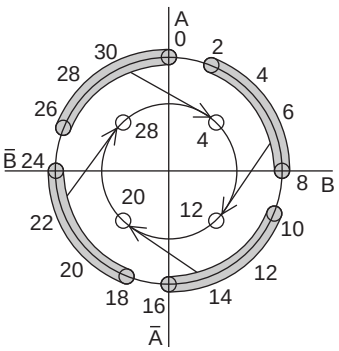
2W1-2 phase → 1-2 phase



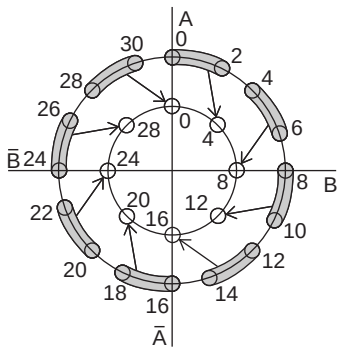
2W1-2 phase → W1-2 phase



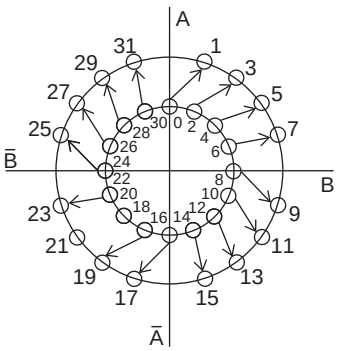
W1-2 phase → 2 phase



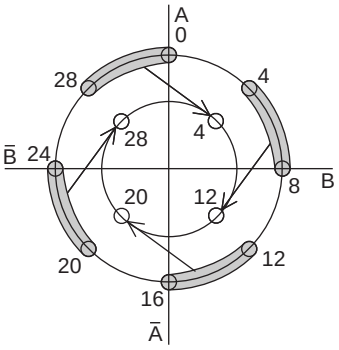
W1-2 phase → 1-2 phase



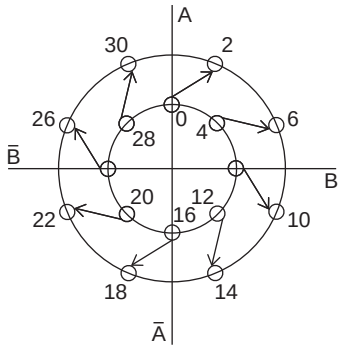
W1-2 phase → 2W1-2 phase



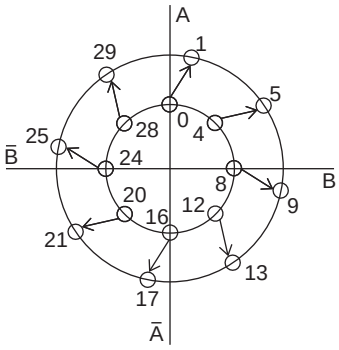
1-2 phase → 2 phase



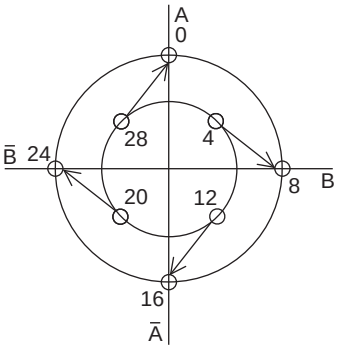
1-2 phase → W1-2 phase



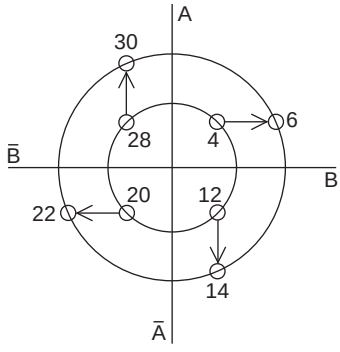
1-2 phase → 2W1-2 phase



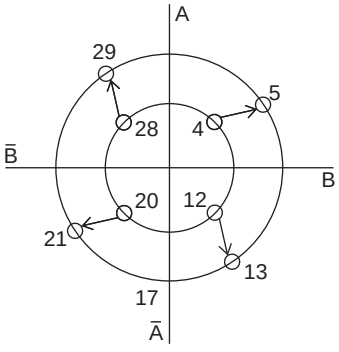
2 phase → 1-2 phase



2 phase → W1-2 phase



2 phase → 2W1-2 phase



Excitation phase developed by the first CLK internal pulse after the change in the excitation mode setting with M1 and M2

Excitation phase immediately prior to the excitation mode setting

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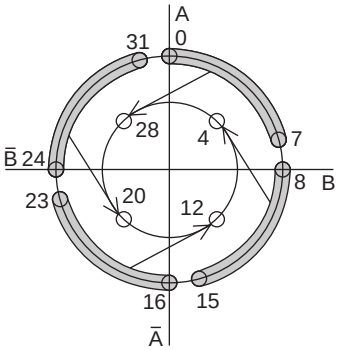
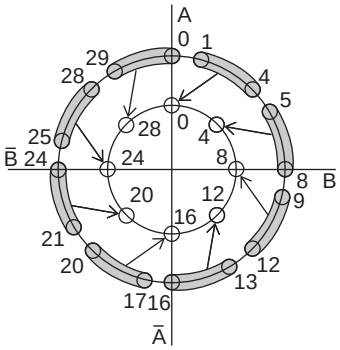
Excitation Phases Before and After Switching Excitation Modes <Clockwise direction>

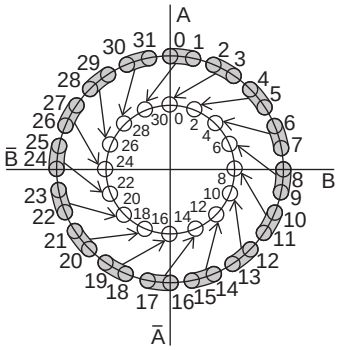
2W1-2 phase → 2 phase



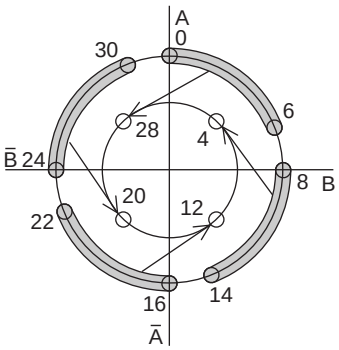
2W1-2 phase → 1-2 phase



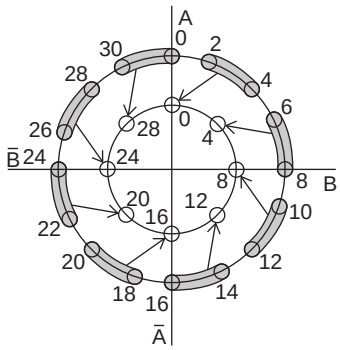
2W1-2 phase → W1-2 phase



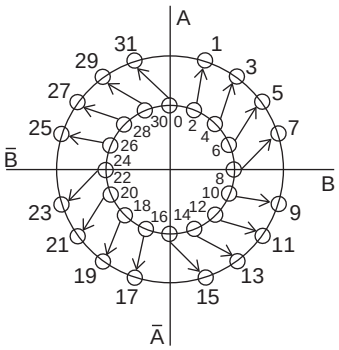
W1-2 phase → 2 phase



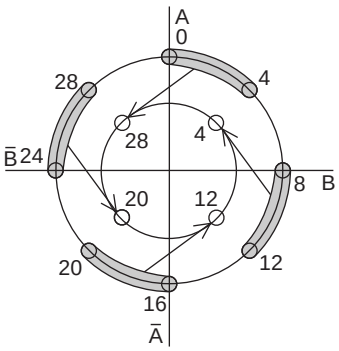
W1-2 phase → 1-2 phase



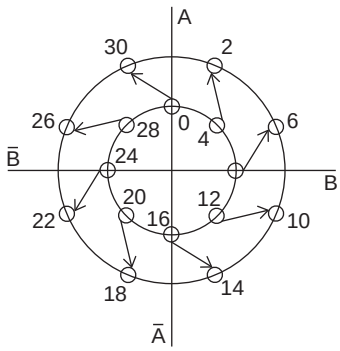
W1-2 phase → 2W1-2 phase



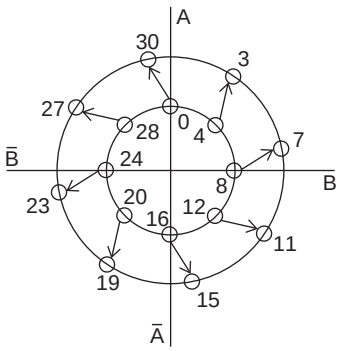
1-2 phase → 2 phase



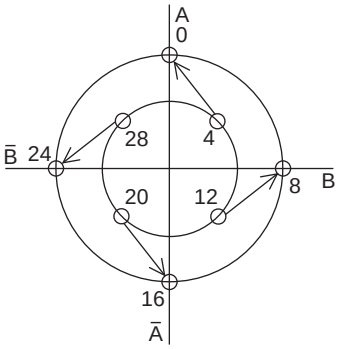
1-2 phase → W1-2 phase



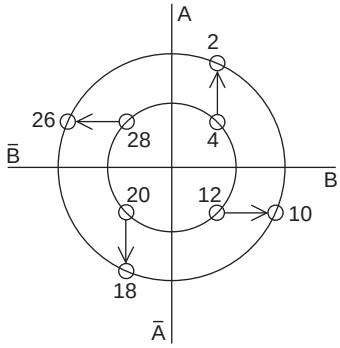
1-2 phase → 2W1-2 phase



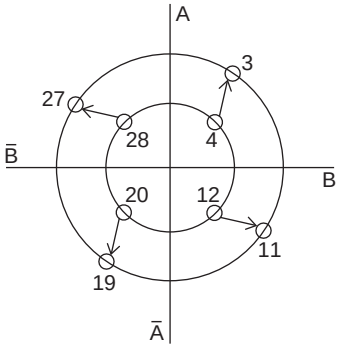
2 phase → 1-2 phase



2 phase → W1-2 phase



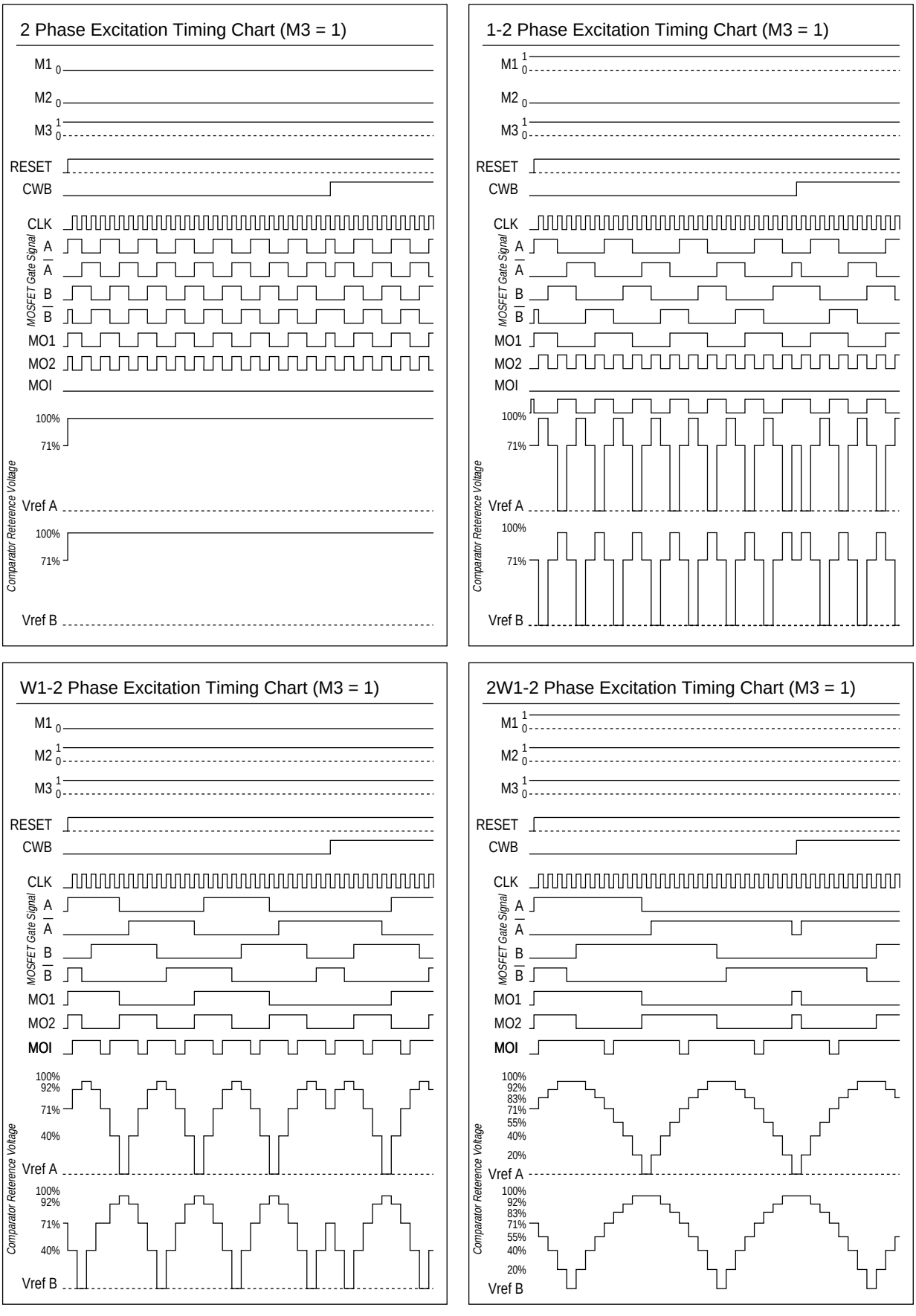
2 phase → 2W1-2 phase



A13267

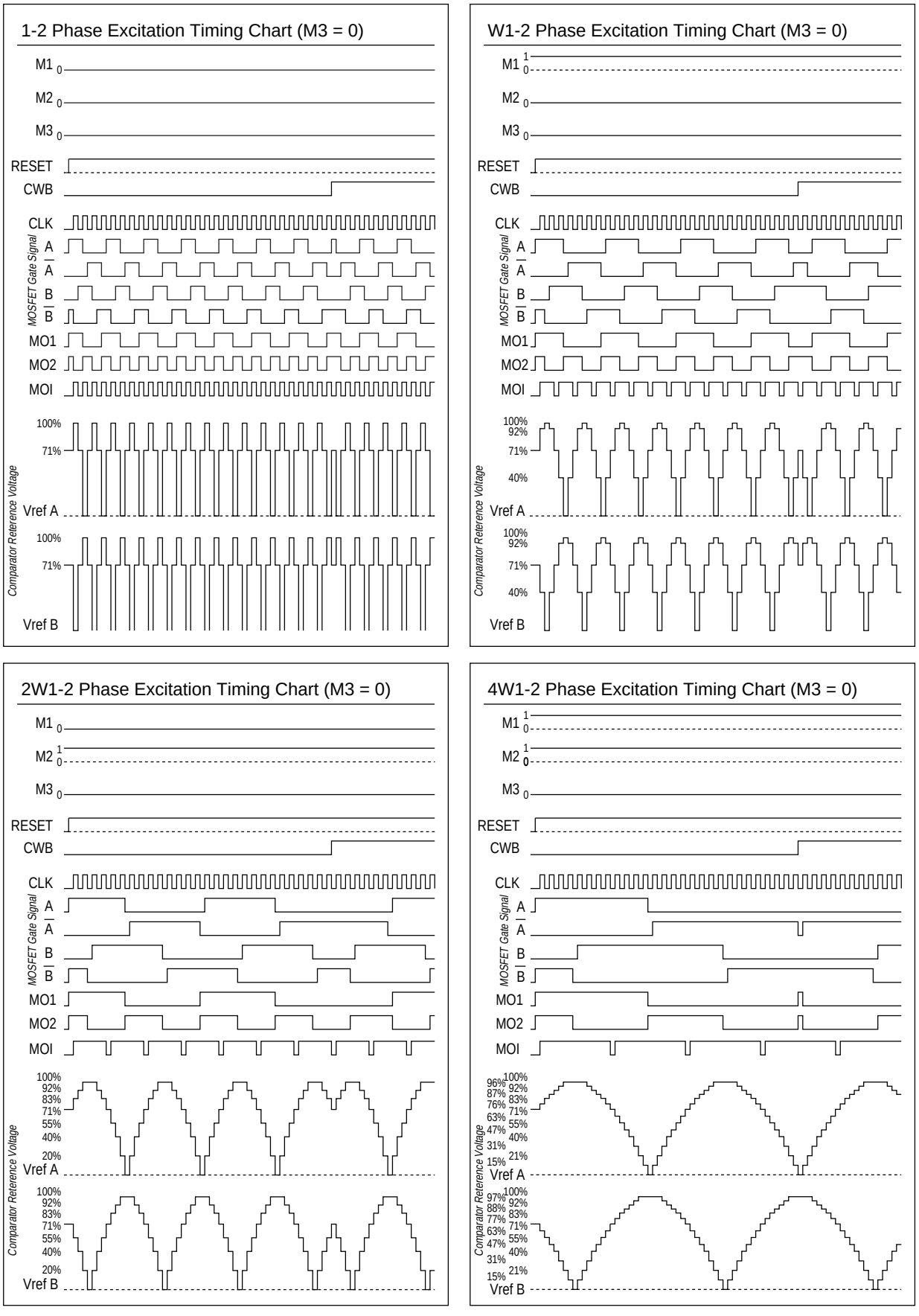
Excitation Time and Timing Charts

CLK Rising Edge Operation



ITF02274

CLK Rising and Falling Edge Operation



ITF02275

Thermal Design

<Hybrid IC Internal Average Power Dissipation, Pd>

The devices with the largest average power dissipation levels in this hybrid IC are the current control devices, the regenerative current diodes, and the current detection resistor. Since sine wave drive is used, the average power dissipation associated with microstepping drive can be approximated by applying a waveform ratio (0.64 in this case) to square wave power dissipation in 2-phase excitation.

The power dissipation levels for the available excitation modes are listed below.

2 phase excitation $$Pd_{2EX} = (Vsat + Vdf) \cdot \frac{fclock}{2} \cdot I_{OH} \cdot t2 + \frac{I_{OH} \cdot fclock}{2} \cdot (Vsat \cdot t1 + Vdf \cdot t3)$$

1-2 phase excitation $$Pd_{1\text{-}2EX} = 0.64 \cdot \{(Vsat + Vdf) \cdot \frac{fclock}{4} \cdot I_{OH} \cdot t2 + \frac{I_{OH} \cdot fclock}{4} \cdot (Vsat \cdot t1 + Vdf \cdot t3)\}$$

W1-2 phase excitation $$Pd_{W1\text{-}2EX} = 0.64 \cdot \{(Vsat + Vdf) \cdot \frac{fclock}{8} \cdot I_{OH} \cdot t2 + \frac{I_{OH} \cdot fclock}{8} \cdot (Vsat \cdot t1 + Vdf \cdot t3)\}$$

2W1-2 phase excitation $$Pd_{2W1\text{-}2EX} = 0.64 \cdot \{(Vsat + Vdf) \cdot \frac{fclock}{16} \cdot I_{OH} \cdot t2 + \frac{I_{OH} \cdot fclock}{16} \cdot (Vsat \cdot t1 + Vdf \cdot t3)\}$$

4W1-2 phase excitation $$Pd_{4W1\text{-}2EX} = 0.64 \cdot \{(Vsat + Vdf) \cdot \frac{fclock}{16} \cdot I_{OH} \cdot t2 + \frac{I_{OH} \cdot fclock}{16} \cdot (Vsat \cdot t1 + Vdf \cdot t3)\}$$

The values of t1 and t3 can be derived from the same formula for each excitation mode

$$t1 = \frac{-L}{R + 0.7} \cdot \ell\, n\,(1 - \frac{R + 0.7}{V_{CC}1} \cdot I_{OH}) \qquad t3 = \frac{-L}{R} \cdot \ell\, n\,(\frac{V_{CC}1 + 0.7}{I_{OH} \cdot R + V_{CC}1 + 0.7})$$

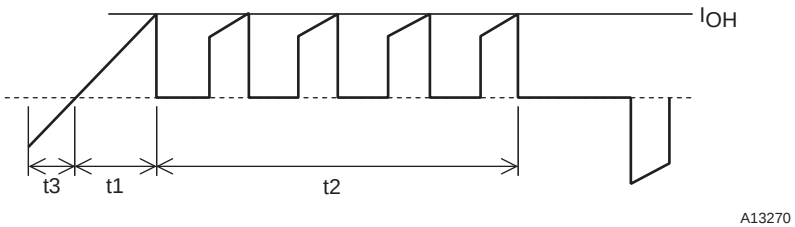
The formula for t2 differs for the excitation modes.

2 phase excitation $$t2 = \frac{2}{fclock} - (t1 + t3)$$

1-2 phase excitation $$t2 = \frac{3}{fclock} - t1$$

W1-2 phase excitation $$t2 = \frac{7}{fclock} - t1$$

2W1-2 phase excitation
4W1-2 phase excitation $$t2 = \frac{15}{fclock} - t1$$



A13270

Motor Phase Current Model (2 phase excitation)

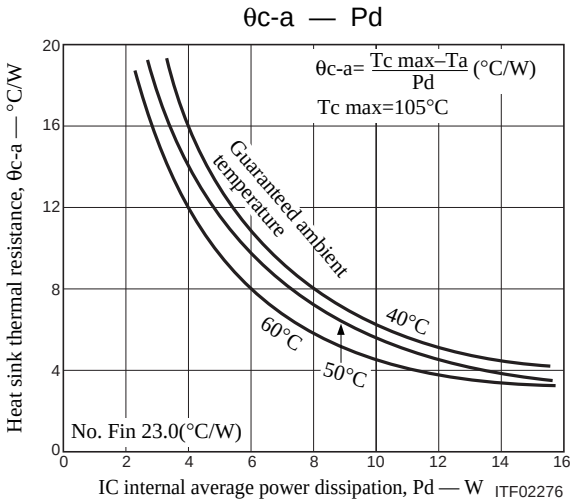
fclock: The CLK pin input frequency (Hz)
Vsat: The voltage drop (V) across the power MOSFET and the current detection resistor
Vdf: The voltage drop (V) across the diode and the current detection resistor
I_{OH}: Phase current peak-to-peak value
t1: Phase current rise time (s)
t2: Constant-current operating time (s)
t3: Phase switchover current regeneration time (s)
$V_{CC}1$: Supply voltage applied to the motor (V)
L: Motor inductance (H)
R: Motor winding resistance (Ω)

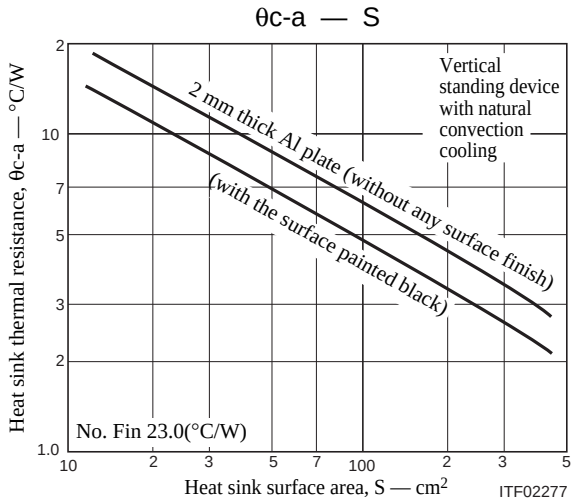
<Determining the Heat Sink Size for this Hybrid IC>
First, we determine the heat sink thermal resistance θc-a from the average power dissipation determined in the previous section.

$$\theta c\text{-}a = \frac{Tc\ max - Ta}{Pd_{EX}}\ [°C/W]$$

Tc max: Hybrid IC substrate temperature (°C)
Ta: End product internal temperature (°C)
Pd_{EX}: Hybrid IC internal average power dissipation (W)

After determining θc-a from the above formula, determine the size S (cm^2) of the heat sink from the following graphs.
The ambient temperature depends strongly on the ventilation conditions within the end product. Thus the size of the heat sink must be checked carefully with the IC installed in the end product so that the back surface (the aluminum surface) of this hybrid IC never exceeds Tcmax (105°C) under all possible operating conditions.





Next, with the hybrid IC used without fins, we determine the allowable hybrid IC average internal power dissipation from H-IC substrate thermal resistance θc-a = 23°C/W.

Assuming that Tcmax is 105°C at an ambient temperature of 50°C: $Pd_{EX} = \frac{105 - 50}{23} = 2.3$ W

With an ambient temperature of 40°C and a Tcmax of 105°C: $Pd_{EX} = \frac{105 - 40}{23} = 2.8$ W

This device can be used under all operating conditions without fins provided that all dissipation values are not exceeded. (See the ΔTc - Pd curve.)

<Hybrid IC Internal Power Device (MOSFET) Junction Temperature Calculation>
Here we determine the junction temperature Tj for each device from the power dissipation for each transistor, Pds and θj-c.

$$Tj = Tc + \theta j\text{-}c \times Pds\ (°C)$$

Here, to determine Pds, we calculate Pd_{EX} separately for each excitation mode and determine the power dissipation Pds for each device.

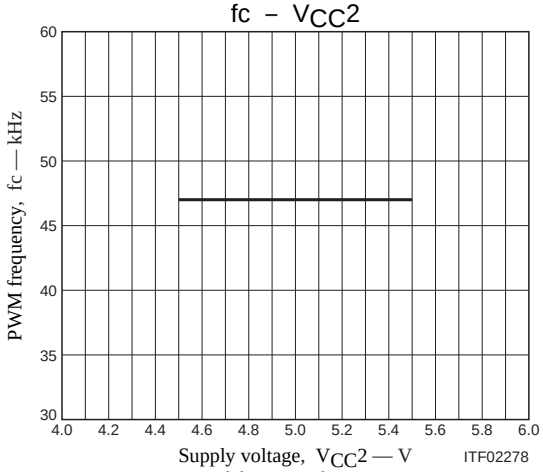
$$Pds = Pd/4$$

Since the power dissipation in the current detection resistor is included in the average power dissipation, here we consider that voltage drop to determine the power dissipation.

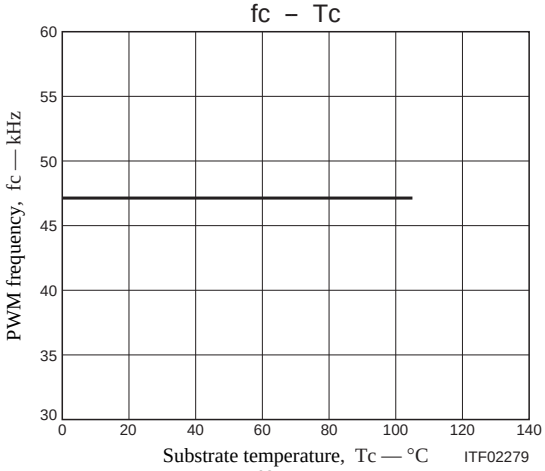
$$Vsat = I_{OH} \cdot Ron + I_{OH} \cdot Rs$$
$$Vdf = Vdf + I_{OH} \cdot Rs$$

The steady-state thermal resistance of the power MOSFET is 18 °C/W.

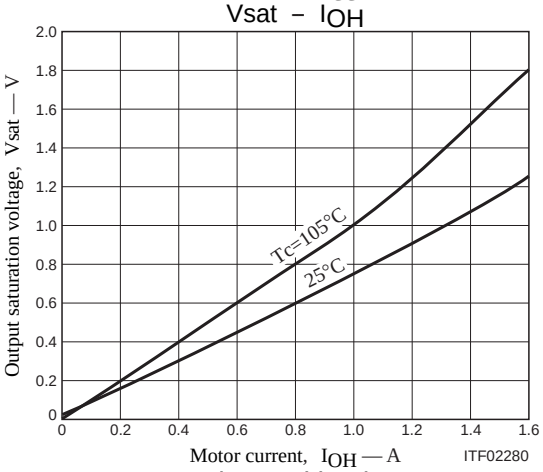
fc – $V_{CC}2$



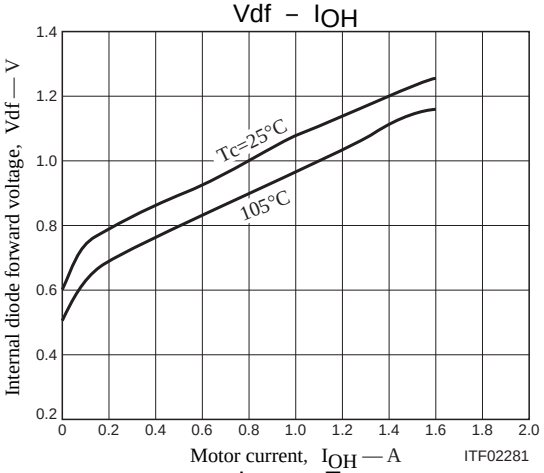
fc – Tc



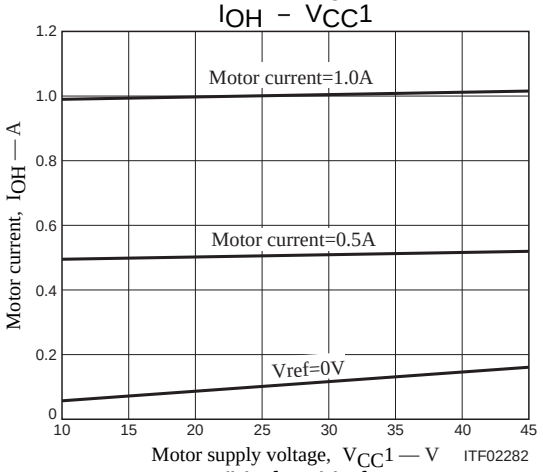
Vsat – I_{OH}



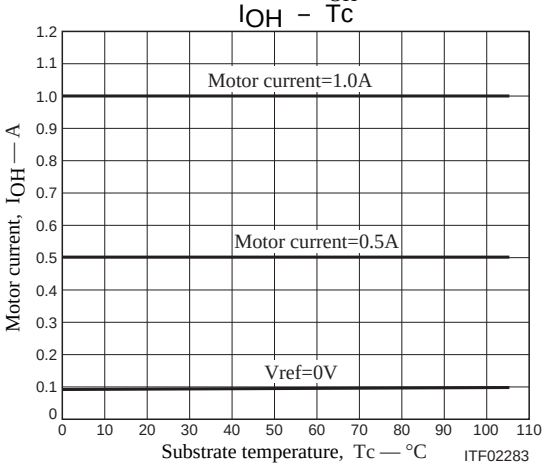
Vdf – I_{OH}



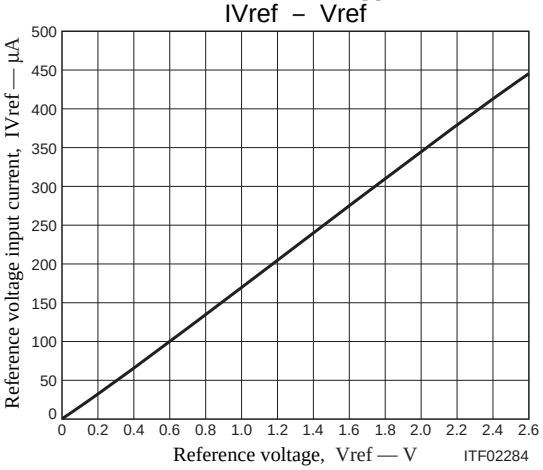
I_{OH} – $V_{CC}1$



I_{OH} – Tc



IVref – Vref



IVref – Tc