Ordering number:ENN1773

Thick Film Hybrid IC

STK7560 Series

Chopper Type Parallel 2-Output Voltage Regulators

Applications

- Voltage regulator for printers, electronic typewriters, XY plotters.
- Voltage regulator for MSX personal computers, floppy disk drive, computer terminals, portable VTRs.

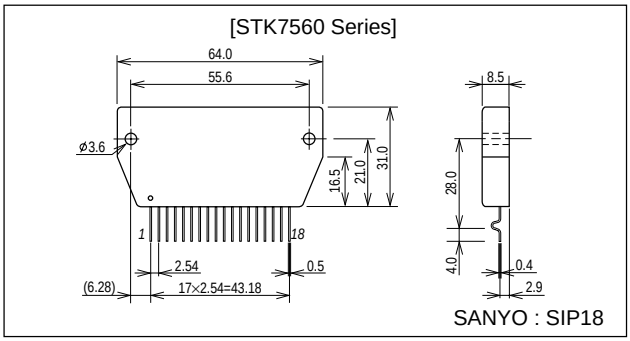
Features

- ICs having 2 outputs for microcomputer power supply (5V) and motor drive power supply (12, 15, 24, 36V) and being capable of delivering 2 regulated outputs from 1 rectifier.
- Good efficiency due to chopper type and no beat trouble due to fixed oscillation type oscillator common to 2 outputs.
- Independent overcurrent protectors for 2 outputs (Foldback characteristics).
- Output 2 (drive power supply) can be turned ON/OFF by external signal. Two outputs can be also turned ON/OFF simultaneously by an external circuit connected (Refer to Sample Application Circuit).
- High-precision setting of output voltage, elminating the need to use a variable resistor for adjustment.
- Input/output Gnd lines are united into one, facilatating combination with other nagative power supply.
- A negative voltage regulator (–5V, –12V, etc.) can be connected externally (Refer to Sample Application Circuit).
- Output voltage/output current are provided in series.

Package Dimensions

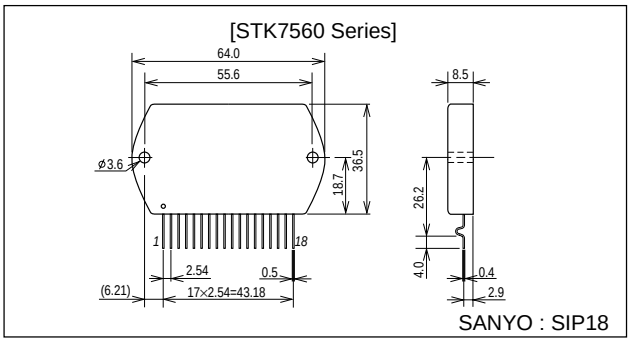
unit:mm

4049



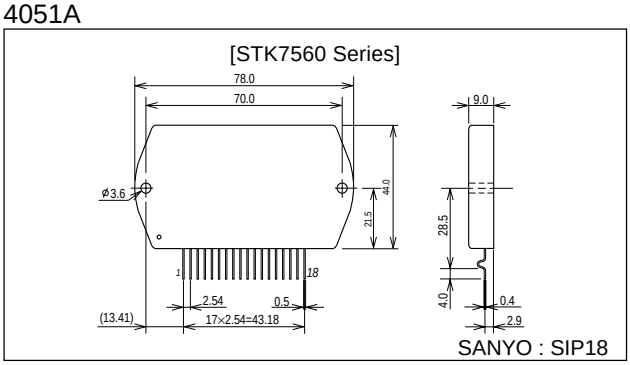
unit:mm

4050



unit:mm

4051A



SANYO Electric Co.,Ltd. Semiconductor Company

TOKYO OFFICE Tokyo Bldg., 1-10, 1 Chome, Ueno, Taito-ku, TOKYO, 110-8534 JAPAN

Case Outline

Type No.	Case Outline	Type No.	Case Outline	Type No.	Case Outline	Type No.	Case Outline
STK7561A	No.4049	STK7562A	No.4049	STK7563A	No.4049	*STK7565A	No.4049
STK7561F	No.4050	STK7562F	No.4050	STK7563F	No.4050	*STK7565F	No.4050
STK7561G	No.4050	STK7562G	No.4050	STK7563G	No.4050		
STK7561J	No.4050	STK7562J	No.4050	STK7563J	No.4050		
STK7561L	No.4051	STK7562L	No.4051	STK7563L	No.4051		

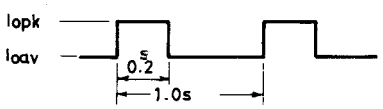
* New product

Specifications

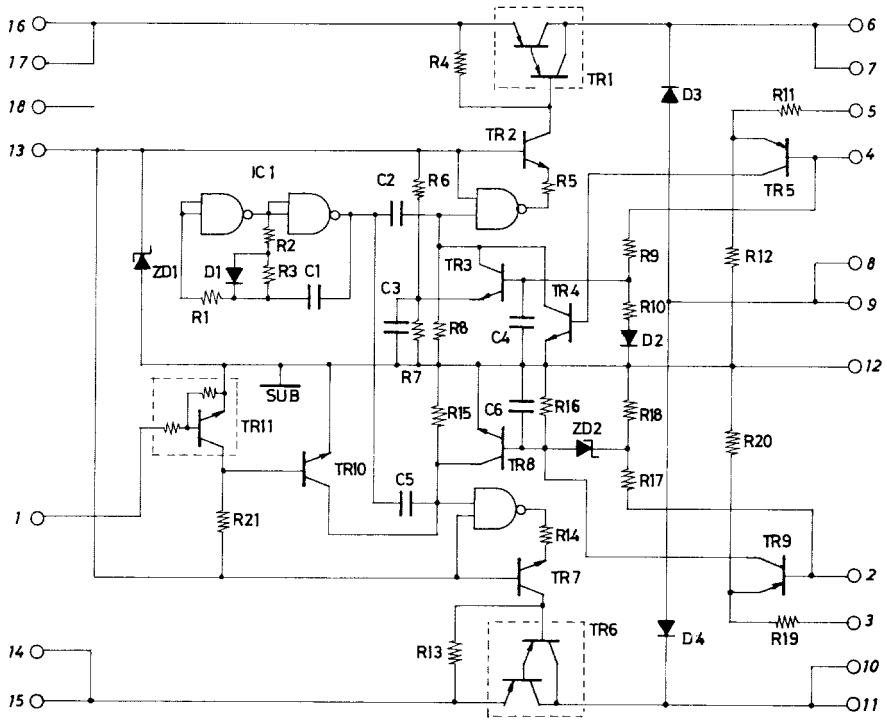
Main Maximum Ratings and Operating Characteistics at Ta = 25˚C

Type No.	Limits			OUTPUT			OUTPUT		
	Vin max	Tc max	Tstg	Vout	Iout	Iop	Vout	Iout	Iop
	(V dc)	(˚C)	(˚C)	(V)	(A)	(A)	(V)	(A)	(A)
STK7561A	50 (25 rating)	105	–30 to +105	5V±0.1V	2	2.4	12V±0.2V	2	4
STK7561F					3	3.6		3	6
STK7561G					3	3.6		5	10
STK7561J					5	6.0		2	4
STK7561L					5	6.0		5	10
STK7562A	50 (30 rating)	105	–30 to +105	5V±0.1V	2	2.4	15V±0.3V	2	4
STK7562F					3	3.6		3	6
STK7562G					3	3.6		5	10
STK7562J					5	6.0		2	4
STK7562L					5	6.0		5	10
STK7563A	50 (35 rating)	105	–30 to +105	5V±0.1V	2	2.4	24V±0.4V	2	4
STK7563F					3	3.6		3	6
STK7563G					3	3.6		5	10
STK7563J					5	6.0		2	4
STK7563L					5	6.0		5	10
STK7565A	80 (45 rating)	105	–30 to +105	5V±0.1V	2	2.4	36V±0.6V	2	4
STK7565F					3	3.6		3	6

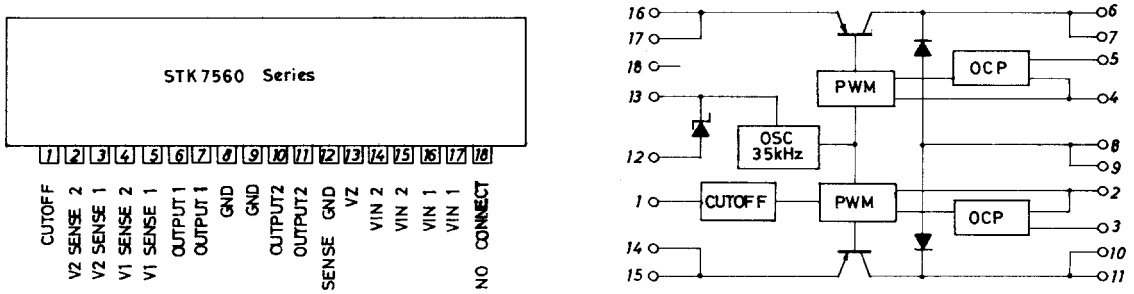
(Note) 1 Output 2 cutoff (pin 1 input) : OUTPUT 2 cutoff at 1V or less, OUTPUT 2 ON at 3V or greater.
2 The peak current value of OUTPUT 1 (5V) is set to 120% of the rating.
3 The peak current value of OUTPUT 2 (12V, 15V, 24V, 36V) is set to 200% of the rating considering the motor driving mode.
4 The secondary winding provided in the 5V choke coil makes OUTPUT 3 (–5V, 12V, –15V, 0.3A) available.
5 Peak current setting time.



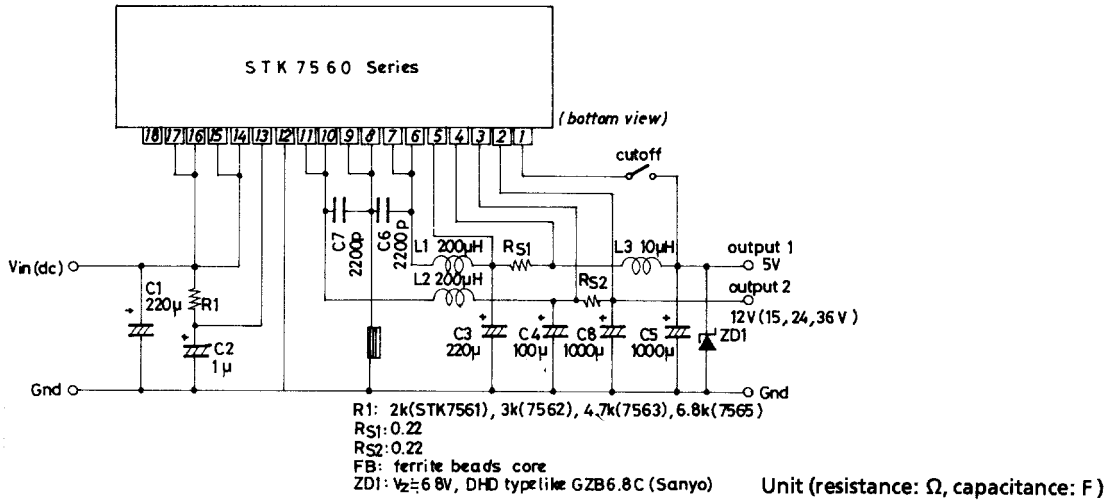
Equivalent Circuit



Equivalent Circuit Block Diagram and Pin Assignment



Sample Application Circuit 1 : Standard peripheral circuit

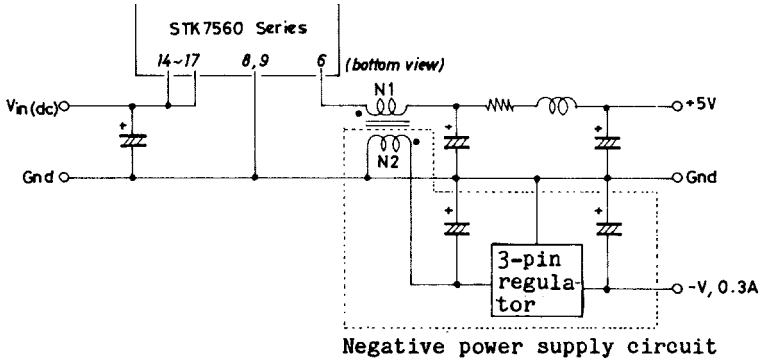


Note 1 The N. C pin (pin 18) must not be used as a relay pin for other line, pin.

2 Pins connected inside the IC (6-7, 8-9, 10-11, 14-15, 16-17) must be also connected on the printed circuit board.

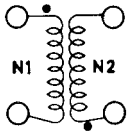
Sample Application Circuit 2 : 3 Outpus including a nagative output

The secondary winding provided in the 5V choke coil provides 2 functions of choke coil and transformer, eliminating the need to use a center tap on the input transformer to make a negative power supply available. The 5V output needs a load of approximately 0.5A.



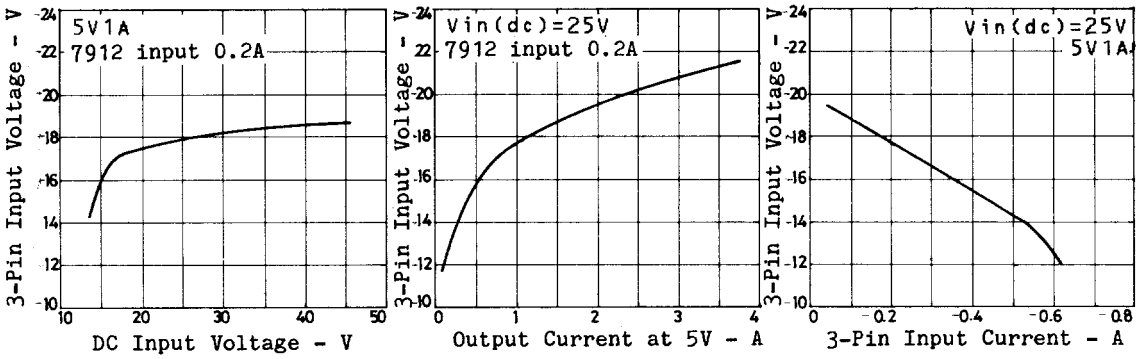
Negative power supply circuit

Sample 5V choke coil (for –12V output)

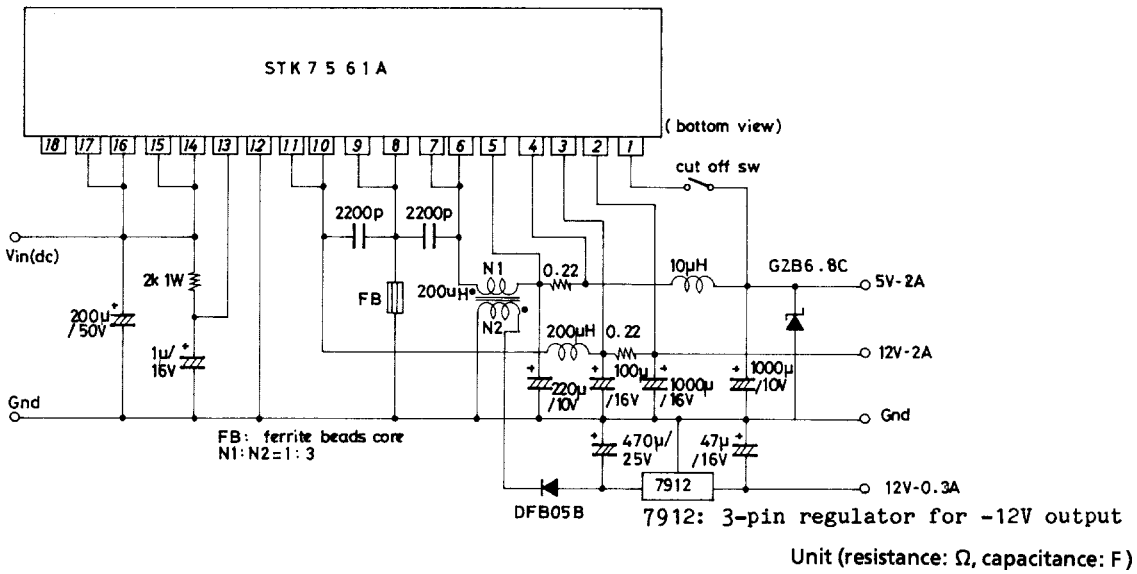


		A, F, or G type	J type
Ferrite core		EI-26	EI-30
Gap		0.5mm	0.5mmt×2
N1	No. of turns	40T	35
	Wire dia	0.6mm	0.8mm
N2	No. of turns	12T	10T
	Wire dia	0.3mm	0.3mm

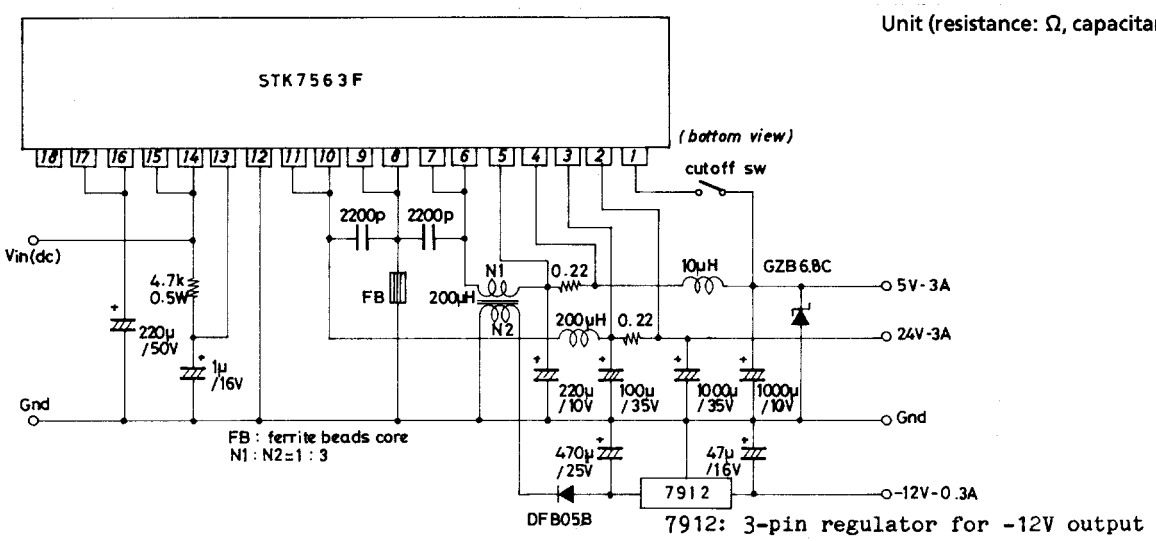
Sample data of 3-pin regulator input voltage (coil output voltage)/A, F, or G type



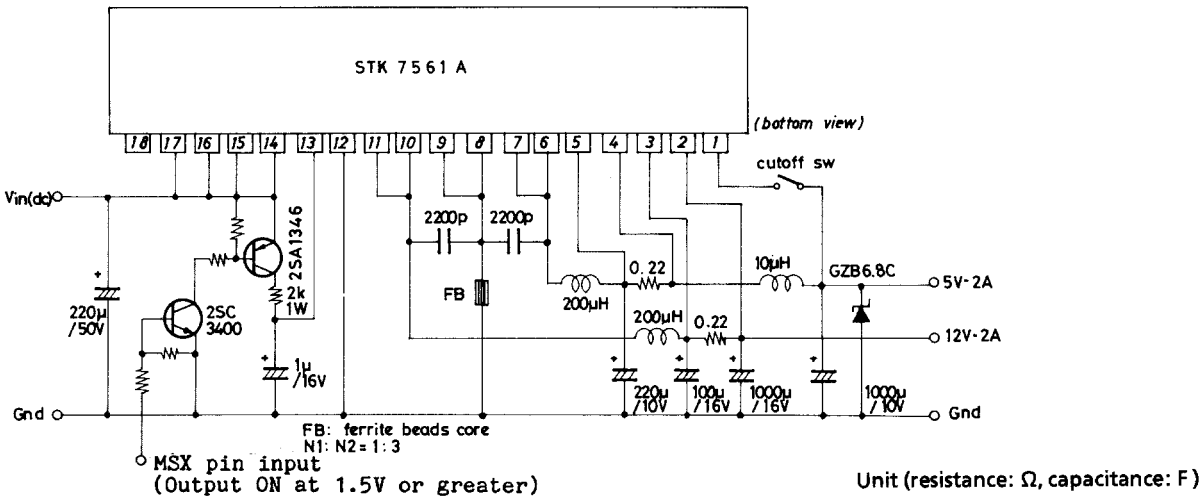
Sample Application Circuit 3 : STK7561A : 3 outputs of 5V, 12V, –12V



Sample Application Circuit 4 : STK7563F : 3 outputs of 5V, 24V, –12V



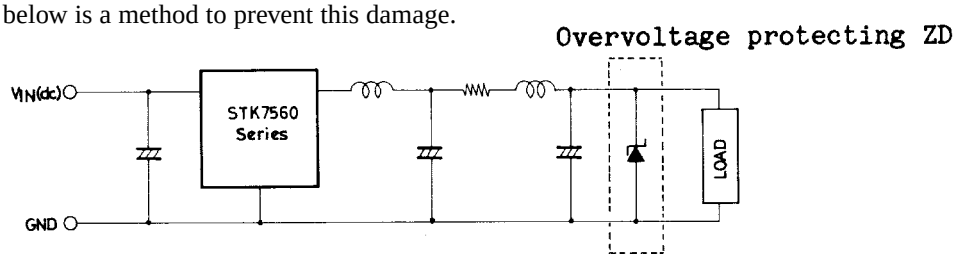
Sample Application Circuit 5 : STK7561A : Power supply for MSX personal computer, 2-output simultaneous ON/OFF



Sample Overvoltage Protector

Overcurrent may cause great damege. Particulary, the circuit connected to microcomputer power supply (5V) may be damaged.

Shown below is a method to prevent this damage.



Connect a zener diode in parallel with the load. Use a DHD (double heat sink) type zener diode whose zener voltage is 1 to 2V higher than supply voltage (5V).

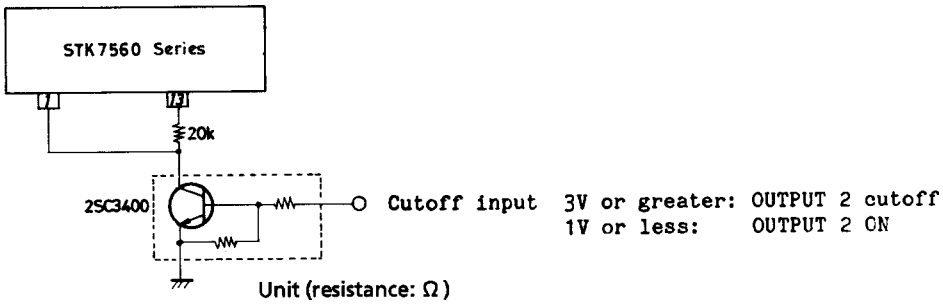
Overvoltage exceeding the zener voltage is limited by the zener diode.

With no current limiting rersistor connected, overcurrent flows in the zener diode.

Then, zener diode is shorted, thus protecting the load.

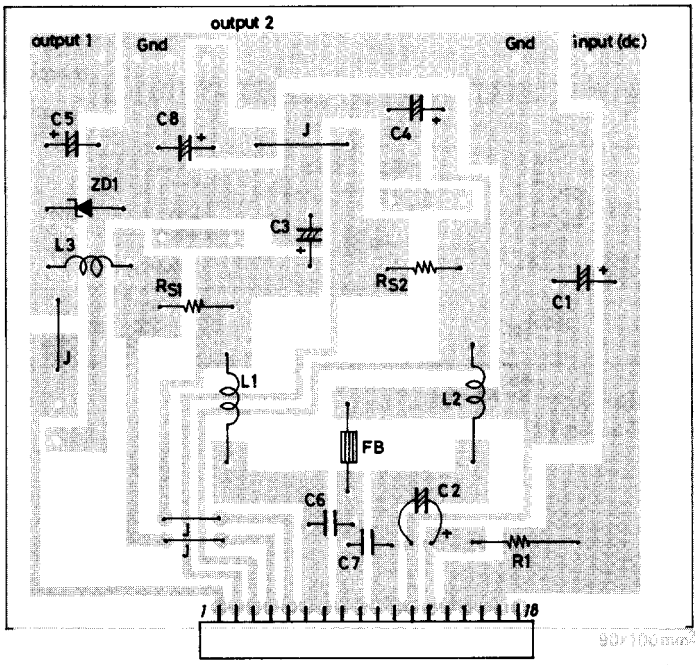
'High active' setting of cutoff input

'Low active' setting of cutoff input can be changed to 'High active' setting as shown below.



Sample Printed Circuit Pattern

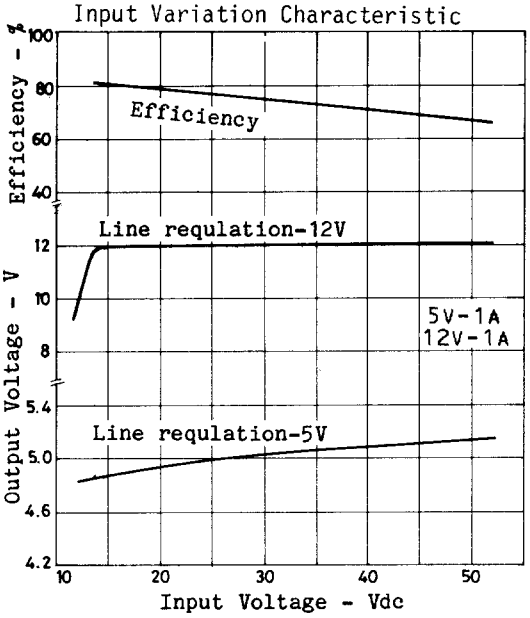
Standard peripheral circuit for Sample Application Circuit 1 (Cu-foiled area)



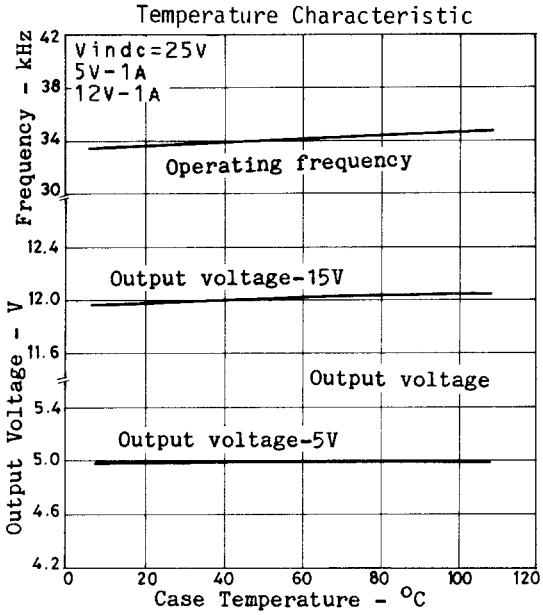
Precautions	Resons
· Make the large current-carrying lines thicker and shorter.	→ To minimize voltage loss on the pattern
· Please high input capacitor C1 close to the input pin of the IC.	→ To minimize input ripple.
· Place switching spike-reducing C6, C7 close to the IC pins.	→ To reduce switching spike more effectively.
· Connect GND of ferrite bead core to GND of input capacitor C1 to minimize the core, C1-related pattern loop area.	→ To reduce switching spike more effectively.
· Connect V SENSE GND (pin 12) to GND of current line near the load.	→ To impro ve load r egulation c haracteristic of output voltage.
· Connect GND of output capacitors C3, C4, C5, C8 near the load not to oppose current flow.	→ To improve ripple characteristic.
· Connect pins connected inside the IC (pins 6, 7, etc.) also on the printed circuit board.	→ To provent current from concentrating on pin.
· Do not use NC (pin 18) as a relay pin for otherline, pin.	

STK7561 Characteristics

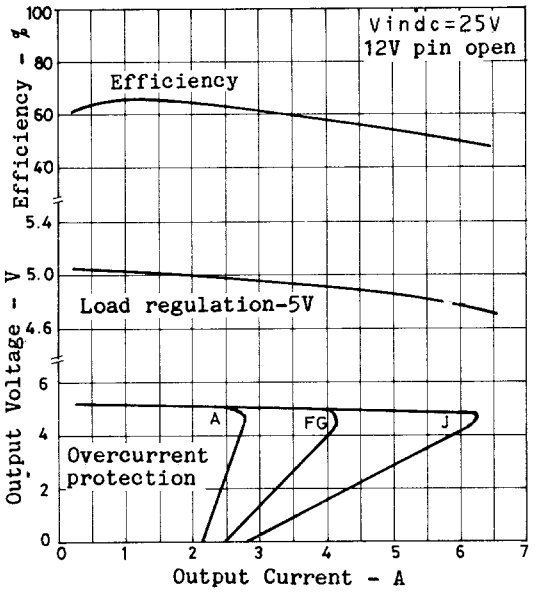
Input Variation Characteristic



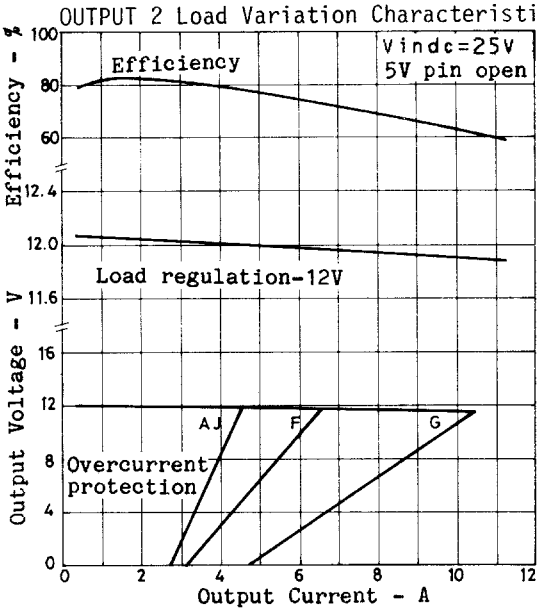
Temperature Characteristic



OUTPUT 1 Load Variation Characteristic

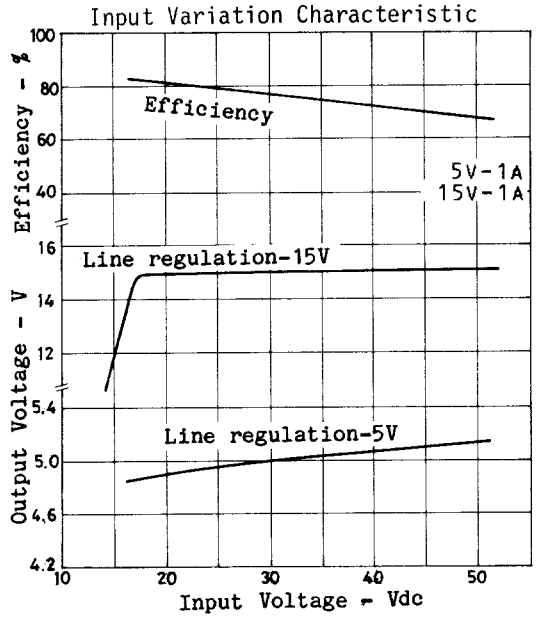


OUTPUT 2 Load Variation Characteristic

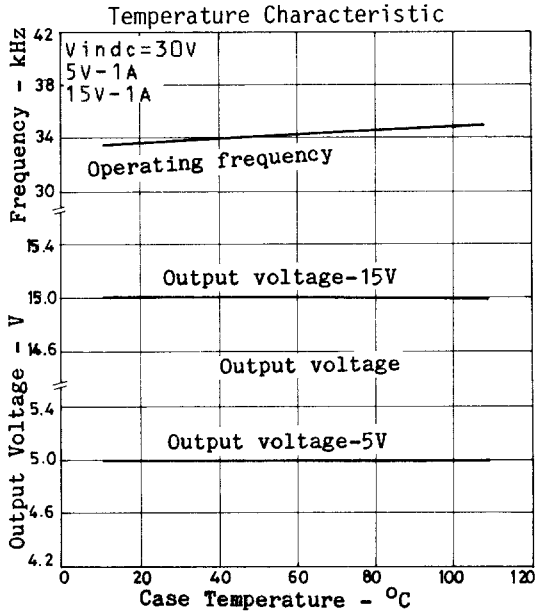


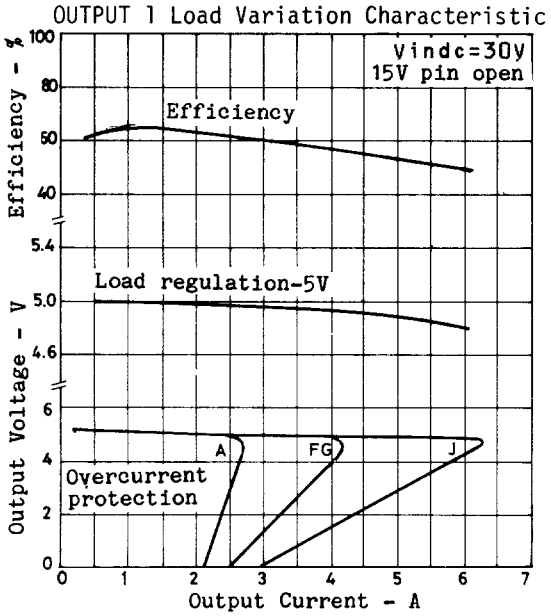
STK7562 Characteristics

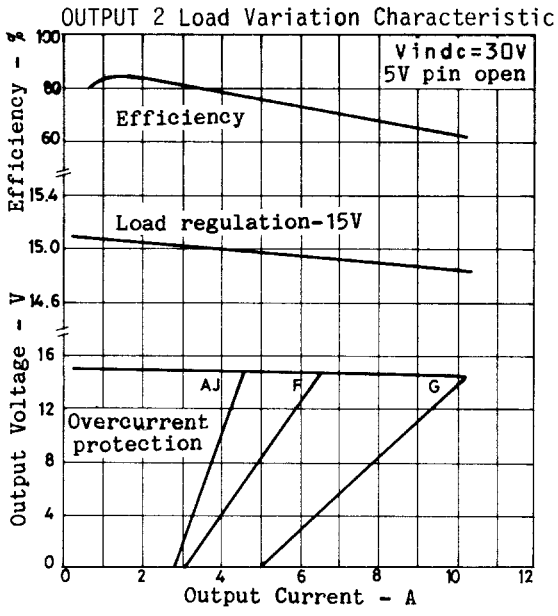
Input Variation Characteristic



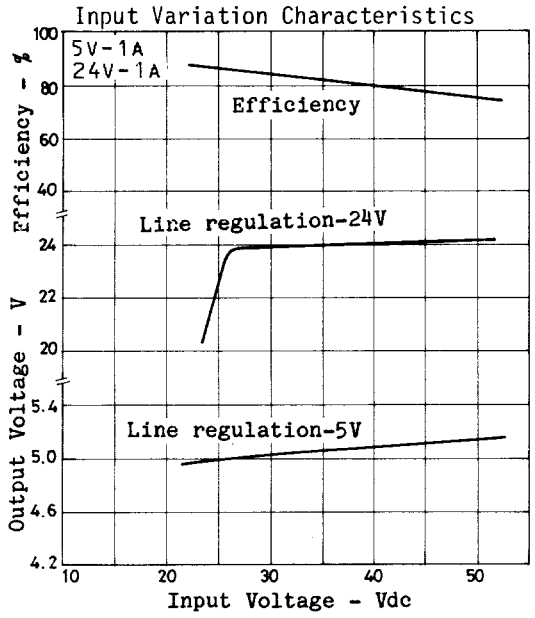
Temperature Characteristic

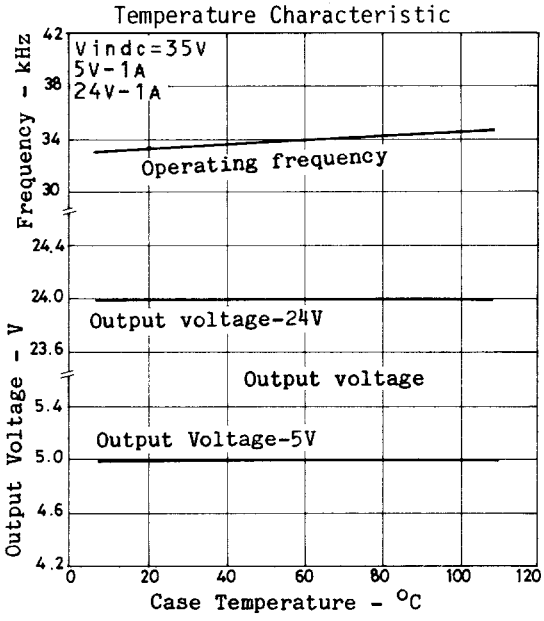


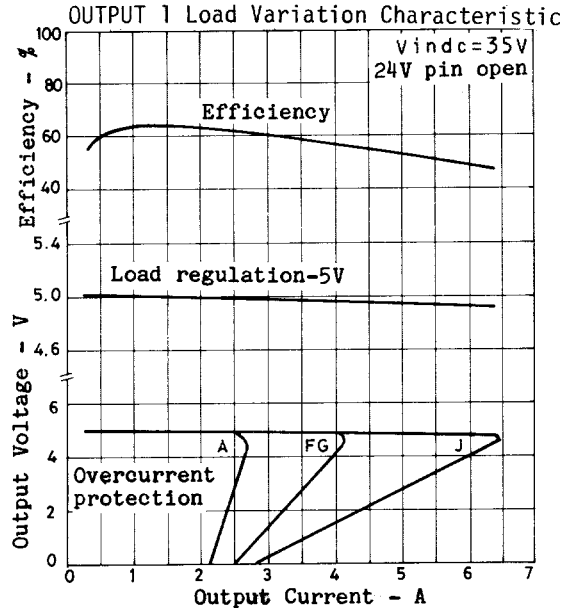


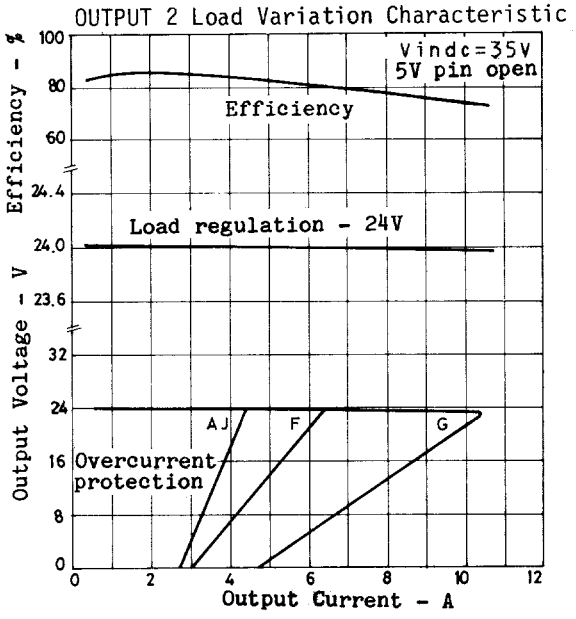


STK7563 Characteristics

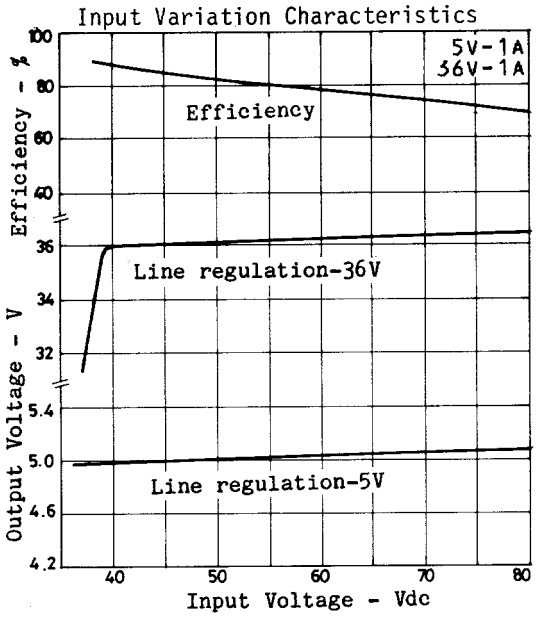


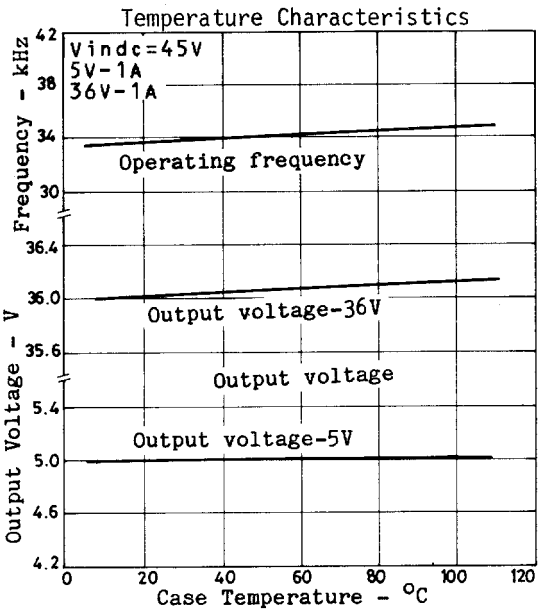


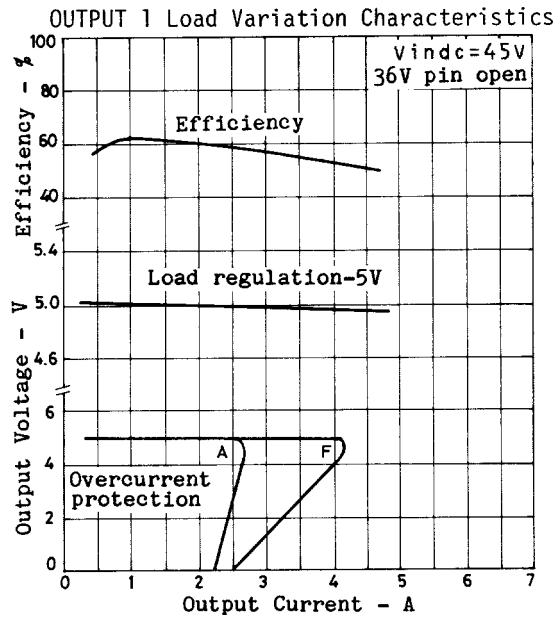


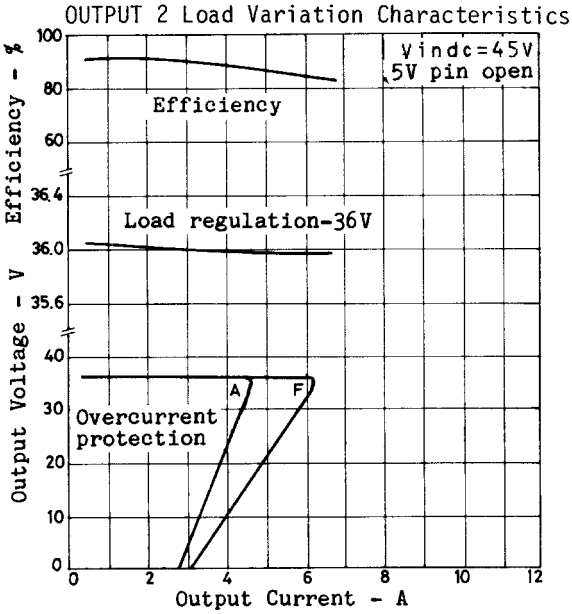


STK7565 Characteristics





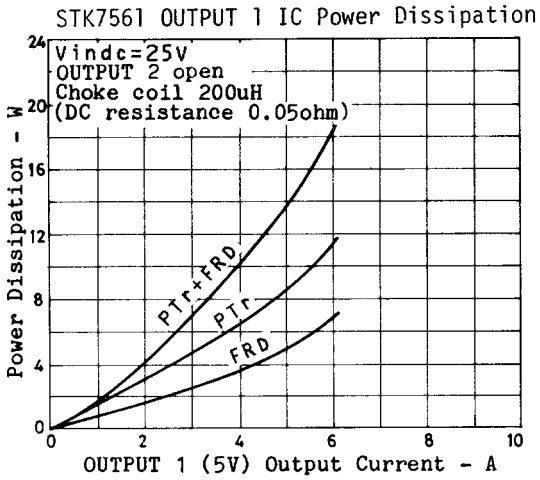


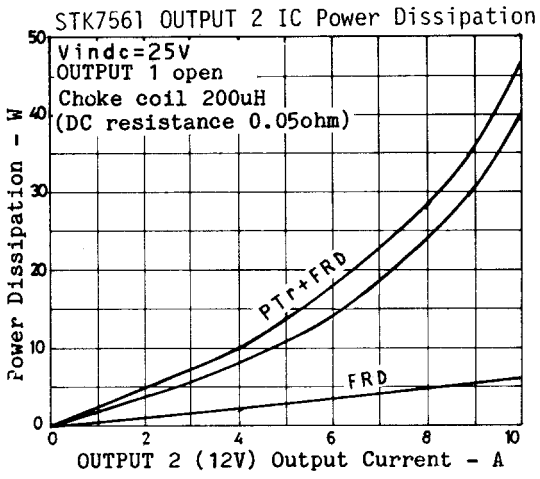


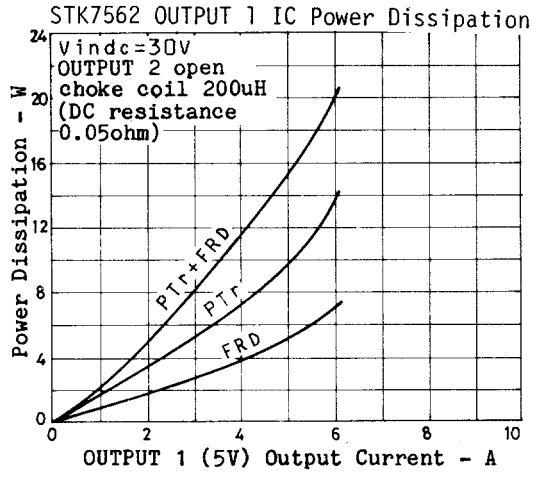
Termal Design

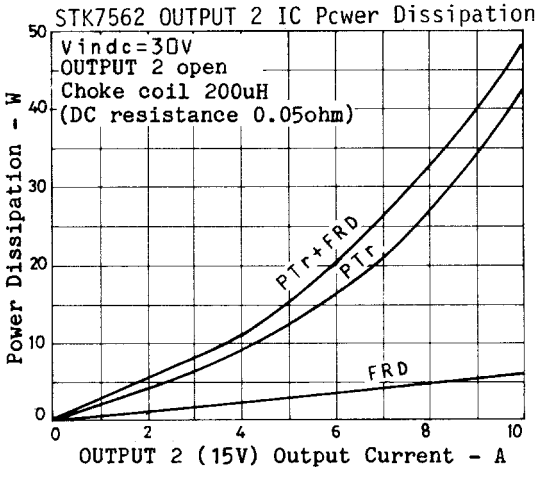
Most power dissipation of STK7560 series-applied volage regulators is caused by power transistor PTr, flywheel diode FRD, choke coil, current detect resistor.

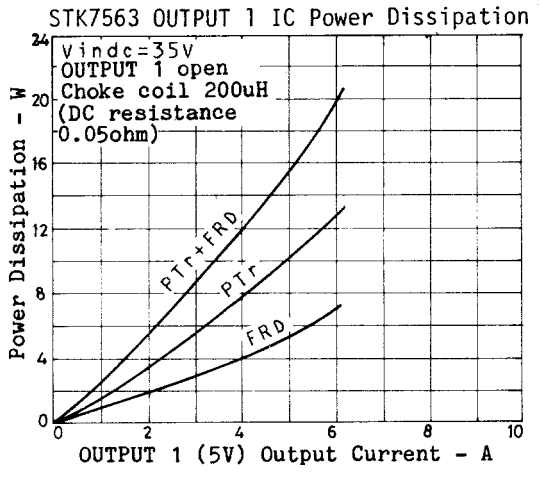
Power detect parts are PTr FRD for the IC system, and TR1, D3 for OUTPUT 1, and TR6, D4 for OUTPUT 2. The relation between output current and power dissipation is shown below.

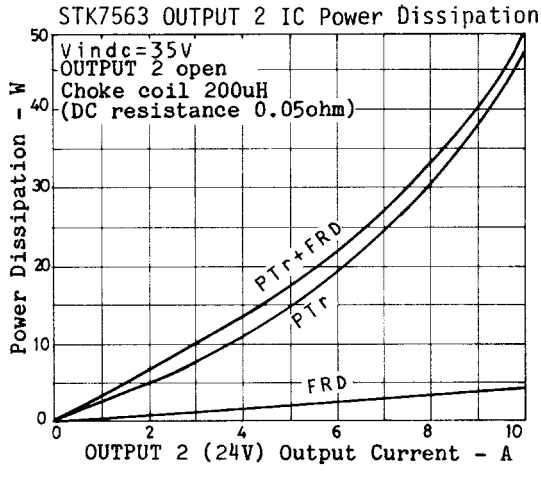












Assuming power dissipation in each element as follows :

P_T1 for power transistor of OUTPUT 1

PF_1 for FRD of OUTPUT 1

PT_2 for power transistor of OUTPUT 2

PF_2 for FRD of OUTPUT 2

Total power dissipation Pd in the IC and heat sink thermal resistance θca are :

$$Pd = (PT + PF1) + (PT2 + PF2) \ [W]$$

$$\theta ca = \frac{Tc - Ta}{Pd} \ [°C/W]$$

where Tc : Case temperature=105°C, Ta=Ambient temperature

Junction temperature in each element is :

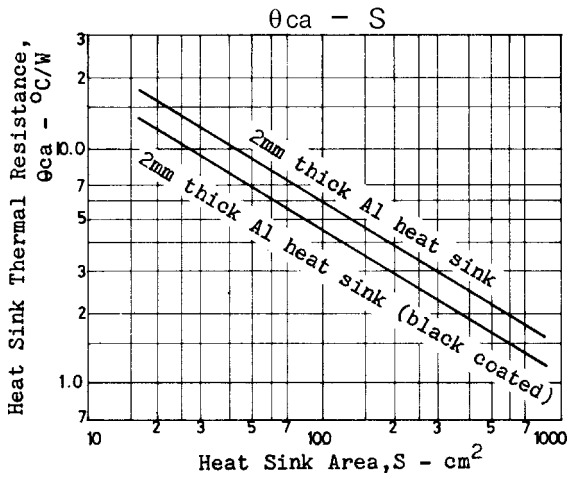
$$Tj = Pd \times \theta jc + Tc \ [°C]$$

where Tj max=150°C, Pd : Power dissipation P_T1, P_F1, P_T2, P_F2 in each element,
θjc=Junction-case thermal resistance in each element.

Type No.	Table of Thermal Resistanc θjc			
	OUTPUT 1		OUTPUT	
	TR1	D6	TR	D
STK7560A	45	12.	45	12.
STK7560F STK7560G	45	12.	25	5.
STK7560J	25	5	45	12.

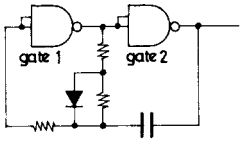
To dessipate heat satisfactorily, use a heat sink with thermal resistance θca meeting two temperature conditions of Tc max=105°C, Tj max=105°C.

Since the actual thermal resistance of the heat sink greatly depends on various conditions such as equipment layout or ventilation, allow an ample margin in thermal design. Shown right is the relation between Al heat sink area and thermal resistance. The Al surface coated with black improves thermal characteristic, lowering thermal resistance approximately 20% as compared with the Al heat sink of the same area.



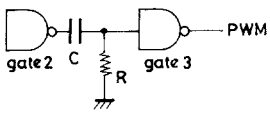
Description of Operation of Internal Blocks

[OSC]



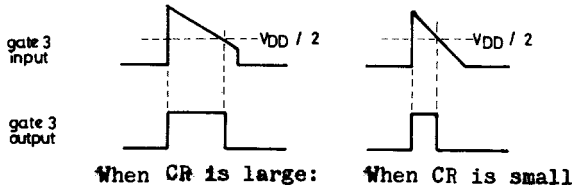
External excitation type OSC circuit where the CMOS NAND gate-used ring OSC is formed by the 2-stage NAND circuit, delivering basic pulses. This circuit provides pulse width modulation where the frequency is constant and the duty only varies.

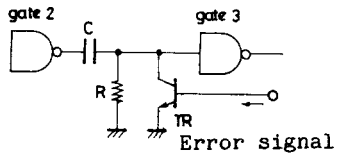
[PWM]



Pulse width modulation (PWM) is provided by differentiating the output of NAND gate 2 using the differentiating circuit of time constant CR as shown left and by applying the result to the input of NAND gate 3.

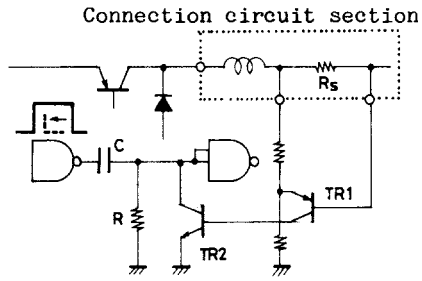
The threshold voltage at the input of NAND gate 3 is approximately 1/2 of supply voltage V_{DD} applied to the gate and the PWM output as shown below is obtained.





In the actual circuit transistor TR is connected in parallel with resistor R as shown left. The error signal from the constant-voltage output side is used to control the base current of TR so that the resistor value is varied equivalently to make the output voltage constant.
When the error signal is large, the base bias of TR is deepend and the equivalent resistance gets small, narrowing the pulse width to control the output voltage.
When the error signal is small, the base bias of TR is shallowed, widening the pulse width to control the output voltage.

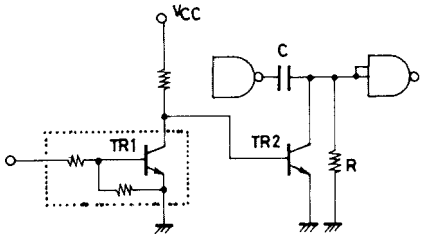
[OCP]



Overcurrent protection (OSC) is provided as follows : The voltage drop across current detect resistor Rs of the external connection circuit is detected to turn ON transistor TR1. Then, the collector current is applied to the base of TR2 to make time constant CR small, forcing the pulse width to be narrow.
The “fold-back” overcurrent characteristic occurs in which the pulse width is narrowd to drop the output voltage and also to decrease the output current.

[Cutoff]

The cutoff circuit (remote ON/OFF control) is so designed that the output is turned ON at ‘H’ level of cutoff input. In the circuit shown below, when the input is at ‘H’ level, TR1 is turned ON to drop the base voltage of TR2 and TR2 is turned OFF. Since TR2 is independent of the differentiating circuit composed of C and R, the output is turned ON.



When the input is at ‘L’ level, TR1 is turned OFF to increase the base voltage of TR2 and TR2 is turned ON. Since TR2 is connected in parallel with R of the differentiating circuit, R is short-circuited to make R of time constant CR O equivalently and the output is turned OFF.

New products = Development of 5V-1A rated small-sized STK7570 series

Series Lineup Type No.	Maximum Ratings / Ta=25°C			OUTPUT 1			OUTPUT 2		
	Vin max	Tg ma	Tst	Vv	Ilo a	Io p	Vv	Ilo a	Io p
	()ydc)	(°C)	(°C)	()V	()A	()A	()V	()A	(A
STK7571A STK7571B	50 [25]	105	–30 to +105	5V±0.1V	1 1	1.2 1.2	12V±0.2V	2 3	4 6
STK7572A STK7572B	50 [30]	105	–30 to +105	5V±0.1V	1 1	1.2 1.2	15V±0.3V	2 3	4 6
STK7573A STK7573B	60 [35]	105	–30 to +105	5V±0.1V	1 1	1.2 1.2	24V±0.4V	2 3	4 6
STK7575B STK7575B	70 [45]	105	–30 to +105	5V±0.1V	1 1	1.2 1.2	36V±0.6V	2 3	4 6