SGS-THOMSON MICROELECTRONICS

STKM2000 SERIES

2 µ/2 POLY/2 METAL BiCMOS MIXED ANALOG-DIGITAL STANDARD CELLS

- ADVANCED BICMOS 2 µ/2 POLY/ 2 METAL PROCESS
- TWIN TUB PROCESS
- HIGH LATCH-UP IMMUNITY
- POWER SUPPLY :
  MAXIMUM RATING : -0.5V TO 12V
  OPERATING CONDITIONS : 3V TO 10V
- MIXED ANALOG - DIGITAL LIBRARY :
  ANALOG BIPOLAR LIBRARY
  ANALOG CMOS LIBRARY
  ANALOG BICMOS LIBRARY
  DIGITAL CMOS LIBRARY
- HIGH PROCESS PERFORMANCES:
  TRANSITION FREQUENCY, NPN = 6 GHz
  VERTICAL PNP = 2, 5 GHz
  DIGITAL CMOS OPERATING FREQUENCY : UP TO 30 MHz
- CAD SOFTWARE SUPPORT:
  FULLY INTEGRATED A.D.S. (ANALOG DESIGN SYSTEM) WITH ANALOG BLOCK GENERATORS, SWITCHED CAPACITOR FILTER COMPILER; DIGITAL FUNCTIONS GENERATOR, RAM, ROM, PLA GENERATORS
- AVAILABILITY OF EEPROM DEVICES, ZENER DIODE, SCHOTTKY DIODE
- OPERATING TEMPERATURE RANGE:
  COMMERCIAL: 0 TO 70°C
  INDUSTRIAL: -40 TO 85°C
  MILITARY: -55 TO 125°C
- PACKAGE OPTIONS:
  DIL: PLASTIC OR CERAMIC
  SMD: SO, PLCC, QFP
  WAFER OR DIE

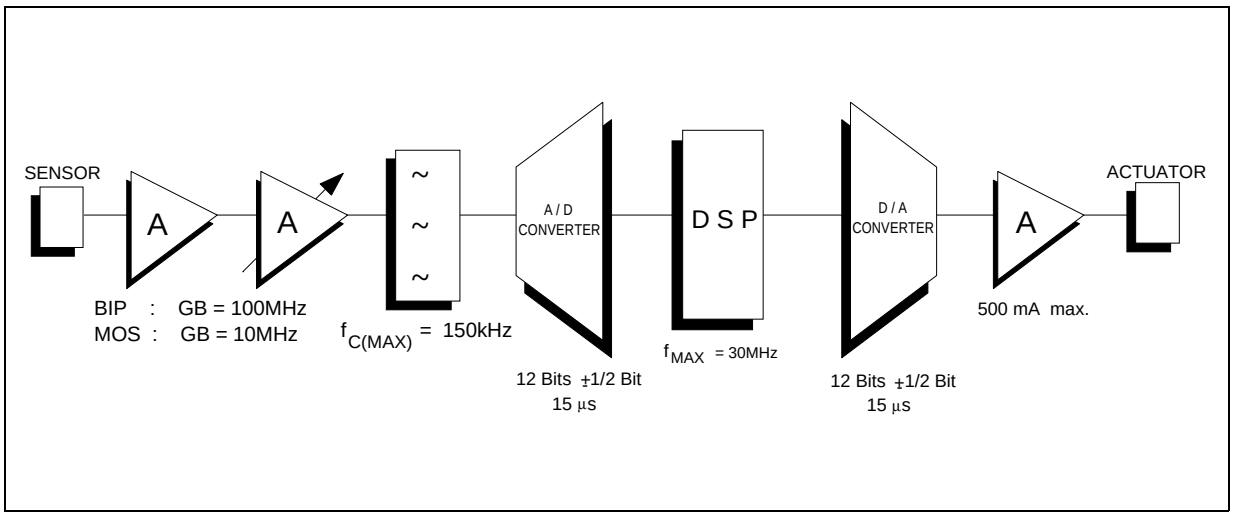
ASIC PRODUCTS DESCRIPTION

With the STKM2000 series, SGS-THOMSON Microelectronics introduces the “state of the art” product for analog signal processing, chain from sensor to actuator.

The introduction of new concepts (cells library and CAD) opens the design of analog functions and mixed analog and digital circuits with a safe and powerful approach. This new ASIC approach is the combination of innovative :

- BICMOS process
- Mixed libraries (ANALOG + DIGITAL)
- Generators and compilers
- “User friendly” CAD system
- Customer interface

Figure 1 : The STKM2000 Series, a complete system solution



STKM2000 ARCHITECTURE

Technology

The STKM2000 Series developed by SGS-THOMSON Microelectronics uses an advanced BICMOS silicon gate process with dual polysilicon layers and dual metal layers. This process is optimized to achieve high performance in digital CMOS applications. Depending on the operating supply voltage (10V, or 5V), the CMOS process behaves as an N-WELL technology (respectively with 2 µ gate length or 1.8 µ gate length) with operating speeds up to 30MHz. Thanks to the two metal layers, the digital part of the circuit can reach high gate density with low parasitic capacitances.

For analog functions, the STKM2000 series takes advantage of the bipolar structure:

- very high speed NPN transistor : f_T = 6 GHz
- very high speed vertical PNP : f_T = 2.5 GHz

This allows high gain - bandwith operational amplifier (50 MHz), low noise input amplifier, short propagation delay comparator, ...
With the same BICMOS process, the analog CMOS performance come from the high density CMOS structure with a double poly layer for accurate capacitors, low consumption CMOS amplifier (30 µA), CMOS switches, high accuracy switched capacitor filters (up to 100 kHz for center frequency).

STKM2000 cell concepts

SGS-THOMSON Microelectronics has predesigned and precharacterized cells which are selected, placed and interconnected on the chip to implement digital and analog cells having different height and supply voltages. In addition some macrocells are designed as fixed blocks, so called "hard blocks" : filters, A/D and D/A converters; some hard blocks are automatically generated and parametrized from a compiler: S.C. filters, PLA, RAM, ROM...

STKM2000 chip topology

The chip is optimized versus the cell complexity, in a row based structure with different heights.

Peripheral cells surround the internal active chip area to interface with its external environment.

Despite the row based architecture, "hard blocks" can be implemented with efficient floor planning organization.

STKM2000 Cell libraries

SGS-THOMSON Microelectronics introduces the "programmable" library; instead of working with a finite number of cells of the library, the designer has now access to an infinite number of functions.

Defining only some properties, the designer is able to create himself the cells needed for his application. For example, the following electrical parameters are accessible and adjustable:

- gain-bandwith product
- phase margins, frequency compensation
- output buffer current
- biasing currents
- resistor, capacitor fields
- current, source or sink
- adjustable Ron switch resistor
- supply voltage assignment

The analog library is operating in a large voltage range: 3V to 10V.

The basic analog library contains:

- 60 analog CMOS functions
- 25 analog BIPOLAR functions

From single transitor to 12 bits A to D converter (with autocalibration), each setup becomes possible.

The digital CMOS library uses the same flexibility with a complete set of basic digital functions (NAND, NOR, Flip-Flop, ...) and some cell generators:

- register, counter, logic comparator, ...

More than 60 digital cells are available.

Figure 2: The STKM2000 Series, a complete system solution

ANALOG LIBRARY

NPN transistor
Lateral PNP
Substrate PNP
Isolated PNP
NPN input comparator
PNP input comparator
N input comparator
P input comparator
N-MOS transistor
P-MOS transistor
NPN high-speed amplifier
N input CMOS Op-Amp
P input CMOS Op-Amp
Crystal oscillator
RC oscillator
Transconductance
Power-on reset
(with adjustable threshold and hysteresis)
Analog multiplexer
Voltage to current converter
Voltage reference
8 bits, A/D and D/A converters
12 bits A/D and D/A converters

DIGITAL LIBRARY

AND, NAND, OR, NOR, inverter
Exclusive OR, NOR
D latch
Input buffer (TTL/CMOS)
Output buffer (TTL/CMOS)
Shift register
Binary counter
Decimal counter
Magnitude comparator

CAD SUPPORT: A.D.S. (Analog Design System) SGS-THOMSON Microelectronics has introduced a sophisticated CAD approach to reduce the development leadtime and to increase design flexibility and safety.

Programmable cells in the library are defined as:
- alternative cell or,
- adjustable cell or,
- telescopic cell or,
- parametrisable cell

Some specific parts of the design are automatically handled by an analog design manager, in order to:

- reduce capture errors
- make unexperienced designer's task easier
- improve schematics lisibility
- check electrical design rules (Analog or Digital)

The Analog Design manager takes into account:
- transconductance block generation
- automatic cell biasing
- unconnected pins and power down processing
- multipower supplies processing

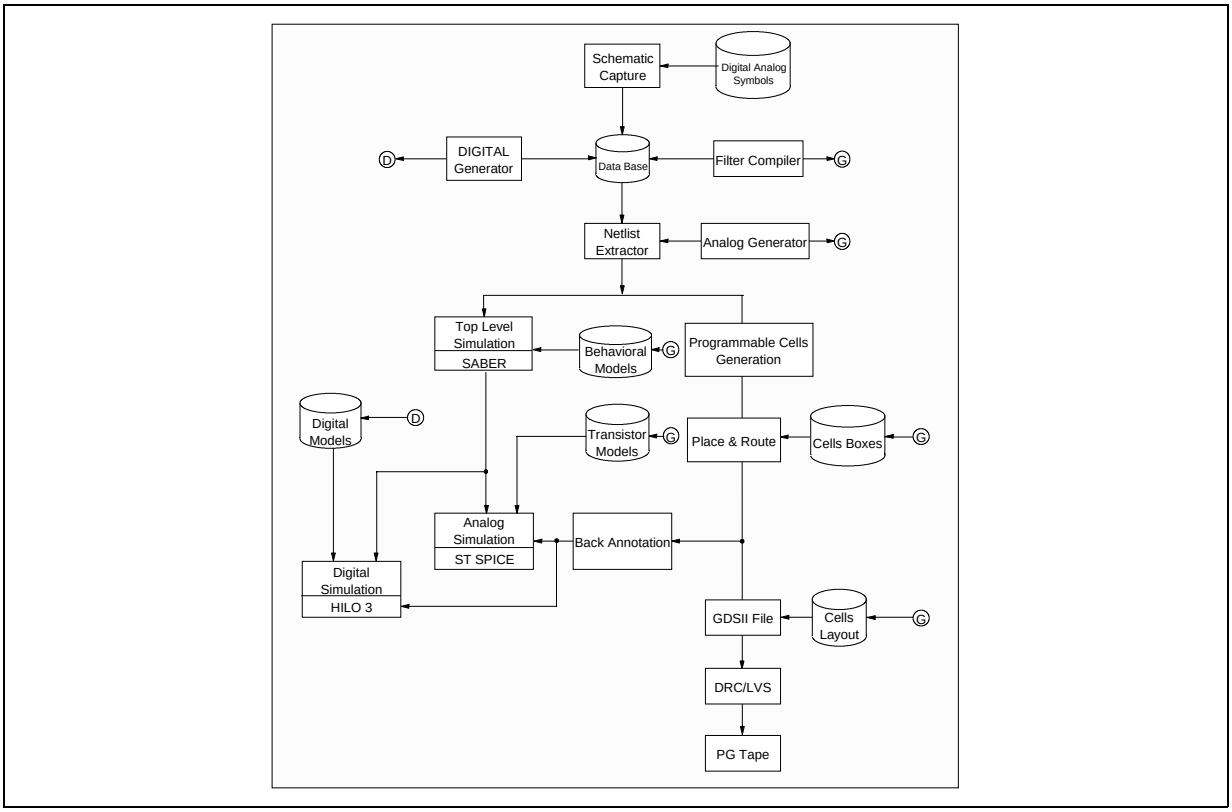
A major step has been made with the introduction of function generator and compiler approaches to improve design automation and design efficiency.

Operational amplifier generator
From a generic symbol and some properties, several parameters of the amplifier will be adjusted:

- Biasing current which controls major parameters of amplifier (gain-bandwidth, slew rate, power consumption).
- Frequency compensation which allows to adjust and optimize the dynamic parameters versus the capacitive and resistive load.
- Power down capabilities.
- Supply voltage of the cell.

A specific software manages all these properties and automatically updates all libraries included in the design flow: macro models and transistor level models, footprint, GDS2 layout, LVS netlist.

Figure 3: Analog Design System (A.D.S.) flow



Filter compiler
From the template defined at the beginning up to the complete layout, the software handles automatically the filter synthesis and the layout compilation:

- evaluation/mathematical analysis
- switched capacitor synthesis
- simulation
- Monte-Carlo analysis
- layout generation

Any kind of filters is available from 2nd up to 12th order.

Digital cell generator
For a set of basic digital cells, the user has access to generators which handle the netlists and interface with the layout tools.

The schematic capture uses a block which is programmable according to the required complexity.

The generator creates a " so-called" soft macrocell taking into account the complete netlist:

- counters
- shift registers
- magnitude comparators, ...

A part from the software automation, the A.D.S. CAD tool works around standard softwares.

The CAD approach is compatible with both approaches:

- VAX$_{TM}$/VMS operating system
- SUN$_{TM}$/UNIX operating system

	VAX$_{TM}$	SUN$_{TM}$
Schematic capture	CASS (SILVAR LISCO$_{TM}$)	EDGE (CADENCE$_{TM}$)
Logic simulation	HILO 3 (GENRAD$_{TM}$)	MOZART (SGS-THOMSON)
Analog simulation	ST-SPICE (SGS-THOMSON)	ST-SPICE (SGS-THOMSON)
Top level simulation	SABER (ANALOGY$_{TM}$)	SABER (ANALOGY$_{TM}$)
Layout	CALMP (SILVAR LISCO$_{TM}$)	EDGE (CADENCE$_{TM}$)
DRC - LVS	DRACULA (CADENCE$_{TM}$)	EDGE (CADENCE$_{TM}$)

Customer design interface
SGS-THOMSON Micorelectronics has developed several interfaces for customers giving them easy and flexible design approaches for STKM2000.

Users can access Analog Design System (A.D.S.):

- via SGS-THOMSON design centers
- via SGS-THOMSON associated design centers
- via CAE workstations

CAE worstation capabilities are under development on:

- Dazix System
- Mentor Graphics
- Sun

In that case,direct interfaces will be offered in order to make design implementation with A.D.S. (layout and test generations).

According to these design possibilities, SGS- THOMSON defines 3 main interfaces.

Figure 4 outlines these interfaces. Each interface details the responsibilities of customer and SGS-THOMSON during circuit development flow.

Figure 4: SGS-THOMSON - CUSTOMER interfaces

	Interface 2	Interface 3	Interface 4
Responsibility level	**Breadboard schematics**	**Simulated schematics**	**Layout tape**
Circuit definition	Ctm	Ctm	Ctm
Schematics	ST		
Simulations			
Layout		ST	
Final control	ST + Ctm	ST + Ctm	ST + Ctm
Prototyping phase	ST	ST	ST

MAXIMUM RATINGS

Symbol	Parameter	Min	Max	Unit
V_{DD}	Supply voltage	- 0.5	12.0	V
V_I, V_O	I/O voltage	- 0.5	V_{DD} + 0.5	V
I_I, I_O	I/O current	- 40	+ 40	nA
T_{stg}	storage temp. (ceramic)	- 65	+ 150	^oC
	storage temp. (plastic)	- 40	+ 125	^oC

Note 1: Stresses above those under "maximum ratings" may cause permanent damage to the device. This is a stress rating only and functional operation for the device at these or any other conditions above indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED DC OPERATING CONDITIONS

Voltage referred to V_{SS}

Symbol	Parameter	Min	Max	Unit
V_{DD}	Operating supply voltage	2.7	11	V
T_{amb}	Operating ambient temperature			
	Military	- 55	+ 125	^oC
	Industrial	- 40	+ 85	^oC
	Commercial	0	+ 70	^oC

DIGITAL LIBRARY AC ELECTRICAL CHARACTERISTICS ABSTRACT

Standard condition = 2 loads + 1 mm of metal interconnect

Cell code	Description	V_{DD} = 10V ± 10%, T = 25°C			Unit
		TPHL	TPLH	OTHER	
IV1	Standard inverter	2.26	2.01		ns
ND2	2 - input NAND	1.74	2.44		ns
NR2	2 - input NOR	2.55	2.02		ns
FD1	D Flip - Flop				
	From C to QN	6.44	8.26		
	TSU			5.00	
	TH			1.75	ns
	TWH			8.25	
	TWL			5.00	
OB11	CMOS inverting output buffer				
	capacitance load = 100 pF	12.4	12.3		ns

DC GENERAL ELECTRICAL CHARACTERISTICS

V_{DD} = 5V ± 10% or V_{DD} = 10V ± 10% (unless otherwise specified)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{IH}	High level TTL input voltage	V_{DD} = 5V ± 10%				
		T^o = 0°C / + 70°C	2.0			V
		T^o = - 40°C / + 85°C	2.25			V
		T^o = - 55°C / + 125°C	2.25			V
V_{IL}	Low level TTL input voltage	V_{DD} = 5V ± 10%			0.8	V
		all temp. ranges				V
V_{IH}	High level CMOS input voltage		70%VDD			V
V_{IL}	Low level CMOS input voltage				30%VDD	V
I_{OZH}	Tristate output leakage current	V_O = V_{DD}				
		T^o = 0°C / + 70°C			2.5	µA
		T^o = - 40°C / + 85°C			5	µA
		T^o = - 55°C / + 125°C			10	µA
I_{OZL}		V_O = V_{SS}				µA
		T^o = 0°C / + 70°C	- 2.5			µA
		T^o = - 40°C / + 85°C	- 5.0			µA
		T^o = - 55°C / + 125°C	- 10.0			µA
I_{IH}	High level input leakage current	VO = V_{DD}				
		T^o = 0°C / + 70°C			1.0	µA
		T^o = - 40°C / + 85°C			3.0	µA
		T^o = - 55°C / + 125°C			5.0	µA
I_{IL}	Low level input leakage current	VI = V_{SS}				
		T^o = 0°C / + 70°C	- 1.0			µA
		T^o = - 40°C / + 85°C	- 3.0			µA
		T^o = - 55°C / + 125°C	- 5.0			µA
I_{CC}	Max admissible current per pin:					
	- analog				± 20	mA
	- digital				± 40	mA

ANALOG LIBRARY AC ELECTRICAL CHARACTERISTICS ABSTRACT

Cell code	Description	Parameters Test conditions	Min	Typ	Max	Unit
CMP11	Static CMOS comparator	Propagation delay (overdrive = 5 mV) Offset		1 ± 3	1.4 ± 10	ms mV
CMP31	Static BICMOS comparator	Propagation delay (overdrive = 5 mV) Offset		90 ± 2	110 ± 7	ns mV
CPX11	Capacitor fields	Unit capacitance Capacitor value range Absolute accuracy Matching (capacitor ratio)	 0.1 	0.1 0.5	 50 ± 15 1.0	pF pF % %
CPP11	Monolithic Capacitor	Capacitor range Absolute accuracy	1 	 	100 ± 15	pF %
RPM/PPM	Resistor/Potentiometer P-Base	Resistor value range Absolute accuracy Matching Temperature coefficient Voltage coefficient	6.5 	 	3000 ± 20 ± 1 0.2 0.05	KΩ % % % %
SWI1	Analog switch	Elementary switch RON value Number of switches in parallel	 1	5 	25 3	KΩ
MN11	Telescopic NMOS transistor	RON value		100		Ω
OPA31	General purpose MOS Operational amplifier	Unity gain bandwidth Current consumption Phase margin (C1 = 100 pF, R2 = 10 kΩ) Offset		3.3 700 60 ± 3	4.6 ± 10	MHz µA ° mV
OPA41	Internal bipolar Operational Amplifier	Unity gain-bandwidth current consumption Phase margin (CL = 15 pF, RL = 100kΩ) Offset		9 240 62 ± 1	30 ± 5	MHz µA ° mV
OPA71	Rail to rail external MOS operational Amplifier	Unity gain bandwidth current consumption Phase margin (CL = 100 pF, RL = 100KΩ) Offset		2.3 360 80 ± 3	 ± 10	MHz uA ° mV
OTA11	MOS transconductance amplifier	Unity gain - bandwidth (CL = 2 pF)		24		MHz
POR11	Programmable Power on Reset	Active Level Accuracy Hysteresis Accuracy			± 5 ± 5	% %
VRF11	Voltage bandgap reference	Output voltage accuracy Temperature coefficient Current consumption		 15	± 2 100 	% ppm µA

ANALOG LIBRARY AC ELECTRICAL CHARACTERISTICS ABSTRACT

Cell code	Description	Parameters Test conditions	Min	Typ	Max	Unit
OSC11	Programmable crystal oscillator	Frequency	0.1		20	MHz
OSC41P	RC oscillator	Frequency Stability versus temperature Stability versus voltage	1	100 0.01 0.5	800	KHz % / ^{o}C % / V
OSC31P	One pad I.C oscillator	Frequency Stability versus temperature Stability versus voltage	2	 0.01 0.5	200	KHz % / ^{o}C % / V
	Filters	Order Center frequency	2		12 100	 KHz
ADC81	8 bit analog to digital converter	Conversion time Integral non linearity Differential non linearity			5 ± 0.5 ± 0.5	µs LSB LSB
DAC81	8 bit analog to digital converter	Conversion time (CL = 2 pF) Integral non linearity			1 ± 0.5	µs LSB