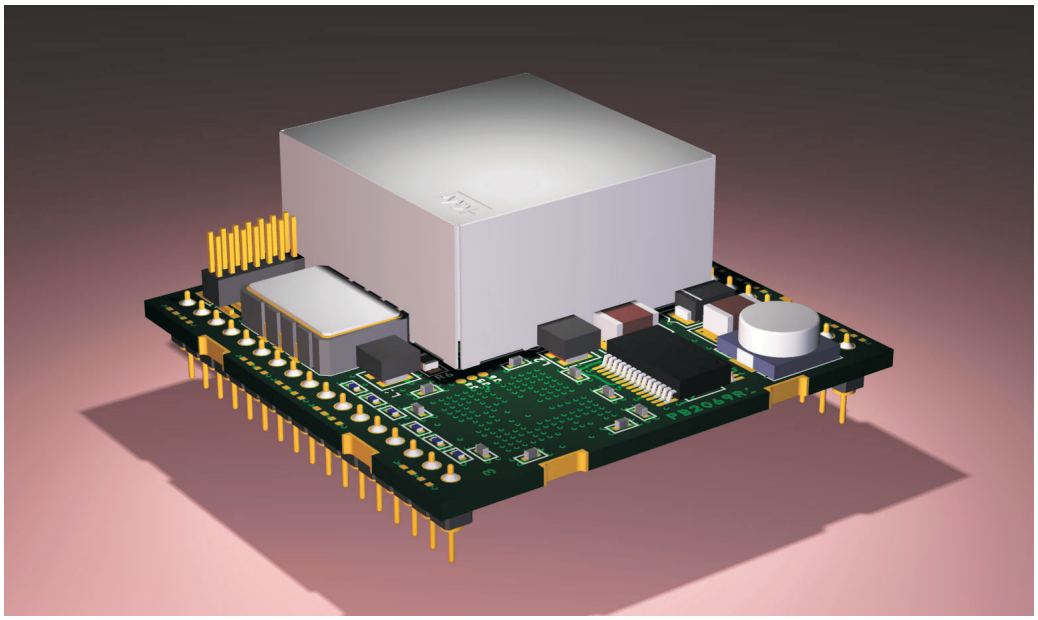
Stratum 3 Timing Module
STL-S3

CONNOR WINFIELD

2111 Comprehensive Drive
Aurora, Illinois 60505
Phone: 630-851-4722
Fax: 630-851-5040
www.conwin.com



Application

The Connor-Winfield Stratum 3 Simplified Control Timing Module acts as a complete system clock module for Stratum 3 timing applications in accordance with GR-1244-CORE, Issue 2, GR-253-CORE, Issue 3, and ITU-T G.812, Option III.

Connor-Winfield's Stratum 3 Timing module helps reduce the cost of your design by minimizing your development time and maximizing your control of the system clock with our simplified design.

Features

- 6 Input References
- Hitless Switch Over
- CMOS output up to 77.76 MHz
- 8 kHz Output
- Fast Acquisition Mode
- Manual/ Autonomous Operation
- Master/Slave Configuration
- Revertive/Non-revertive Modes

Bulletin	**TM055**
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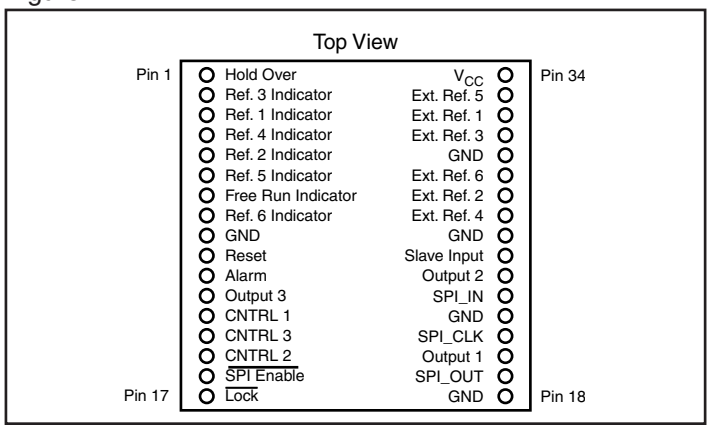
General

Connor-Winfield's STL timing module provides Stratum 3 synchronization for a complete system clock solution in a single module in accordance with GR-1244-CORE Issue 2, GR-253-CORE Issue 3, and ITU-T G.812 Option III. The STL provides a reliable network element clock reference to line cards used in TDM, PDH, SONET, and SDH application environments. Typical applications include digital cross connects, DSLAMs, ADMs, multiservice platforms, switches and routers.

The STL meets 0.37 ppm Hold Over requirements over 0° - 70°C temperature range. The 3.3V power requirement will draw a maximum of 1.3 A during an initial start-up period and then drop to a typical current of 0.5A during normal operating conditions. It accepts six input references and can supply up to 3 CMOS outputs (see Tables 1-4 for specific information).

Pin Diagram

Figure 1



Functional Block Diagram

Figure 2

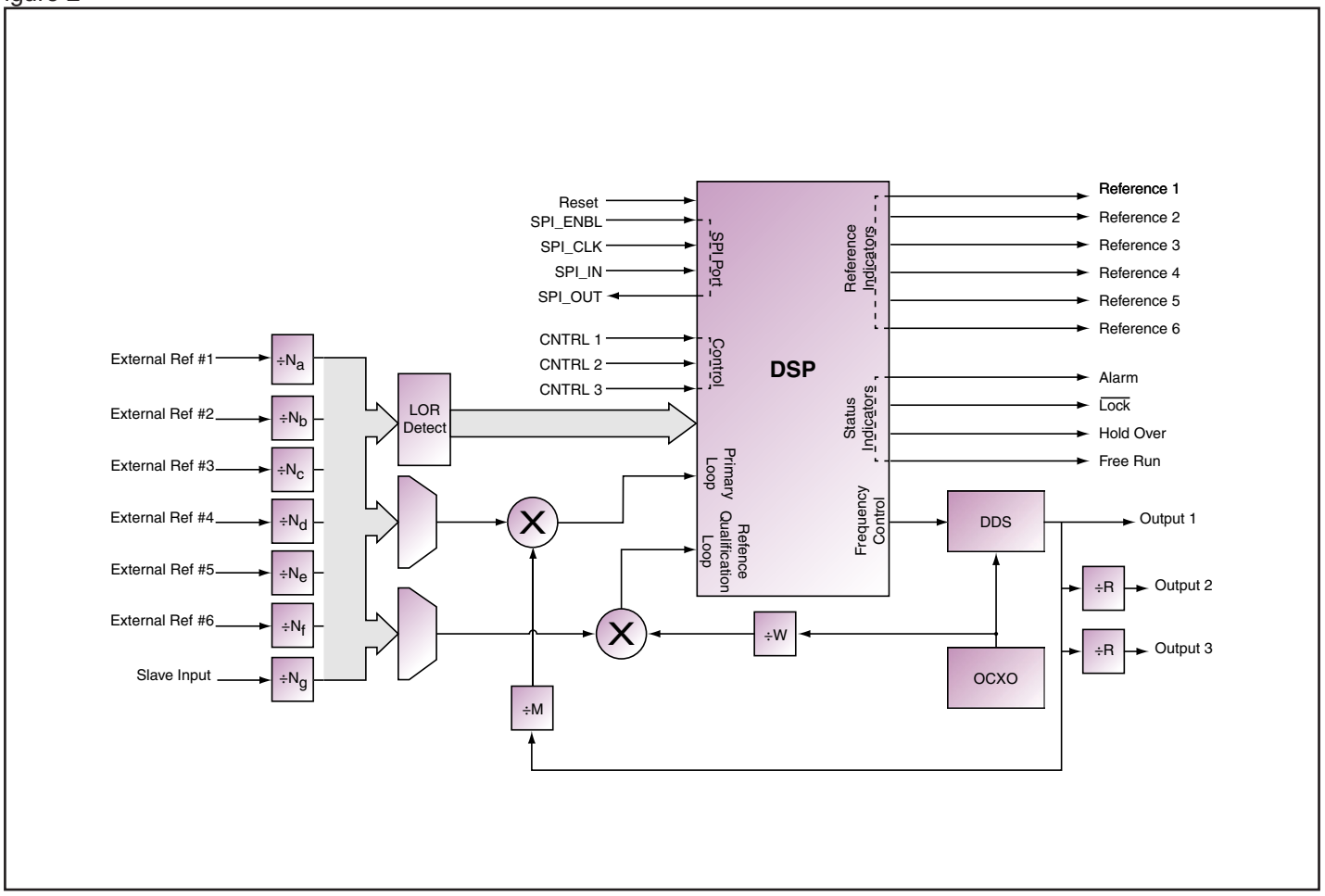


Table 1

Absolute Maximum Rating

Symbol	Parameter	Minimum	Nominal	Maximum	Units	Notes
V_{CC}	Power Supply Voltage	-0.5		4.0	Volts	1.0
V_I	Input Voltage	-0.5		5.5	Volts	1.0
T_s	Storage Temperature	-40		85	deg. C	1.0

Table 2

Recommended Operating Conditions

Symbol	Parameter	Minimum	Nominal	Maximum	Units	Notes
V_{cc}	Power Supply Voltage	3.135		3.465	Volts	
V_{IH}	High level input voltage - CMOS	2.0		5.25	Volts	2.0
V_{IL}	Low level input voltage - CMOS	0		0.8	Volts	
t_{PULSE}	Minimum pulse width, positve/negative for external references	30			ns	
t_{TR}	Input signal transistion time			250	ns	
t_{RST}	Time for module to re-configure after a reset (manual or POR)		1.5		sec.	
t_{HLD}	Time to hold reset pin high	0.3		100	ms	

Table 3

DC Characteristics

Symbol	Parameter	Minimum	Nominal	Maximum	Units	Notes
V_{OH}	High level output voltage, I_{OH} = -4.0mA, V_{CC} = min.	2.4	3.3	3.6	Volts	3.0
V_{OL}	Low level output voltage, I_{OL} = 8.0mA, V_{CC} = max.			0.4	Volts	

Table 4

Specifications

Parameter	Specifications	Notes
Frequency Range - Output 1	8 kHz - 77.76 MHz	6.0
Output 2	8 kHz - 77.76 MHz	6.0
Output 3	8 kHz - 77.76 MHz	6.0
Supply Current	0.5A typical @25°C, 1.3 A during warm-up (Maximum)	
Timing Reference Inputs	8 kHz - 77.76 MHz	6.0
Slave Input	8 kHz	
Jitter, Wander and Phase Transient Tolerances	GR-1244-CORE 4.2-4.4, GR-253-CORE 5.4.4.3.6	
Wander Generation	GR-1244-CORE 5.3, GR-253-CORE 5.4.4.3.2	
Wander Transfer	GR-1244-CORE 5.4	
Jitter Generation	GR-1244-CORE 5.5, GR-253-CORE 5.6.2.3	
Jitter Transfer	GR-1244-CORE 5.5, GR-253-CORE 5.6.2.1	
Phase Transients	GR-1244-CORE 5.6, GR-253-CORE 5.4.4.3.3	
Output 1,2 & 3 Free Run Accuracy	±4.6 ppm over temperature range	
Hold Over Stability	±0.370 ppm	4.0
Inital Offset	±0.050 ppm	
Temperature	±0.280 ppm	
Drift	±0.040 ppm	
Maximum Hold Over History	1049 seconds	
Minimum Time for Hold Over	141 seconds after a reference rearrangement	
Lock Time	100 sec.	
Lock Accuracy	0.1 ppm	5.0
Environmental Characteristics		
Shock	100G's, 6mS, halfsine per MIL-STD-202F, Method 2138, Test Condition C	
Vibration	0.06" D.A. or 10G peak 10 to 500 Hz, per MIL-STD-202F, Method 204D, Test Condition A	

NOTES:

1.0: Stresses beyond those listed under Absolute Maximum Rating may cause damage to the device. Operation beyond Recommended Conditons is not implied.

2.0: Inputs are 3.3V CMOS,5V tolerant

3.0: Logic is 3.3V CMOS

4.0: Hold Over stability is the cumulative fractional frequency offset as described by GR-1244-CORE, 5.2

5.0: After 100 seconds at stable temperature (±5° F)

6.0: Frequencies must be specified at the time of order.

Pin Description

Table 5

Pin #	Connection	Description
1	Hold Over	Indicator = 1 when module is in Hold Over
2	Reference 3	Indicator = 1 when module is locking to or is locked to external reference 3
3	Reference 1	Indicator = 1 when module is locking to or is locked to external reference 1
4	Reference 4	Indicator = 1 when module is locking to or is locked to external reference 4
5	Reference 2	Indicator = 1 when module is locking to or is locked to external reference 2
6	Reference 5	Indicator = 1 when module is locking to or is locked to external reference 5
7	Free Run	Indicator = 1 when module is in Free Run
8	Reference 6	Indicator = 1 when module is locking to or is locked to external reference 6
9	GND	Ground
10	Reset	Reset Pin (↓)*
11	Alarm	Indicator = 1 when module is in an alarm condition
12	Output 3	8 kHz output derived from system clock
13	CNTRL 1	Mode control input for manual operation. (↓)
14	CNTRL 3	Mode control input for manual operation. (↓)
15	CNTRL 2	Mode control input for manual operation. (↓)
16	$\overline{\text{SPI Enable}}$	Enable for SPI communication port. (↑)
17	$\overline{\text{Lock}}$	Indicator = 0 when module is locked to selected reference.
18	GND	Ground
19	SPI_OUT	Serial data output for SPI communication
20	Output 1	System clock output
21	SPI_SCLK	Input clock for SPI communication. (↓)
22	GND	Ground
23	SPI_IN	Serial data input for SPI communication
24	Output 2	8 kHz output derived from system clock
25	Slave Input	Input for synchronizing a module in slave configuration.
26	GND	Ground
27	External Reference 4	External reference input #4
28	External Reference 2	External reference input #2
29	External Reference 6	External reference input #6
30	GND	Ground
31	External Reference 3	External reference input #3
32	External Reference 1	External reference input #1
33	External Reference 5	External reference input #5
34	V_{CC}	+3.3V_{cc} power supply required

(↑) = Internal pull-up
(↓) = Internal pull-down
Internal pull-up/pull-down resistors range from 50 kΩ to 100 kΩ
(↓)* = 10 kΩ pull-down resistor

Functional Truth Table

Table 6

Reference#	Alarm	$\overline{\text{Lock}}$	Hold Over	Free Run	Condition
1	0	1	0	0	Locking to selected reference but the phase error is > 20µs
1	0	0	0	0	Tracking selected reference and the phase error is ≤ 20µs
0	1	1	1	0	Auto Mode - There are no valid references so module has entered Hold Over.
0	1	1	1	0	Manual Mode - Module is in Hold Over mode.
0	1	1	0	1	Auto Mode - There are no valid references and there is no valid Hold Over history so module has entered Free Run.
0	1	1	0	1	Manual Mode - Module is in Free Run mode.
0	0	0	0	0	Slave Mode - Module is locked to master module and phase error is ≤ 20µs
0	0	1	0	0	Slave Mode - Module is locked to master module and phase error is > 20µs
0	1	1	0	0	Slave Mode - Module is unable to track master module due to Loss of Reference condition or the frequency is out of range.

Control Inputs

Table 7

CNTRL3/CF3	CNTRL2/CF2	CNTRL1/CF1	Mode of Operation
0	0	0	Free Run
0	0	1	Locked to Ref #1
0	1	0	Locked to Ref #2
0	1	1	Hold Over
1	0	0	Locked to Ref #3
1	0	1	Locked to Ref #4
1	1	0	Locked to Ref #5
1	1	1	Locked to Ref #6

Module Restabilization Times

Table 8 - For a given off-time, the time required to meet daily aging, short term stability and TDEV requirements:

Off Time	**Restabilization Time**
< 1 Hour	< 1.5 Hours
< 6 Hour	< 8 Hours
< 24 Hour	< 36 Hours
1 to 16 Days	36 Hours + ¼ Off Time
> 16 Days	< 5 Days

Operation Overview

The STL offers both manual and autonomous modes of operation, and the option of revertive or non-revertive reference switching during autonomous mode. In manual mode, the user has control of the module using pins CNTRL 3:1 to determine whether the module should lock to a specific reference, enter Free Run or enter Hold Over. In autonomous mode, the module determines the proper operating behavior depending on the state of the external references, which are frequency qualified by the module. For further details of autonomous operation, see the state diagram in Figure 3. The STL also offers master and slave modes and incorporates reference qualification on all 6 external references and the Slave Input.

When the module is locked to a valid reference, the appropriate external indicator will be asserted for that reference. When internal phase error is less than 20µs, the $\overline{\text{Lock}}$ signal will be asserted. The STL takes up to 100 seconds to obtain complete phase lock to a qualified reference. To assure that the STL will always lock to any valid frequency offset within 100 seconds, the module goes into a Fast Acquisition mode immediately after switching to a new reference. If the module experiences a $\overline{\text{Lock}}$ alarm after it has phase-locked to the selected reference, the module will re-enter the Fast Acquisition stage of filtering if the reference has not been disqualified. Once locked, the filtering will return to the 0.1 Hz filter. The filtering during Fast Acquisition mode will not allow frequency movement faster than 2.9 ppm per second on a frequency step of up to 9.2ppm. Fast Acquisition mode is further described as fast start mode in GR-1244-CORE, Issue 3, section 3.6. The current PLL status can be accessed via SPI port in register 0Eh.

A manual reset pin called Reset is provided on pin 10 of the STL device. This will reset the DSP, FPGA, and DDS causing a disruption in all programmable devices and is the same type of reset, though not software controlled, described in Table 16. The STL device will treat this reset as if it were following a power-up; all registers are reset to their default values. Resetting the unit by cycling the power requires more time for restablization of the internal ovenized oscillator and is not recommended.

Hold Over mode provides a stable frequency that is guaranteed to be within ±0.370ppm over the entire temperature range for the first 24 hours after entry into Hold Over. The module establishes a new Hold Over history within 141 seconds after a reference is selected and continues to do a running average every 8 seconds for the next 1049 seconds. Long-term Hold Over values are based on a 1049 second moving window average. Hold Over values are not updated when the reference is disqualified or during Fast Acquisition mode. Hold Over values are buffered for at least 32 seconds to allow enough time to respond to the alarms and frequency qualification status.

Free Run is a mode of operation in which the module is not locked to a reference and its output frequency is solely dependent on the initial frequency setting of the internal oscillator. The output frequency in Free Run is guaranteed to be ±4.6ppm of the nominal frequency.

Reference qualification continually monitors all 6 input references, as well as the Slave Input. The references are monitored for both frequency accuracy and presence. Although loss of presence is detected almost immediately due to being continually monitored, a delay of approximately 7 seconds may occur before an out-of-band frequency is detected. This delay is caused by the fact that reference qualification is done one reference at a time, in a round robin fashion. Each reference takes just over one second to qualify, and so cycle time is the cause of the delay.

The STL module provides three output frequencies. Output 1 is the primary synchronized output. It is phase locked to the input reference during normal operation and is set to a fixed frequency when operating in Hold Over or Free Run. Output 2 and Output 3 are derived from Output 1.

The STL module provides a variety of alarm and status information to alert the user to multiple conditions that may affect the overall performance of their system. Some of this information is brought out to external pins, while other information is accessible through the SPI port on internal memory-mapped registers. Status information from reference qualification, including frequency offsets, is contained in these registers; information regarding phase build out and valid Hold Over is also stored here. Additionally, the current mode of operation and SPI status are available. Certain features of the STL are programmable by the user. For complete details on memory-mapped registers, please see SPI Timing and Operation section. For SPI timing, see Figures 7-8.

In master mode, the module will experience an alarm condition (Alarm=1) when the module is in Hold Over or Free Run. In manual mode, an alarm condition will occur if the user selects Hold Over, Free Run or a reference that is disqualified. If the reference is disqualified after the module starts to track it, the module will enter holdover if a valid holdover history is available, or the unit will enter Free Run (see figure 19). In autonomous mode, the module will experience an alarm condition when there are no available references. This may be caused by all references being disqualified by LOR or an off-frequency condition or all references may be set to unavailable in the priority table. In these cases, the module will enter holdover if there is a valid holdover history available, or the module will enter Free Run. In slave mode, the module will experience an alarm condition if the module is not able to lock to the master because the master frequency has exceeded the pull-in range of the slave, or due to an LOR of the master.

The $\overline{\text{Lock}}$ indicator will be de-asserted ($\overline{\text{Lock}}$=1) when the internal phase error is greater than 20us from the final, locked value (See figure 20). This alarm can occur when the unit is initially locking to a new reference, or it can occur after lock if the module loses lock. This alarm will be de-asserted ($\overline{\text{Lock}}$=1) during holdover and freerun modes.

Phase build out operation can be internally enabled or disabled through the internal memory-mapped registers. It is initially disabled. Internal circuitry monitors the input reference for greater than 3.4µs of change over any 0.1 second interval. When this occurs, internal buffers are reset so that the phase change is ignored, allowing the phase shift between input and output. Any phase shift smaller than 3.4µs over 0.1 seconds will be followed to re-establish the original input/output phase relationship, unless the rate of change causes the reference to be disqualified. Refer to Reference Qualification section (pg. 10) for more details on disqualification.

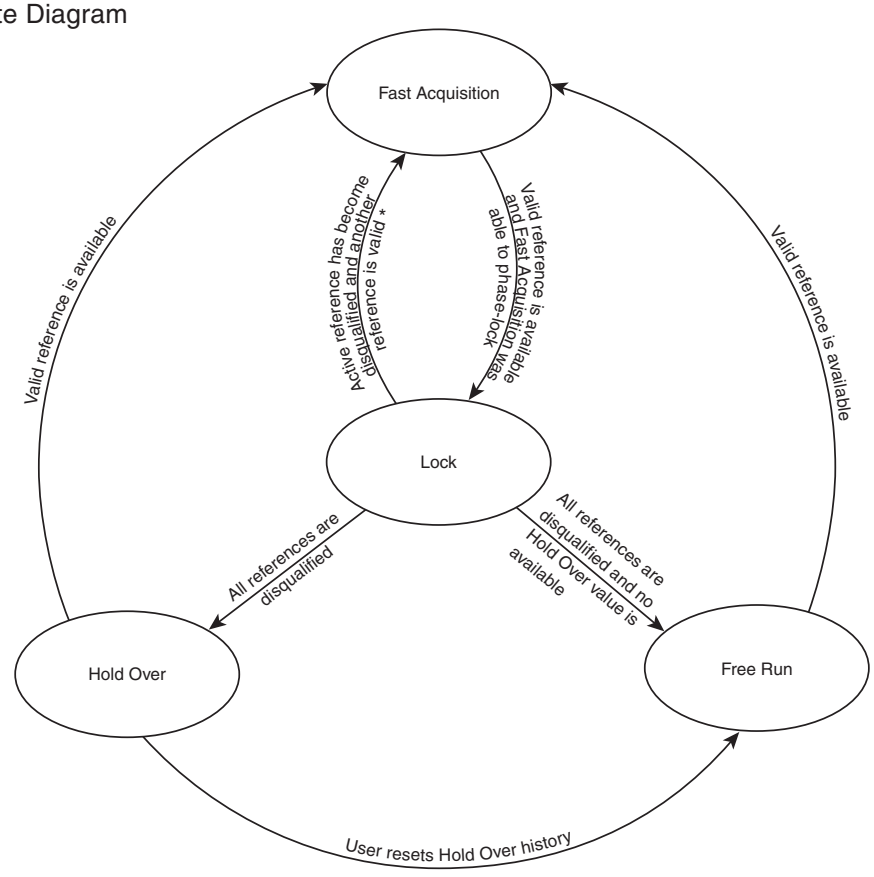
The STL meets the requirements for wander generation and wander transfer as required by GR-1244, sections 5.3 and 5.4. It also complies with phase transient requirements during Reference Rearrangement, Entry into Hold Over, and 1µs transient. Input jitter is attenuated at about 20 dB/decade to minimize the jitter noise passed on to other network elements or clocks. Figure 15 illustrates the STL's typical roll off of attenuated jitter.

Autonomous Mode

During autonomous mode, the unit makes the decision about which reference to track based on priority and qualification status. The goal of the module is to lock onto the highest priority qualified reference. If the revertive option is selected, the module will switch out of the current reference, even when that reference is still qualified, as soon as a higher priority qualified reference becomes available. The module will also switch into the highest priority qualified reference when the current reference is disqualified. If the non-revertive option is selected, the module will only switch into another reference when the current reference is disqualified.

If the current reference is disqualified, and there are no other qualified references to switch to, the module will enter the last valid Hold Over value. As soon as a reference is qualified, the module will begin to track it. If no Hold Over value has been calculated, then the unit will revert into Free Run until a reference is available. If multiple references are set to the same priority in the priority table, the module will select the lowest reference number as the highest priority. For example, if Reference 5 and Reference 3 are both set to priority 1, the module will consider Reference 3 to be of a higher priority than Reference 5 (assuming both are qualified references).

Autonomous Mode State Diagram
Figure 3



*Note: During autonomous, revertive operation, if a valid reference of a higher priority is available, the module will switch from a reference that is still qualified.

Manual Mode

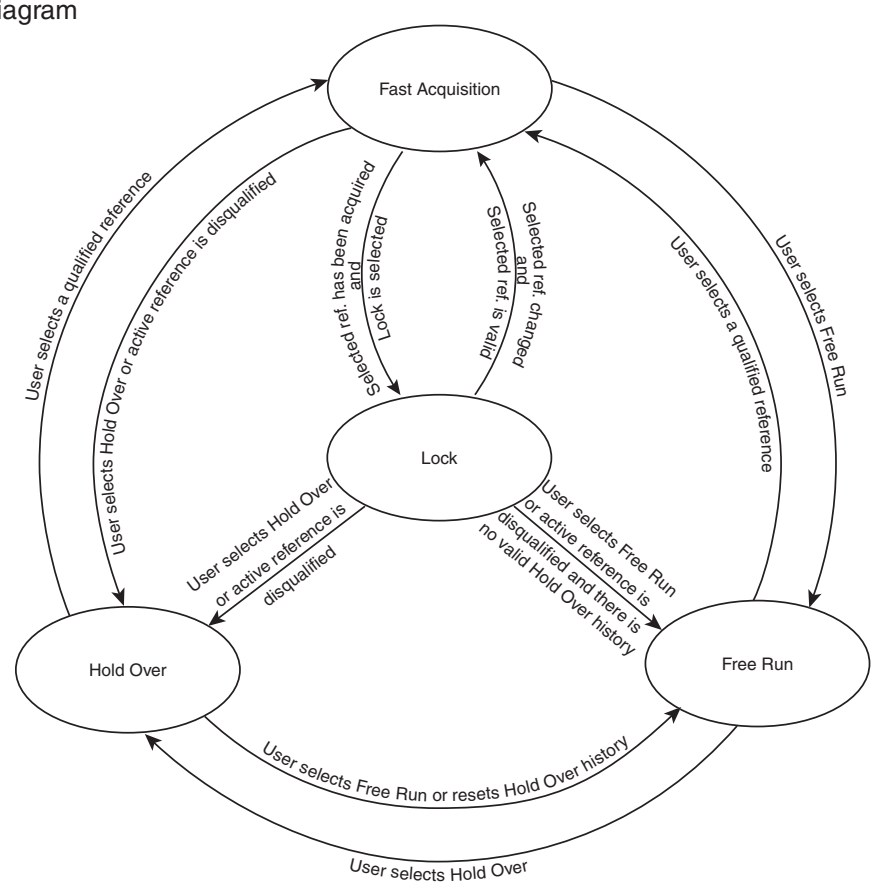
During manual operation, the mode of operation is determined by the user through either the external control pins CNTRL3:1 or internal configuration bits CF3:1 (see Table 7). The default configuration is to have external control, but this can be changed to internal control by setting the INT bit in the memory-mapped registers via the SPI port. During manual operation, the user can select Free Run, Hold Over, or locked operation. Any of the six input references can be selected for the unit to track.

If the module is locked to a reference and that reference becomes disqualified, the module will automatically go into Hold Over. If the module has been phase-locked to the current reference for at least 50 seconds and is in the final stage of the filter (as indicated in register 0Eh), the Hold Over value will be derived from the data from the current reference. If the module has been phase-locked to the current reference for less than 50 seconds, then the last valid Hold Over value will be used. If the control bits/pins remain in the same selection that caused the unit to go into Hold Over, the unit will remain in Hold Over until the reference is re-qualified. At that time, after a minimum 10s soak time, the unit will attempt to relock to the same reference.

If the external user control pins select a new reference that the module has not qualified, the module will switch into the last valid Hold Over value. If the module has not yet established a valid Hold Over, the module will return to the pre-programmed Free Run value. As soon as the module qualifies the selected reference, it will begin the locking process.

At no time during manual mode will the unit attempt to lock to a reference that is not selected by the external pins/internal bits. The only mode that the unit will enter automatically is into Hold Over or Free Run, and that is due to a disqualification of the selected reference.

Manual Mode State Diagram
Figure 4



Master/Slave Operation

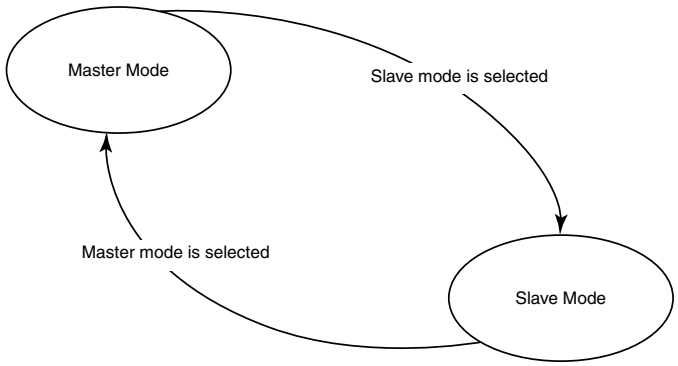
During master operation, the master pays no attention to the Slave Input reference other than monitoring it for qualification purposes. If the slave unit is removed, there is no behavioral change in the master.

During slave operation, the slave module locks to the Slave Input reference from the master, and continually qualifies it. If the slave module determines that the master input has gone out of range, the slave continues to lock to the master until it reaches the end of its pull-in/hold-in range, which is approximately ±125 ppm. If the slave determines that the Slave Input frequency from the master has been removed, the slave will use its internal priority table (which should be configured the same as the master module) and configuration registers to begin locking to the highest priority qualified reference (or to the selected input reference if the master unit was in manual mode). As soon as the Slave Input from the master returns, (after a 10 sec. minimum soak time) the slave will begin locking to it.

When the module is in slave mode, the external indicator pins (Reference 1-Reference 6, Free Run, Hold Over) will remain low, regardless of the mode. If the module is locked to or is attempting to lock to the master, the alarm indicator will be low. The $\overline{\text{LOCK}}$ alarm works normally as long as the module is tracking the master. If the master is lost (due to LOR or out of tracking range), and the module enters another mode, the alarm and $\overline{\text{LOCK}}$ indicators will both remain high (=1). The internal PLL status register (0Eh) must be read to determine the current mode of operation of the module.

The goal of the slave is to maintain a zero-phase error with the Slave Input from the master. In order to accomplish this, the BW during slave mode is increased so that the slave can respond very quickly to any change in the master's frequency to minimize the phase difference between master and slave.

Master/Slave State Diagram
Figure 5

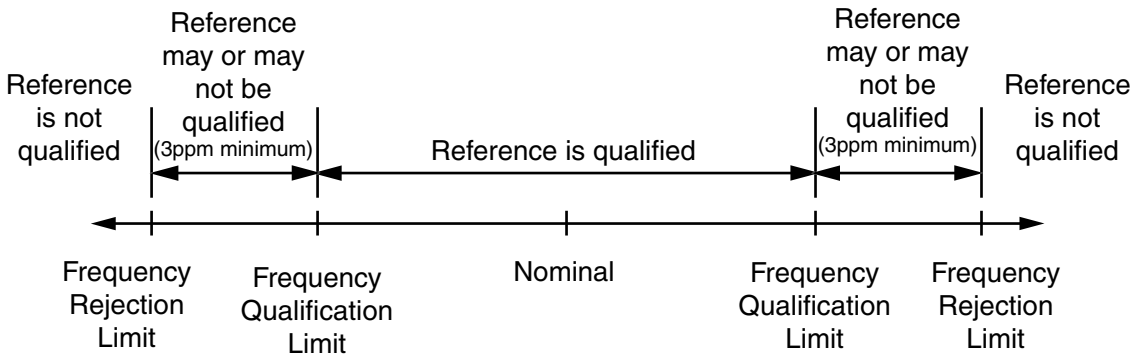


Reference Qualification

Reference qualification requires that a reference be both present and within the required frequency limits for a minimum of 10 seconds. Any time a reference is disqualified due to a loss of signal or frequency offset, the 10 second window will start over. The active reference can also be disqualified if there is a phase-time movement on the input that is greater than the allowable movement for jitter tolerance and frequency hold-in range. If active reference is disqualified due to a faster than allowed phase-time change (phase hit), the module will immediately go into Hold Over (or Free Run if Hold Over is not valid) for a minimum of 2ms, after which the module will act as though the reference was disqualified due to a LOR or off-frequency condition.

Reference Frequency Qualification Test

Figure 6



SPI Timing and Operation

The SPI port is set up for 8 bit communication. All address bytes are 8 bits in length, reads return 8 bits and writes require 8 bits. The MSB of each address byte is the read/write bit. The lower 7 bits are the lowest 7 bits of the specified address. For example, a read from address 01h would require the byte 1000 0001b to be sent to the module, MSB first.

Table 9

A7	A6	A5	A4	A3	A2	A1	A0
R/W	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit0

Format for Address Byte
R/W: Read=1/Write=0
Bit 6 - Bit 0: Address Information
Send A7 First

Table 10

D7	D6	D5	D4	D3	D2	D1	D0
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0

Format for Data Byte
Bit 7 - Bit 0: Data Information
Receive/Send D7 First

SPI Timing Diagrams

Figure 7

Write Cycle

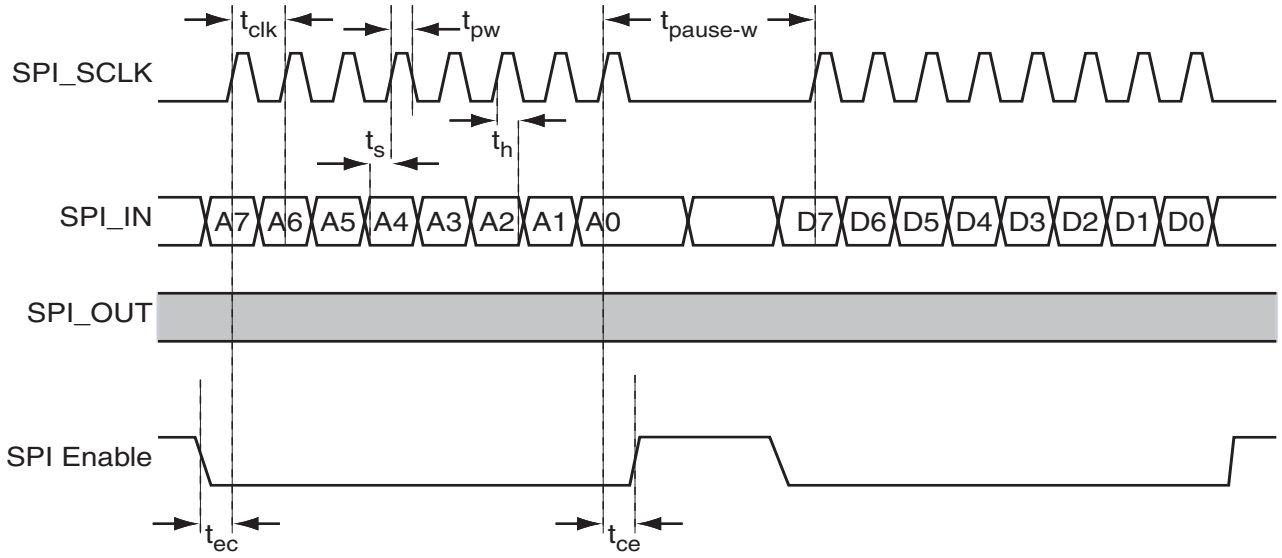
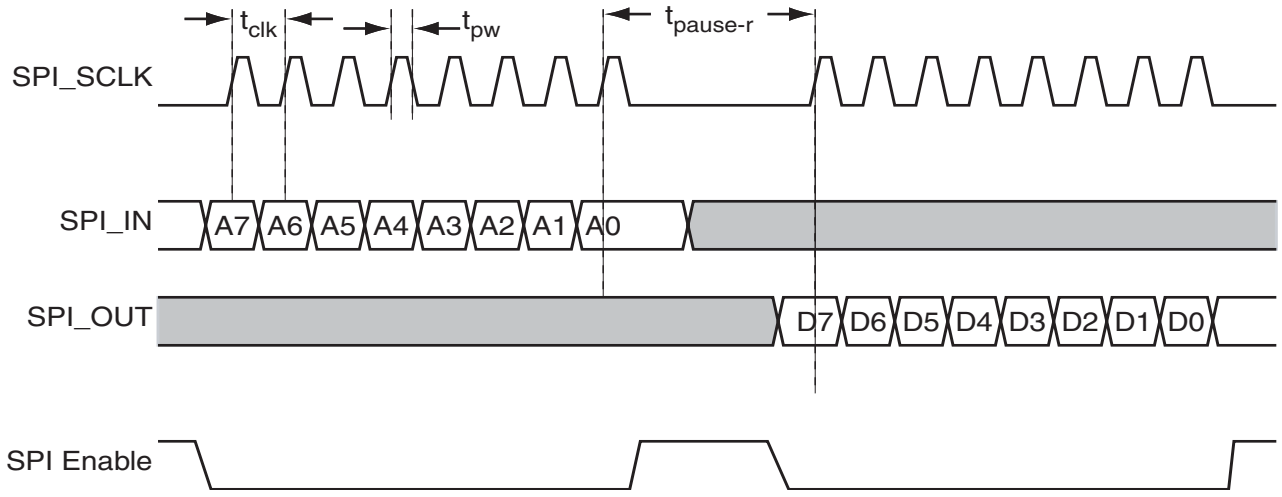


Figure 8

Read Cycle



***See tables 9 & 10 for specific Bit information.**

Parameter	Description	Min	Max
t_{CLK}	SPI CLK rising edge to SPI CLK rising edge	100 ns	
t_S	Setup time, Valid data to SPI CLK rising edge	10 ns	
t_h	Hold time, Valid data following SPI CLK rising edge	1 ns	
$t_{pause-w}$	Minimum time between address and data byte, Write only	1 s	
$t_{pause-r}$	Minimum time between address and data byte, Read only	1 ms	
t_{ec}	Setup time, $\overline{\text{SPI Enable}}$ to first SPI CLK rising edge	(t_{CLK}/2)	
t_{ce}	Hold time, $\overline{\text{SPI Enable}}$ following last SPI CLK rising edge	(t_{CLK}/2)	
t_{pw}	Pulse width, SPI CLK	(t_{CLK}/2) - 10 ns	

SPI Memory Mapped Registers

The internal memory-mapped registers are accessible through the SPI port on the STL module. Some registers are read-only, while others are are accessible for a read or a write operation. The registers contain status information, alarm information, configuration tables, and ID registers. To access the registers, please see the read and write timing diagrams in Figures 7-8.

Table 11 - Register Map

Addrs	Description
00h 01h 02h	Priority Selection Table
03h	Reserved
04h 05h 06h 07h 08h 09h	Reference Measurement
0Ah	Slave Reference Measurement
0Bh	Reserved
0Ch 0Dh	Qualification Status for References and Slave Input
0Eh	Phase-Locked Loop Status
0Fh	Reserved
10h 11h	Reference Qualification Limits
12h 13h	Configuration
14h 15h	Reserved
16h 17h	Bandwidth Selection
18h	SPI Status
19h 1Ah 1Bh	Identification
1Ch	Reserved

Table 12 - Priority Selection Table
Read/Write

Addrs	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Description
00h	P23	P22	P21	P20	P13	P12	P11	P10	Priority register for References 1 and 2
01h	P43	P42	P41	P40	P33	P32	P31	P30	Priority register for References 3 and 4
02h	P63	P62	P61	P60	P53	P52	P51	P50	Priority register for References 5 and 6

P13,P12,P11,P10 - Priority for Reference 1(Default - 0110)
P23,P22,P21,P20 - Priority for Reference 2(Default - 0101)
P33,P32,P31,P30 - Priority for Reference 3(Default - 0100)
P43,P42,P41,P40 - Priority for Reference 4(Default - 0011)
P53,P52,P51,P50 - Priority for Reference 5(Default - 0010)
P63,P62,P61,P60 - Priority for Reference 6(Default - 0001)

The Priority Selection Table registers contain default information on the priority of the references, but these registers can be overwritten by the user. The lowest priority is 0000 and the highest priority is 0110. If a reference is given priority 0000, then that reference will be evaluated for frequency and presence, but will be considered an unavailable reference in autonomous mode.

If multiple references are assigned the same priority, and the module is in autonomous, revertive mode, the module will select the lowest reference number as the highest priority.

All priorities with a binary number greater than 0110 will be treated as though their priority was 0110. No 4-bit binary combinations will be considered invalid.

Table 13 - Reference Measurement and Qualification Status

Read only

Addrs	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Description
04h	F17	F16	F15	F14	F13	F12	F11	F10	Reference 1 Frequency offset from Free Run
05h	F27	F26	F25	F24	F23	F22	F21	F20	Reference 2 Frequency offset from Free Run
06h	F37	F36	F35	F34	F33	F32	F31	F30	Reference 3 Frequency offset from Free Run
07h	F47	F46	F45	F44	F43	F42	F41	F40	Reference 4 Frequency offset from Free Run
08h	F57	F56	F55	F54	F53	F52	F51	F50	Reference 5 Frequency offset from Free Run
09h	F67	F66	F65	F64	F63	F62	F61	F60	Reference 6 Frequency offset from Free Run
0Ah	FS7	FS6	FS5	FS4	FS3	FS2	FS1	FS0	Slave Input frequency offset from Free Run
0Ch	R41	R40	R31	R30	R21	R20	R11	R10	Status indicators for References 1-4
0Dh	X	X	RS1	RS0	R61	R60	R51	R50	Status indicators for References 5-6

Fx7,Fx6,Fx5,Fx4,Fx3,Fx2,Fx1,Fx0 - Frequency offset of Reference x (Default - 1111 1111)

R#1,R#0 - Describes status of Reference #, see Table 20 (Default - 00)

X - Reserved for future use (Default - 0)

The Reference Measurement and Qualification Status registers hold the information regarding the specified reference's frequency offset from nominal (accurate to within 1.5 ppm of actual frequency) and status information regarding presence and qualification status. The Frequency Offset registers have a resolution of 0.5 ppm, and are in 2s complement form. A maximum frequency offset of +63.5 ppm or -64 ppm can be shown in these registers. If a reference is determined to have a frequency offset past these limits, the register will only show the maximum. The Status Indicator registers show qualification status of each reference.

Table 14 - Phase-Locked Loop Status

Read only

Addrs	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Description
0Eh	HA	R2	R1	R0	S3	S2	S1	S0	Reference used in PLL and PLL Status

HA = 1 when Holdover history is available (Default - 0)

R2,R1,R0 - Describes reference in use, see Table 21 (Default - 000)

S3,S2,S1,S0 - Describes state of PLL, see Table 22 (Default - 1001)

Bit HA=1 when holdover history for the current reference is available. It will remain high when switched directly from the current reference into holdover mode. Changing references, switching into free run, or setting the HOR bit in register 13h will clear the HA bit. However, the valid holdover history will remain in the module's memory until it is either overwritten by history from a new reference, or until it is cleared by HOR.

When the module detects a 3.4 μ second phase-time change in 0.1s, it is unable to determine whether this is an actual phase hit or a 34 ppm (or higher) frequency step. If phase build out is triggered due to a 34 ppm (or higher) frequency step, the module will go into continuous phase build out. As the phase of the new frequency varies with the phase of the internal reference from 0 degrees to 359 degrees and then back to 0, the phase build out bit in the pll status register (0Eh) will blink. The frequency of this blinking will depend on the actual size of the frequency step

To prevent the module from going into a continuous phase build out state, do not attempt a 34 ppm (or greater) frequency step unless phase build out is disabled.

Table 15 - Reference Qualification Limits

Read/Write

Addrs	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Description
10h	RJ7	RJ6	RJ5	RJ4	RJ3	RJ2	RJ1	RJ0	Frequency rejection limit
11h	FQ7	FQ6	FQ5	FQ4	FQ3	FQ2	FQ1	FQ0	Frequency qualification limit

RJ7,RJ6,RJ5,RJ4,RJ3,RJ2,RJ1,RJ0 - Limit beyond which references always rejected (Default - 0001 1111 (+/-15.5 ppm))

FQ7,FQ6,FQ5,FQ4,FQ3,FQ2,FQ1,FQ0 - Limit below which references always qualified (Default - 0001 1001 (+/-12.5 ppm))

The Reference Qualification Limits registers hold the information used to determine the always reject and always qualify regions for the references. For proper module operation, the minimum space between these numbers should be 3 ppm. The LSB of each of these registers is 0.5 ppm, and the MSB is 64 ppm, so the max number is 127.5 ppm. The format is 2s complement, positive numbers. Note that the qualification and rejection ranges are symmetrical so that +15.5 ppm in register 10h gives a frequency rejection limit at + or - 15.5 ppm. See Figure 6 for further details.

Table 16 - Configuration

Read/Write

Addrs	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Description
12h	INT	X	X	SLV	X	CF3	CF2	CF1	Mode configuration register
13h	X	X	DPB	FRV	RST	HOR	REV	AUT	Feature configuration register

INT - When set to 1, INT selects internal user configuration data over the external CNFG pins. (Default - 0)

SLV - When set to 1, the module is in slave mode. (Default - 0)

CF3,CF2,CF1 - Internal configuration pins, see Table 7 (Default - 000)

DPB - When set to 1, Phase Build Out is disabled. (Default - 1)

FRV - When set to 1, will choose priority of reference based on frequency offset rather than priority table. (Default - 0)

RST - Will internally reset the module when set to 1. (Default - 0)

HOR - Will reset Hold Over history when set to 1. Holdover history defaults to Free Run value when reset. (Default - 0)

REV - Selects revertive reference switching when set to 1. Revertive switching only occurs while in autonomous mode. (Default - 0)

AUT - Select pin for autonomous mode. When set to 1, enables autonomous selection of modes. (Default - 0)

X - Reserved for future use. (Default - 0)

The Configuration registers are read/write registers that hold all of the configuration options for the device. If INT is set high, the external pins CNTRL3:1 are ignored, and full user control is maintained through these two registers. Bits CF3:1 mimic pins CNTRL3:1 operation, and SLV bit in the mode configuration register controls whether the unit acts as a master or slave module. For complete master/slave operation, see Figure 5. The feature configuration register turns on and off optional features of the device such as phase build out, revertive switching, and autonomous operation. Bits are also provided to judge priority of references (applicable during autonomous mode only) based on their frequency offset (see registers 04h-09h) or on the priority table (see registers 00h-02h). The module also allows a reset of Hold Over history (HOR), as well as a complete module reset (RST).

The RST bit is used to initiate a complete software reset. The proper procedure to reset the device is to write a 1 to RST and then wait for the device to re-boot. This will reset the DSP, as well as the FPGA and DDS. Due to the complete reset, the output frequencies will be temporarily disrupted while the programmable chips reinitialize and then the Free Run value will be reestablished. All previous histories will be cleared. The registers will initialize as though following a power-up. Please note that there will be an increase in current as the device reinitializes, but the current increase will stay below the stated datasheet maximum.

For optimal performance during master/slave operation, the slave unit should be configured the same as the master unit. This will allow proper selection of input reference for the slave module in the event the signal from the master module is lost.

Table 17 - Bandwidth Selection

Read/Write

Addrs	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Description
16h	FB3	FB2	FB1	FB0	X	X	X	X	Primary PLL Bandwidth selection
17h	SF3	SF2	SF1	SF0	X	X	X	X	Slave mode Bandwidth selection

FB3,FB2,FB1,FB0 - Selected bandwidth. See Table 23 (Default - 0011)

SF3,SF2,SF1,SF0 - Slave bandwidth. (Default - 0101, 20 Hz)

X - Reserved for future use. (Default - 0)

The bandwidth may be changed at any time during operation, even when the device is locked. However, the module may experience a phase hit as the filters change bandwidth and so it is recommended to only change bandwidth upon initialization, or when in Free Run or Hold Over modes.

If the bandwidth is changed to an undefined selection, no change in operation will occur. The initial bandwidth will remain in effect until a valid new bandwidth is selected.

Slave mode bandwidth selection will take effect only when the unit is configured to be in slave mode. If the Slave Input reference is lost (LOR), and the unit uses its configuration data to determine which reference to lock to, this bandwidth remains the same. The purpose of the slave mode of operation is to lock to the master; if the master is lost, then the next best reference is used.

Table 18 - SPI Status

Read only

Addrs	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Description
18h	ER7	ER6	ER5	ER4	ER3	ER2	ER1	ER0	Error status

ER7,ER6,ER5,ER4,ER3,ER2,ER1 - SPI Error Status. See Table 24 (Default - 0000 0000)

The SPI Status register holds the state of the last SPI communication. An overrun error occurs when too many bytes of information have been sent too quickly and the module was not able to process the address information before the clock started for the data byte. Both reads and writes are invalid if this error follows their communication sequence. If an address error shows up in this register, then the address that was sent to the module was invalid. No read or write will occur in this case. If an invalid address is sent to the module, the module will still expect to see the SPI Enable line active and the SPI CLK line pulsed 8 times before the next read/write cycle. All communication cycles are expected to be 2 bytes wide, whether there is an error or not. If an invalid data error is displayed in the SPI Status register, it means that either a write was attempted on a read-only address, or an invalid data word was written to an address. In either case, no data will be written into memory.

Table 19 - Identification

Read only

Addrs	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Description
19h	CI7	CI6	CI5	CI4	CI3	CI2	CI1	CI0	Customer Identification
1Ah	SI7	SI6	SI5	SI4	SI3	SI2	SI1	SI0	Software Model/Version Identification
1Bh	HI7	HI6	HI5	HI4	HI3	HI2	HI1	HI0	Hardware Model/Version Identification

CI7, CI6, CI5, CI4, CI3, CI2, CI1, CI0 Customer Identification

SI7, SI6, SI5, SI4, SI3, SI2, SI1, SI0 Software Model/Version Identification

HI7, HI6, HI5, HI4, HI3, HI2, HI1, HI0 Hardware Model/Version Identification

Table 20 - Reference Status Table

R#1	R#0	Description
0	0	Reference is not present.
0	1	Reference is present but frequency is disqualified.
1	0	Reference is qualified but is unavailable.*
1	1	Reference is present and frequency is qualified.

* Reference is unavailable in autonomous mode when priority register =0000 for that reference and FRV bit (register 13h) =0

Table 21 - Active Reference Table

R2	R1	R0	Description
0	0	0	No reference. Module is in Free Run or Hold Over
0	0	1	Tracking reference 1
0	1	0	Tracking reference 2
0	1	1	Tracking reference 3
1	0	0	Tracking reference 4
1	0	1	Tracking reference 5
1	1	0	Tracking reference 6
1	1	1	Module is locked to Slave input. (Valid only in Slave mode)

Table 22 - Primary PLL State

S3	S2	S1	S0	Description
0	0	0	0	Loss of Lock
0	0	0	1	Acquisition Filter
0	0	1	0	Future Use
0	0	1	1	Future Use
0	1	0	0	Future Use
0	1	0	1	Future Use
0	1	1	0	Final Filter
0	1	1	1	Phase Build-Out
1	0	0	0	Hold Over
1	0	0	1	Free Run

Table 23 - Bandwidth Selecton

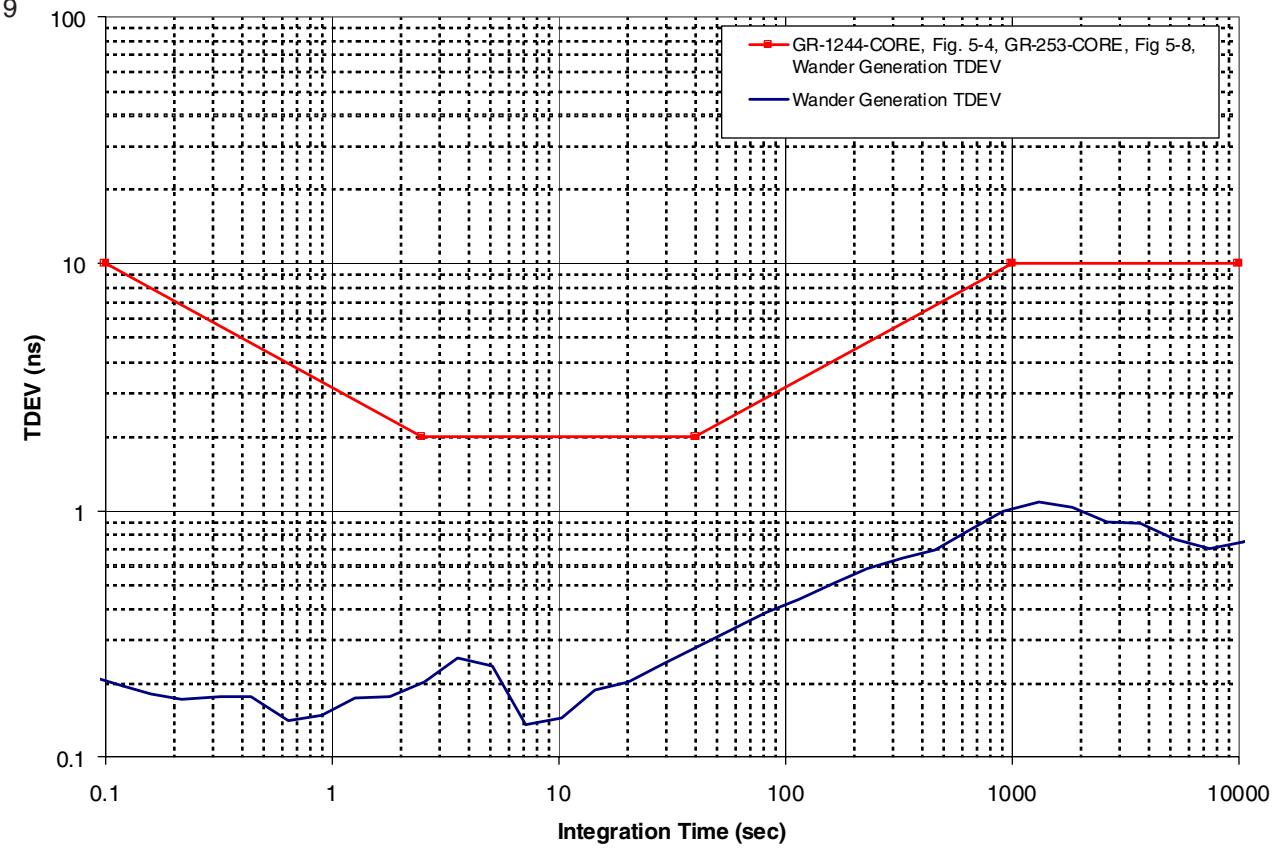
FB3	FB2	FB1	FB0	Description
0	0	1	1	0.1 Hz BW (S3 compatible)

Table 24 - SPI Status

ER7	ER6	ER5	ER4	ER3	ER2	ER1	ER0	SPI Status
0	0	0	0	0	0	0	0	SPI
0	0	0	0	0	0	1	0	SPI overrun error
0	0	0	0	0	0	1	1	SPI address error
0	0	0	0	0	1	0	0	SPI invalid data

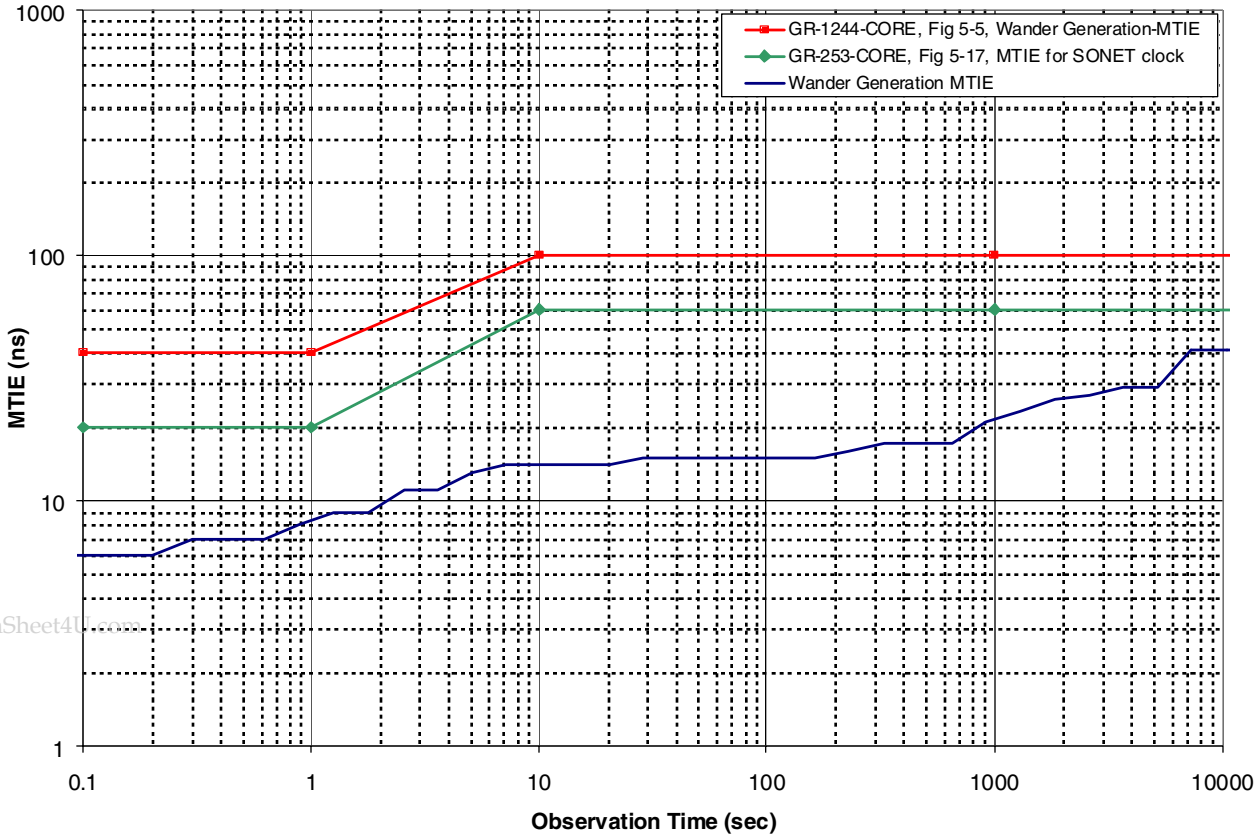
Wander Generation TDEV

Figure 9



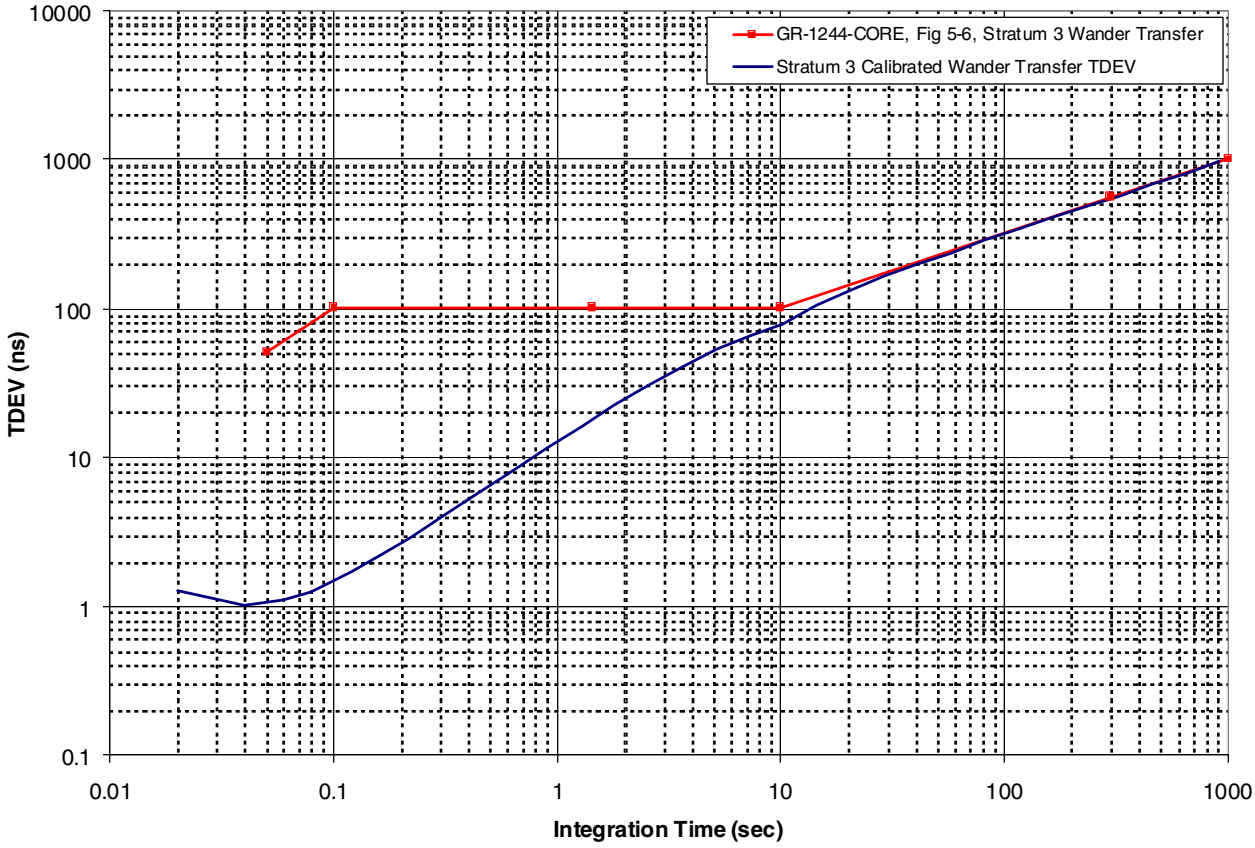
Wander Generation MTIE

Figure 10



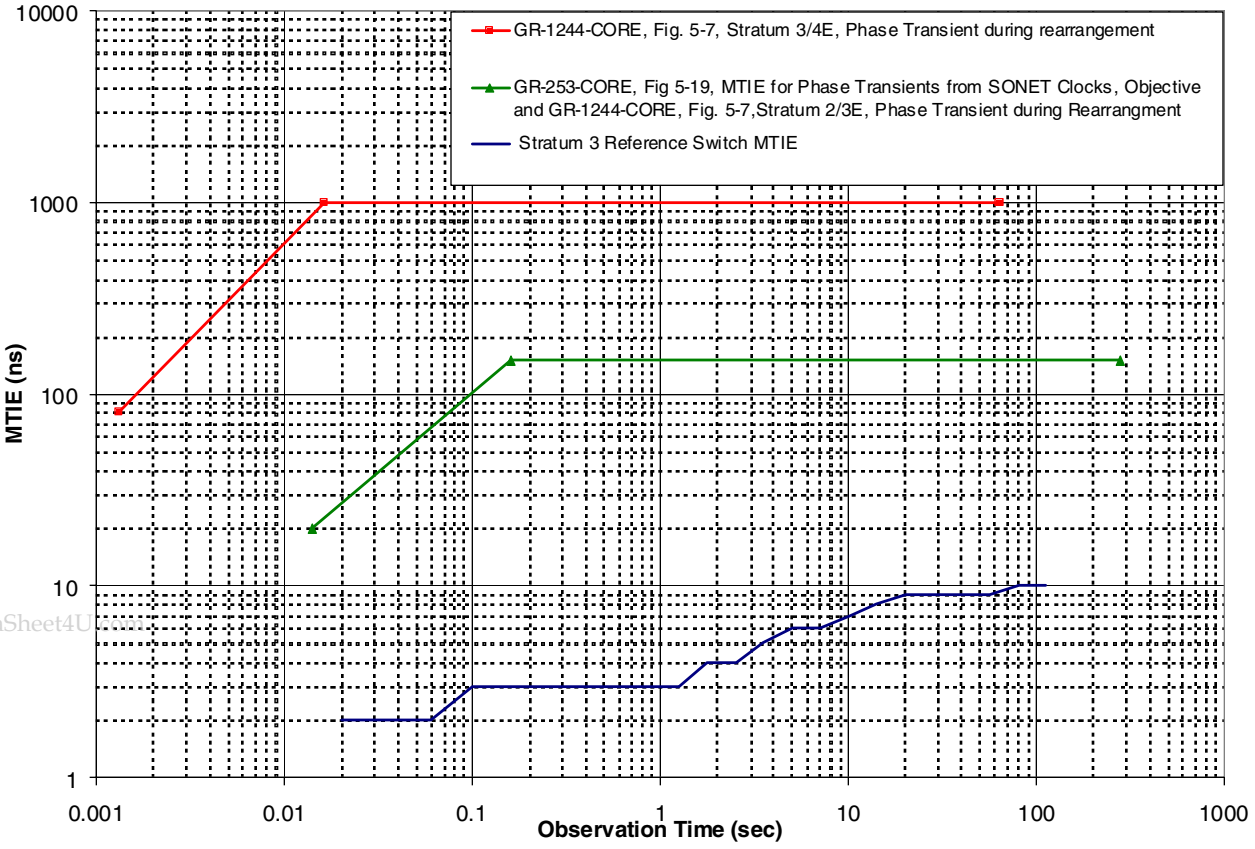
Wander Transfer TDEV

Figure 11



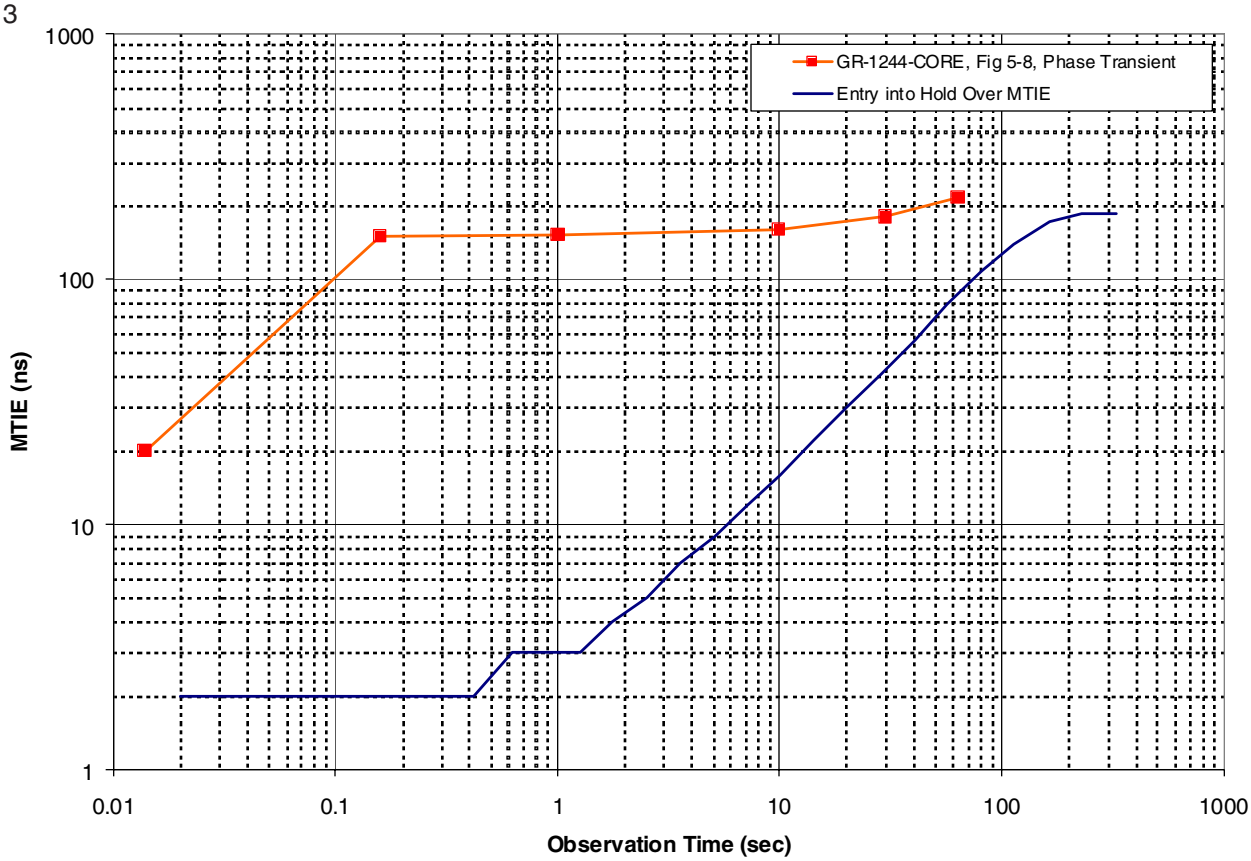
MTIE During Reference Rearrangement

Figure 12



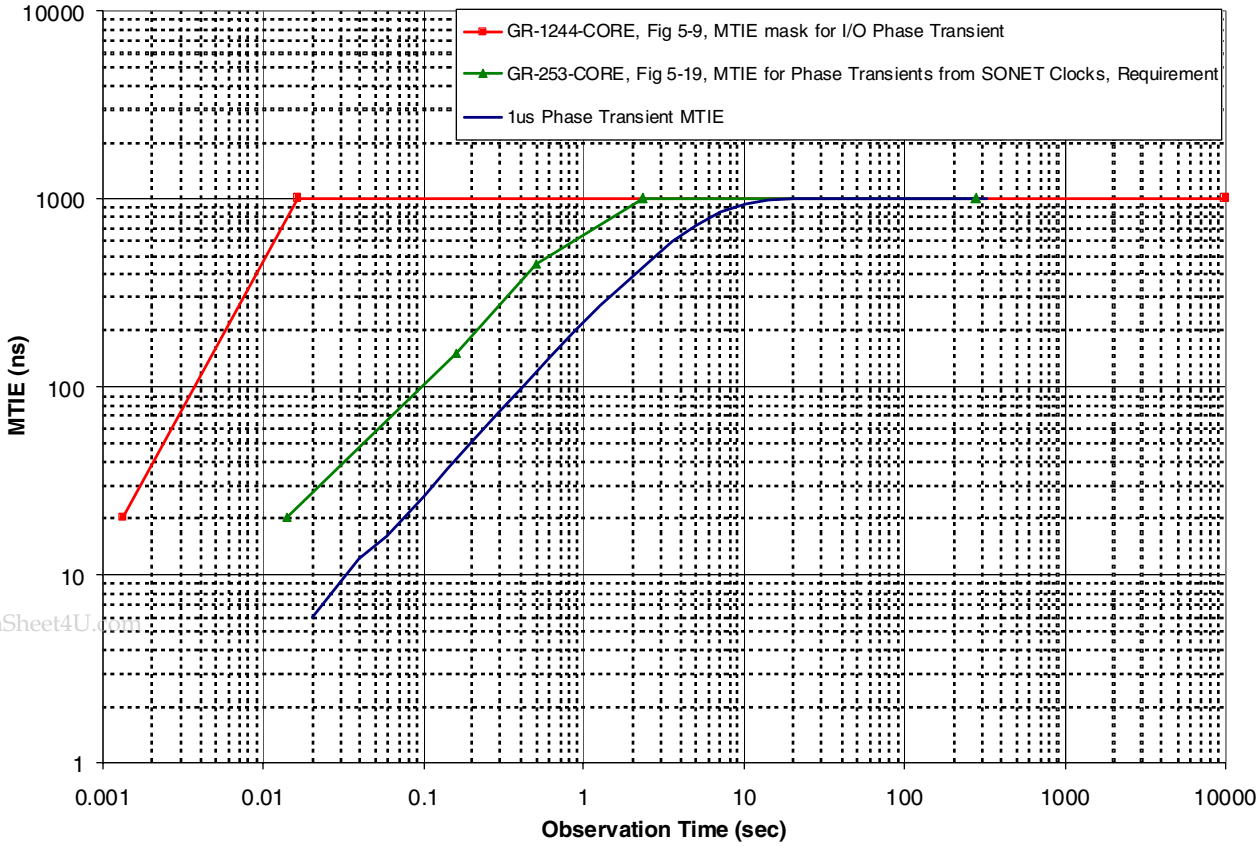
Entry into Hold Over MTIE

Figure 13



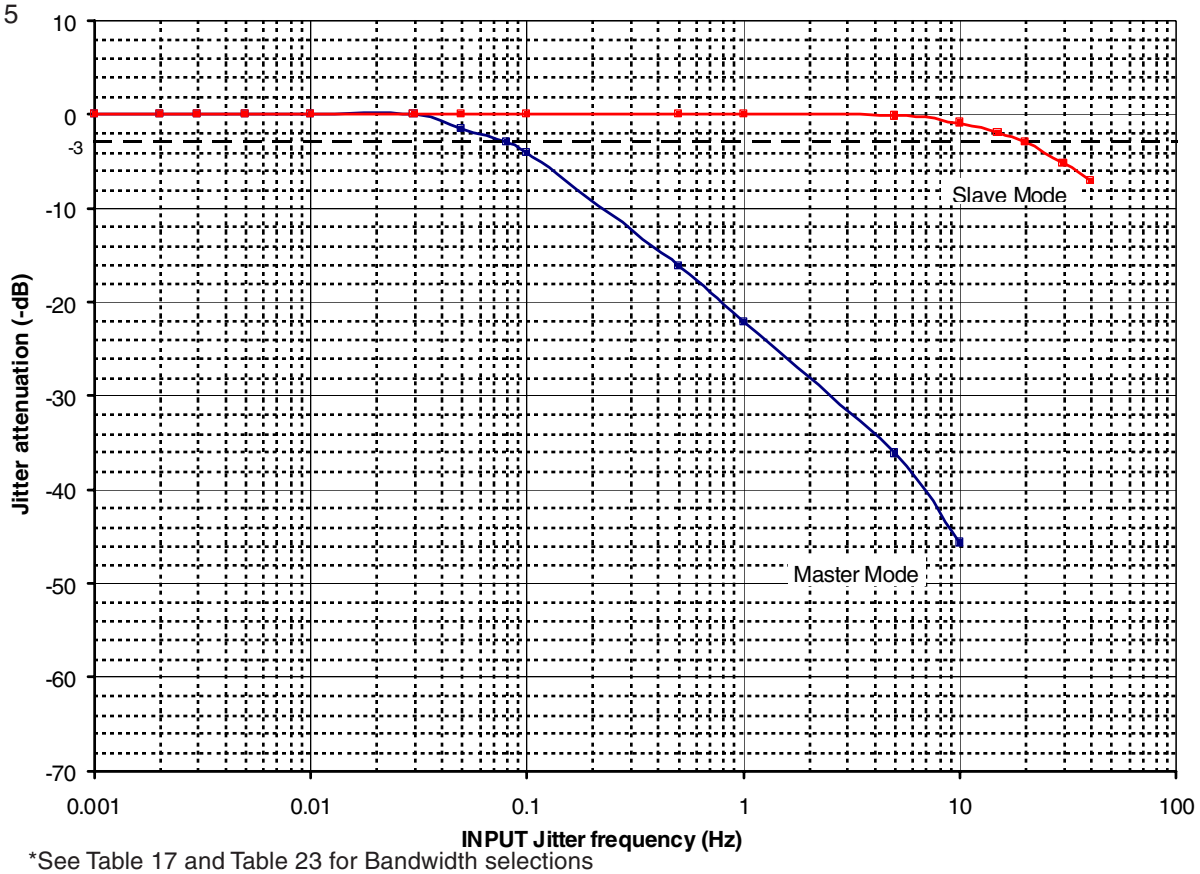
1µs Phase Transient MTIE

Figure 14



Jitter Attenuation

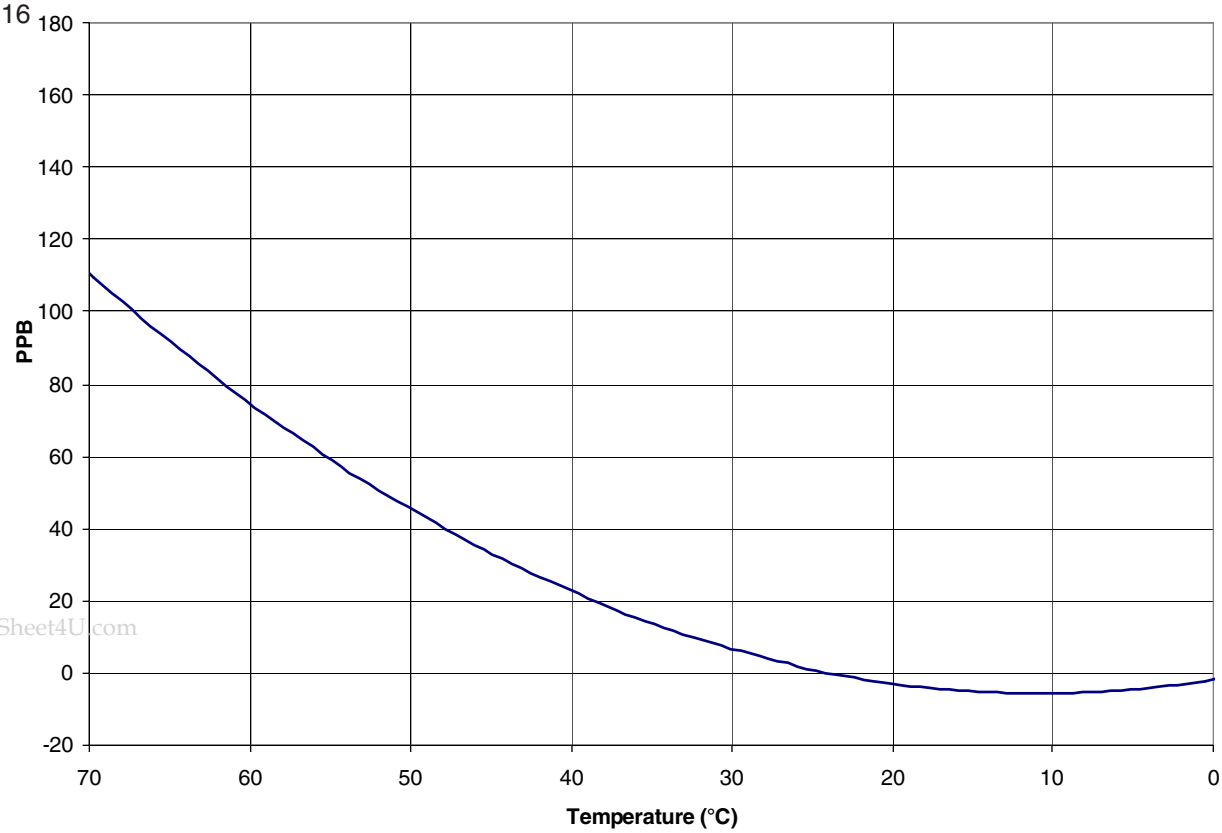
Figure 15



*See Table 17 and Table 23 for Bandwidth selections

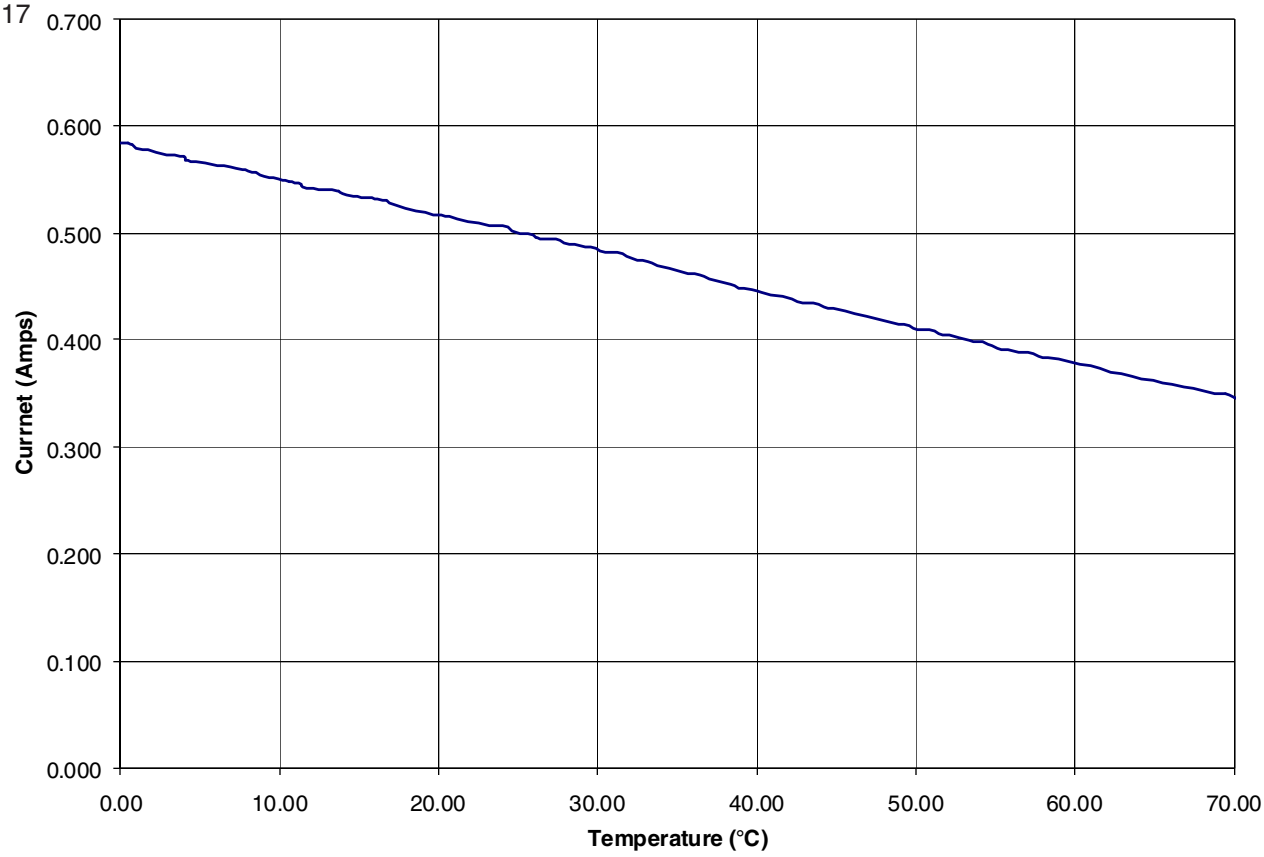
Hold Over Stability over Temperature

Figure 16



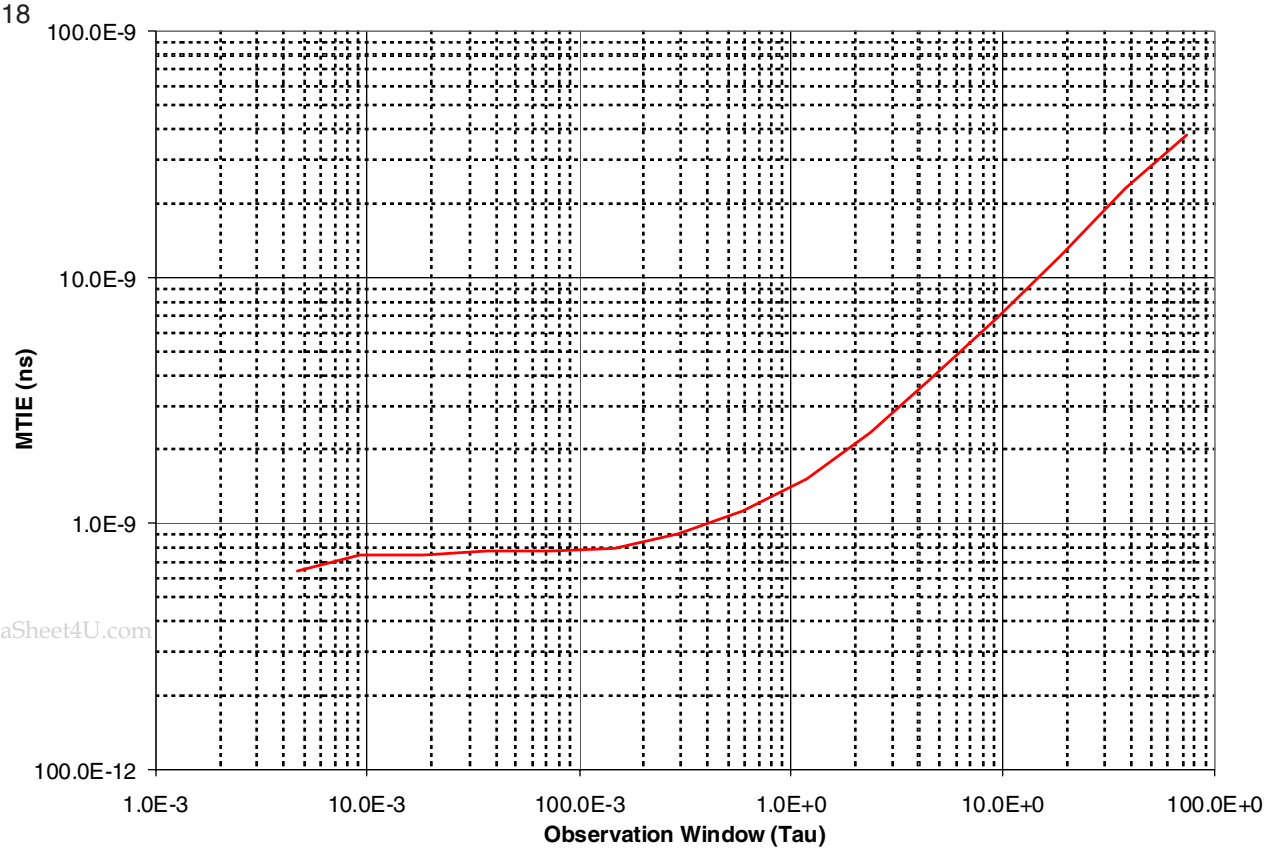
Typical Current Consumption Over Temperature

Figure 17



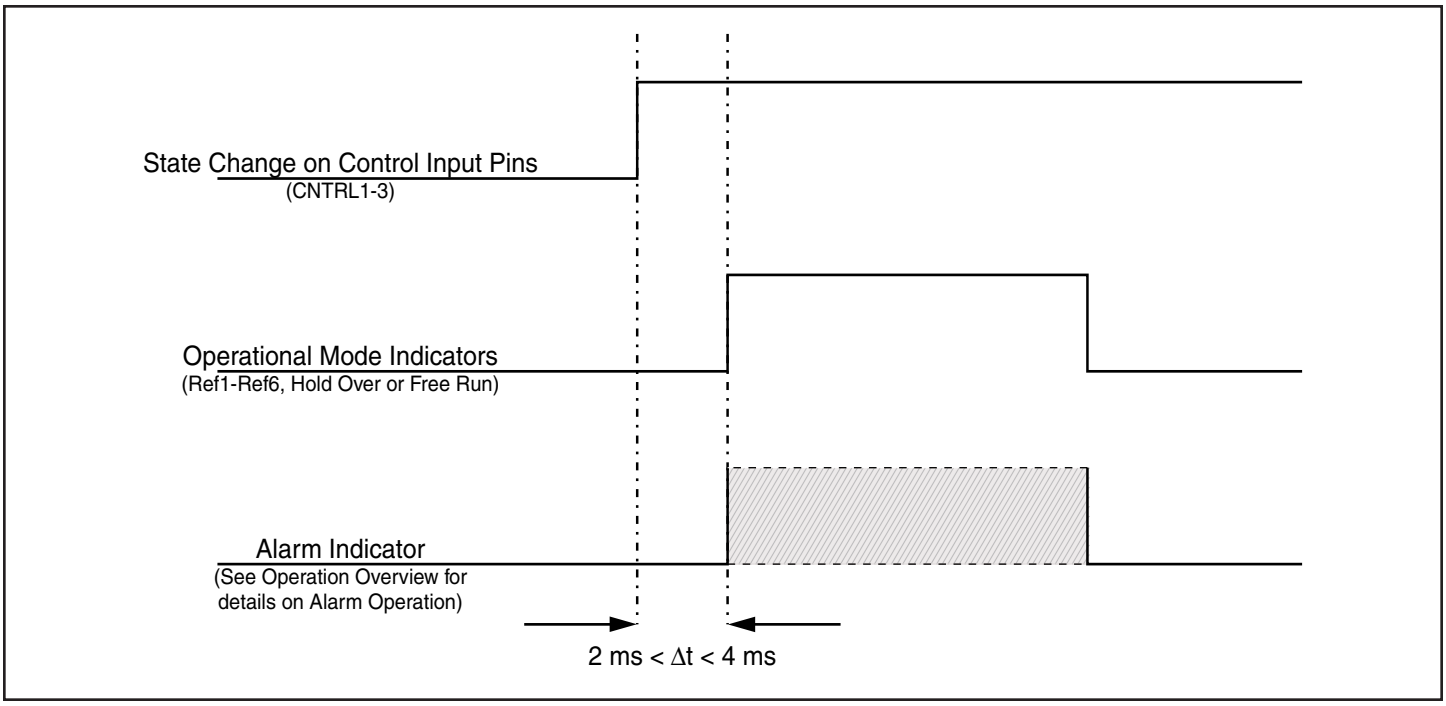
Typical Phase Build Out MTIE (Disabled by default for Stratum 3 compliance)

Figure 18



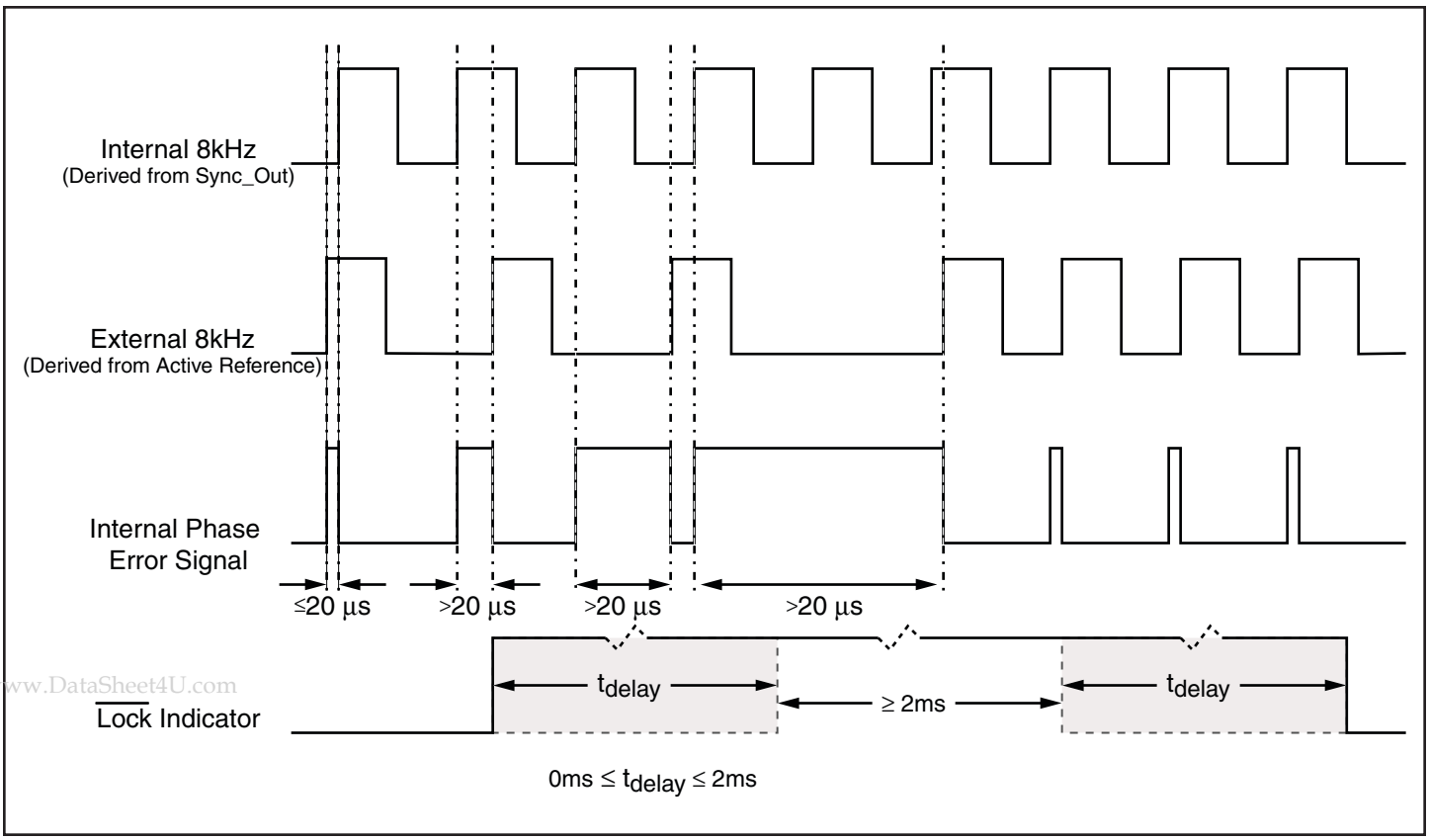
Mode and Alarm Timing Diagram

Figure 19



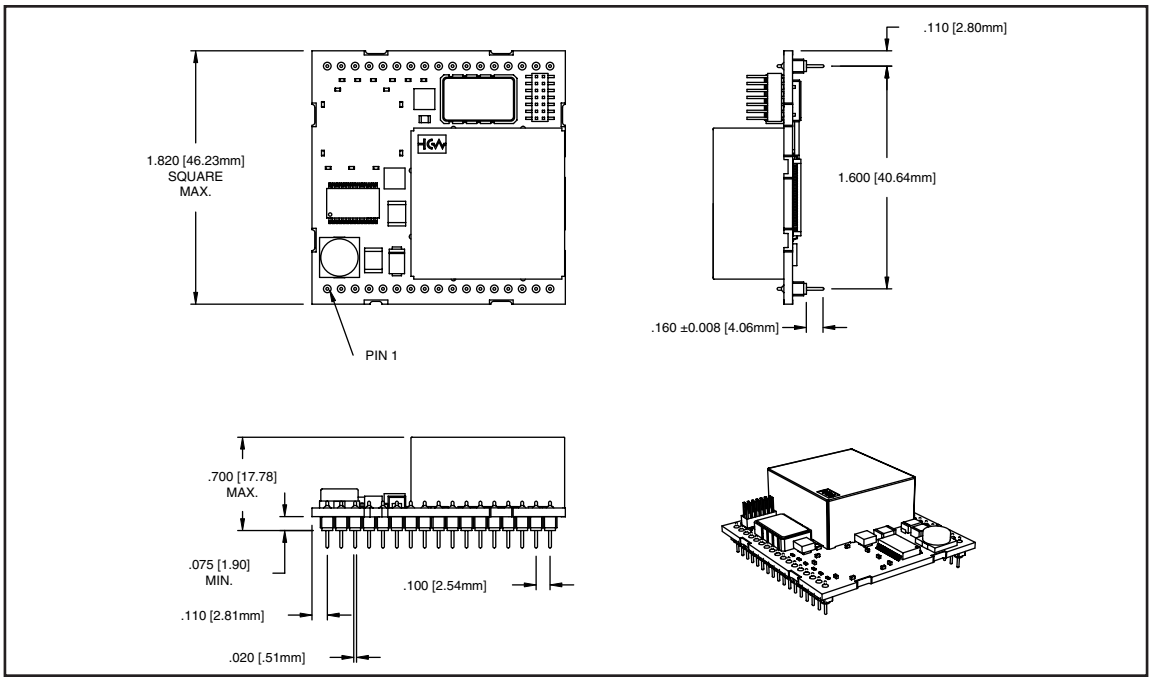
$\overline{\text{LOCK}}$ Timing Diagram

Figure 20



Package Dimensions

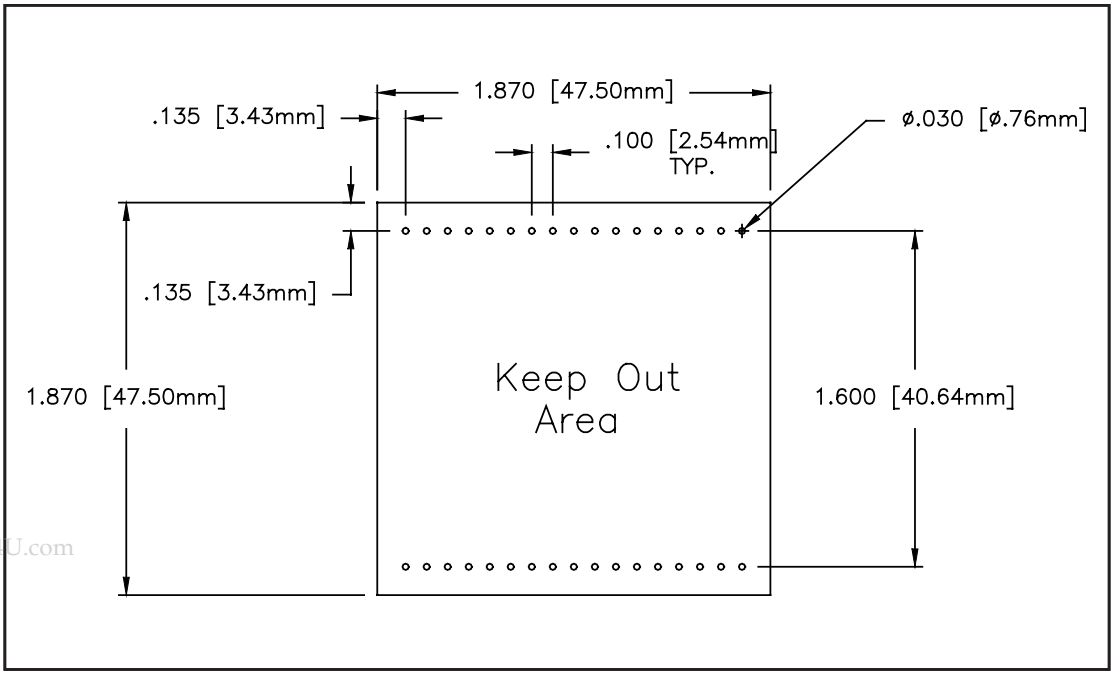
Figure 21



***Please consult the factory for alternate pin connector lengths.**

Footprint and Keepout Dimensions

Figure 22



CONNOR WINFIELD

2111 Comprehensive Drive
Aurora, Illinois 60505
Phone: 630-851-4722
Fax: 630-851-5040
www.conwin.com

Revision #	Revision Date	Notes
P00	05/17/04	Preliminary informational release