



STL16N1VH5

N-channel 12 V, 0.0022 Ω , 16 A, PowerFLAT™ (3.3 x 3.3)
STripFET™ V Power MOSFET

Features

Order code	V _{DSS}	R _{DS(on) max}	I _D
STL16N1VH5	12 V	0.003 Ω	16 A ⁽¹⁾

1. The value is rated according R_{thj-pcb}

- Improved die-to-footprint ratio
- Very low profile package (1mm max)
- Very low thermal resistance
- Very low gate charge
- Very low on-resistance
- Optimized to be driven @ 2.5 V
- In compliance with the 2002/95/EC European directive

Applications

- Switching applications

Description

This device is an N-channel Power MOSFET developed using STMicroelectronics' STripFET™V technology. The device has been optimized to achieve very low on-state resistance, contributing to an FOM that is among the best in its class.

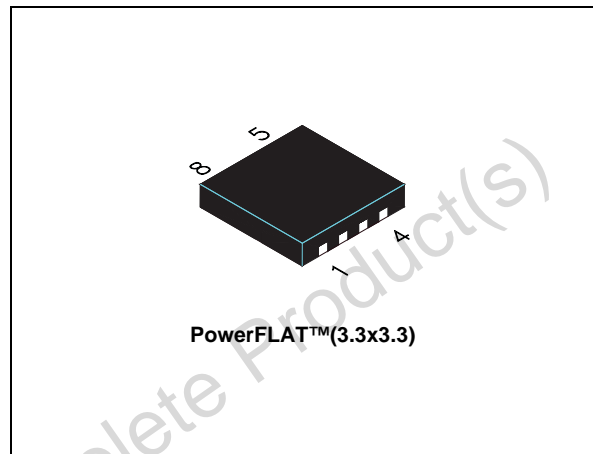


Figure 1. Internal schematic diagram

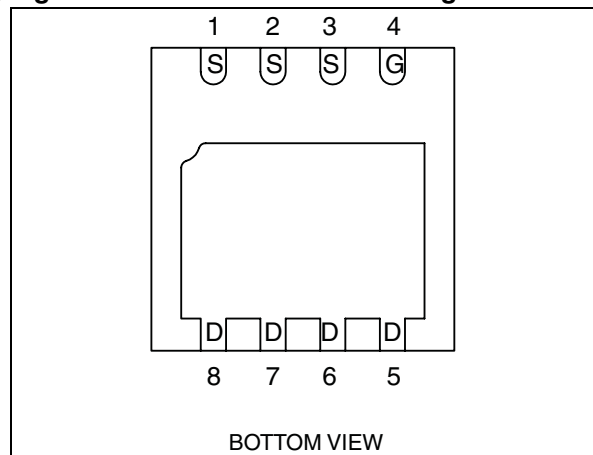


Table 1. Device summary

Order code	Marking	Package	Packaging
STL16N1VH5	16N1V	PowerFLAT™ (3.3 x 3.3)	Tape and reel

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Obsolete Product(s) - Obsolete Product(s)

1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage ($V_{GS} = 0$)	12	V
V_{GS}	Gate-source voltage	± 8	V
$I_D^{(1)}$	Drain current (continuous) at $T_C = 25\text{ }^\circ\text{C}$	16	A
$I_D^{(1)}$	Drain current (continuous) at $T_C = 100\text{ }^\circ\text{C}$	10	A
$I_{DM}^{(2)}$	Drain current (pulsed)	64	A
$P_{TOT}^{(3)}$	Total dissipation at $T_C = 25\text{ }^\circ\text{C}$	50	W
$P_{TOT}^{(1)}$	Total dissipation at $T_C = 25\text{ }^\circ\text{C}$	2	W
	Derating factor	0.4	W/ $^\circ\text{C}$
T_J T_{stg}	Operating junction temperature storage temperature	-55 to 150	$^\circ\text{C}$

1. The value is rated according to $R_{thj-pcb}$
2. Pulse width limited by safe operating area.
3. The value is rated according R_{thj-c}

Table 3. Thermal resistance

Symbol	Parameter	Value	Unit
$R_{thj-case}$	Thermal resistance junction-case (drain)	2.5	$^\circ\text{C}/\text{W}$
$R_{thj-pcb}^{(1)}$	Thermal resistance junction-pcb	42.8	$^\circ\text{C}/\text{W}$
$R_{thj-pcb}^{(2)}$	Thermal resistance junction-pcb	63.5	$^\circ\text{C}/\text{W}$

1. When mounted on FR-4 board of 1inch², 2oz Cu, $t < 10\text{sec}$
2. Steady state

Table 4. Avalanche data

Symbol	Parameter	Value	Unit
I_{AV}	Not-repetitive avalanche current (pulse width limited by $T_J \text{ Max}$)	11	A
E_{AS}	Single pulse avalanche energy (starting $T_J = 25\text{ }^\circ\text{C}$, $I_D = I_{AV}$, $V_{DD} = 12\text{ V}$, $L = 6\text{ mH}$)	350	mJ

2 Electrical characteristics

($T_{CASE}=25^{\circ}C$ unless otherwise specified)

Table 5. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$I_D = 250 \mu A, V_{GS} = 0$	12			V
I_{DSS}	Zero gate voltage drain current ($V_{GS} = 0$)	$V_{DS} = \text{Max rating},$ $V_{DS} = \text{Max rating} @ 125^{\circ}C$			1 10	μA μA
I_{GSS}	Gate body leakage current ($V_{DS} = 0$)	$V_{GS} = \pm 8 V$			± 100	nA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}, I_D = 250 \mu A$	0.5			V
$R_{DS(on)}$	Static drain-source on resistance	$V_{GS} = 4.5 V, I_D = 8 A$ $V_{GS} = 2.5 V, I_D = 8 A$		0.0022 0.0032	0.003 0.004	Ω Ω

Table 6. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	$V_{DS} = 12 V, f = 1 \text{ MHz},$ $V_{GS} = 0$	-	2085	-	pF
C_{oss}	Output capacitance			949		
C_{rss}	Reverse transfer capacitance			240		
Q_g	Total gate charge	$V_{DD} = 12 V, I_D = 16 A$	-	26.5	-	nC
Q_{gs}	Gate-source charge	$V_{GS} = 4.5 V$		5.2		
Q_{gd}	Gate-drain charge (see Figure 14)			4.8		
R_G	Gate input resistance	$f = 1 \text{ MHz}$ Gate DC Bias = 0 Test signal level = 20mV Open drain	-	1.5	-	Ω

Table 7. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD}=6\text{ V}$, $I_D=8\text{ A}$, $R_G=4.7\ \Omega$, $V_{GS}=4.5\text{ V}$ <i>(see Figure 13)</i>	-	14.4	-	ns
t_r	Rise time			31.6		ns
$t_{d(off)}$	Turn-off delay time			50		ns
t_f	Fall time			16		ns

Table 8. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		16	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)		-		64	A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD}=16\text{ A}$, $V_{GS}=0$	-		1.1	V
t_{rr}	Reverse recovery time	$I_{SD}=16\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$, $V_{DD}=10\text{ V}$, $T_j=150\text{ }^\circ\text{C}$ <i>(see Figure 18)</i>	-	49		ns
Q_{rr}	Reverse recovery charge			54		nC
I_{RRM}	Reverse recovery current			2.2		A

1. Pulse width limited by safe operating area
2. Pulsed: pulse duration= 300 μs , duty cycle 1.5%

2.1 Electrical characteristics (curves)

Figure 2. Safe operating area

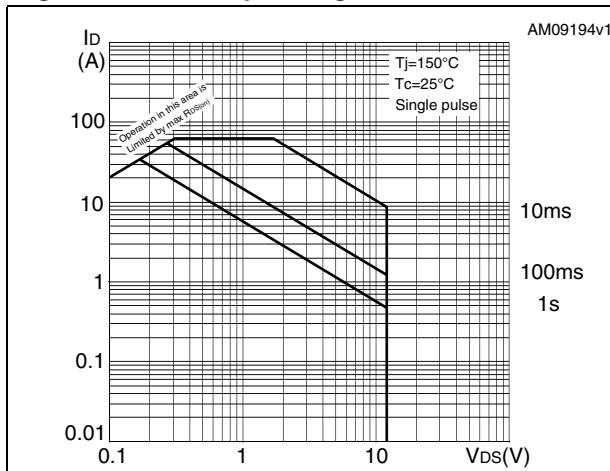


Figure 3. Thermal impedance

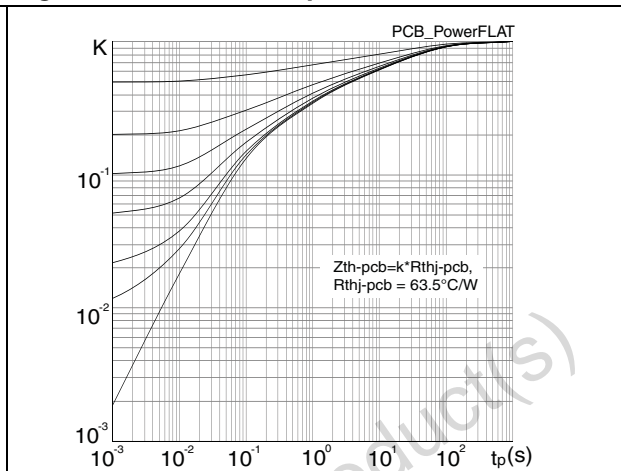


Figure 4. Output characteristics

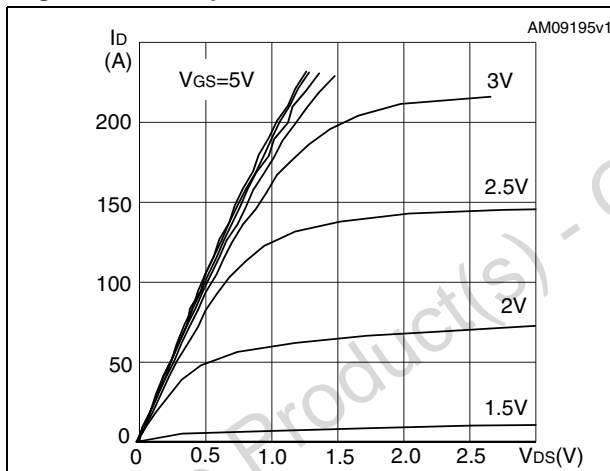


Figure 5. Transfer characteristics

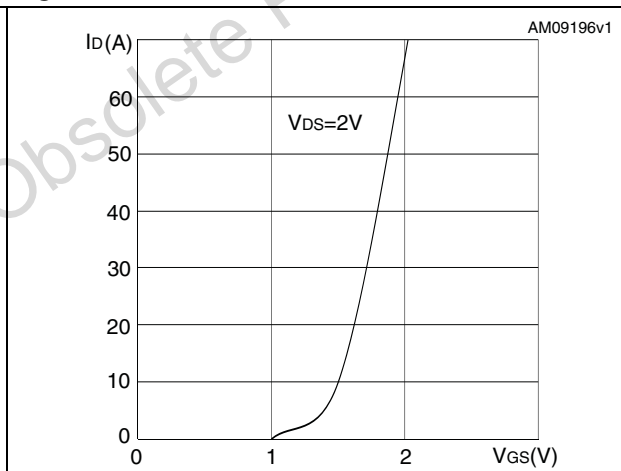


Figure 6. Normalized $B_{V_{DSS}}$ vs temperature

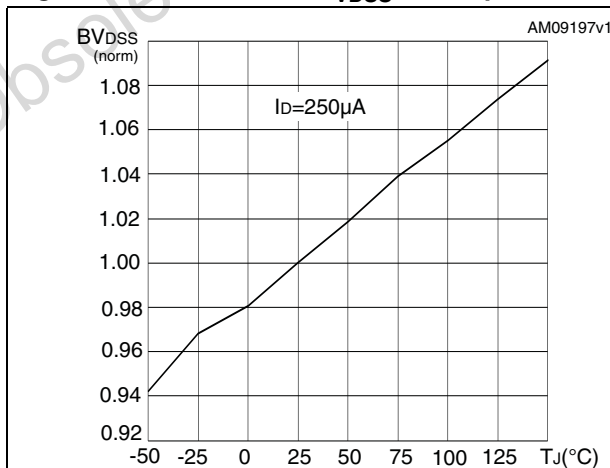


Figure 7. Static drain-source on resistance

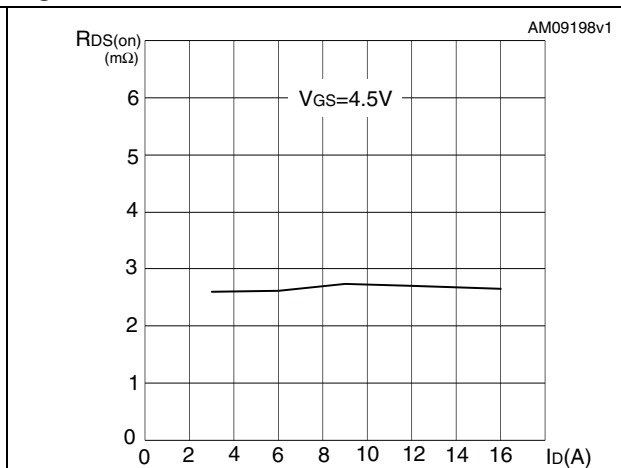


Figure 8. Gate charge vs gate-source voltage Figure 9. Capacitance variations

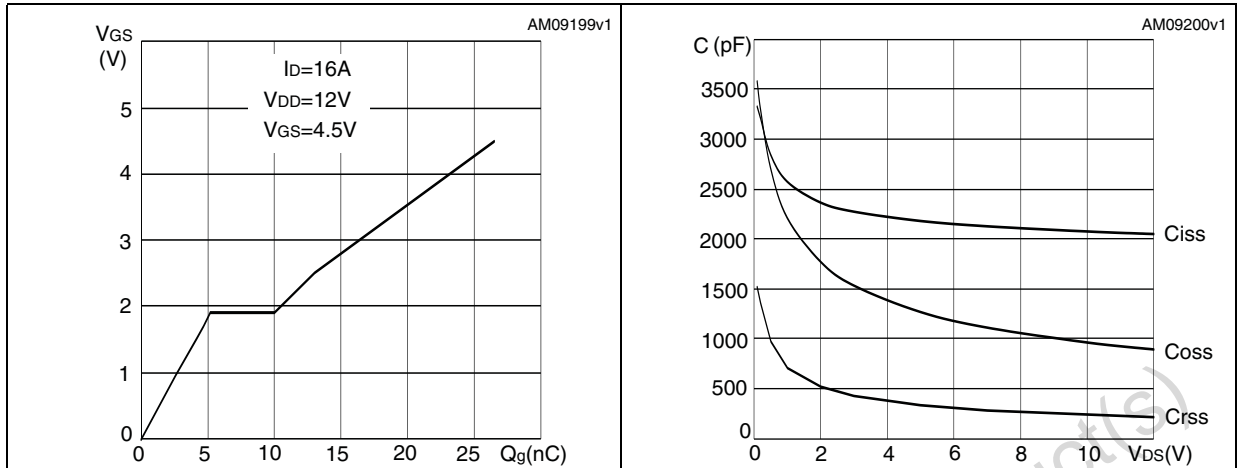


Figure 10. Normalized gate threshold voltage vs temperature Figure 11. Normalized on resistance vs temperature

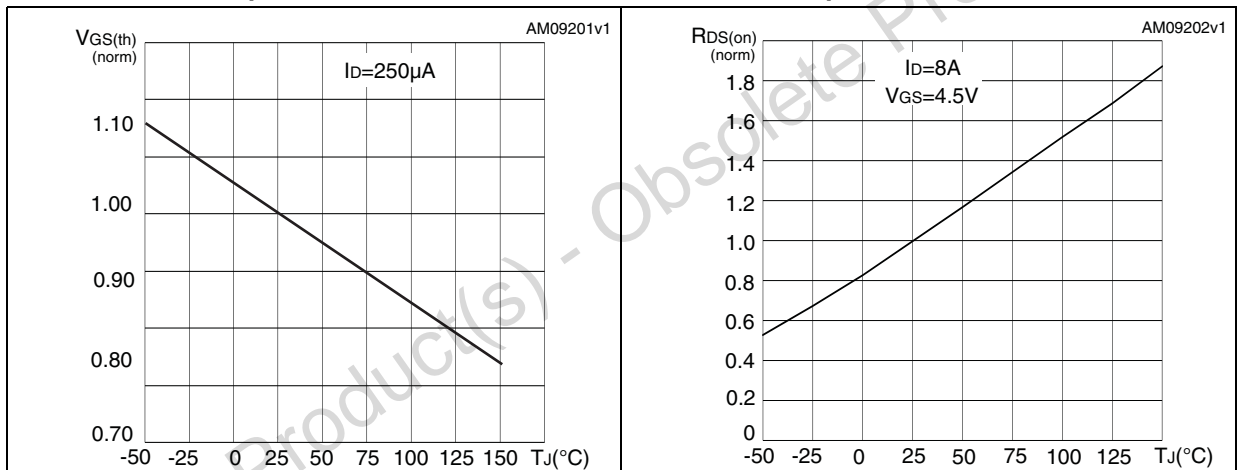
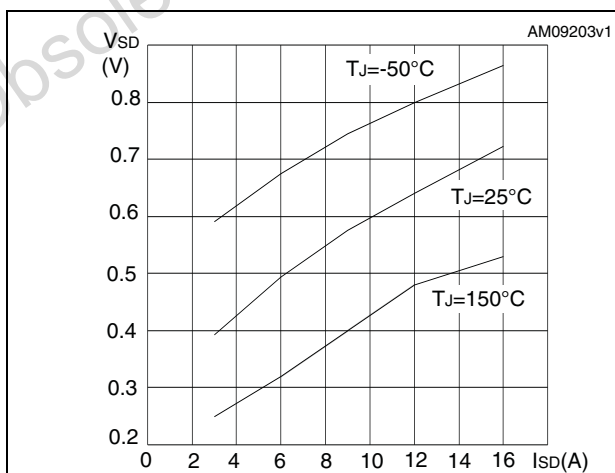


Figure 12. Source-drain diode forward characteristics



3 Test circuits

Figure 13. Switching times test circuit for resistive load

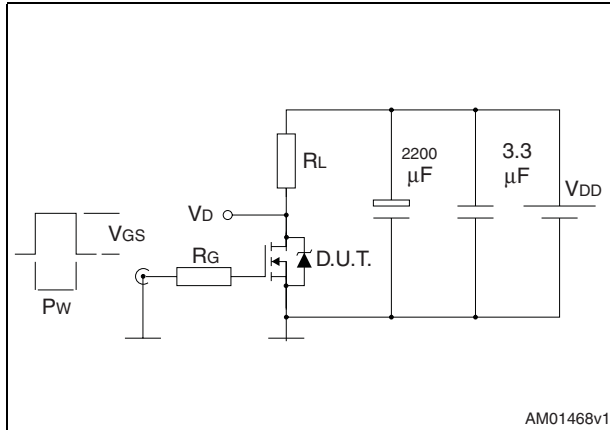


Figure 14. Gate charge test circuit

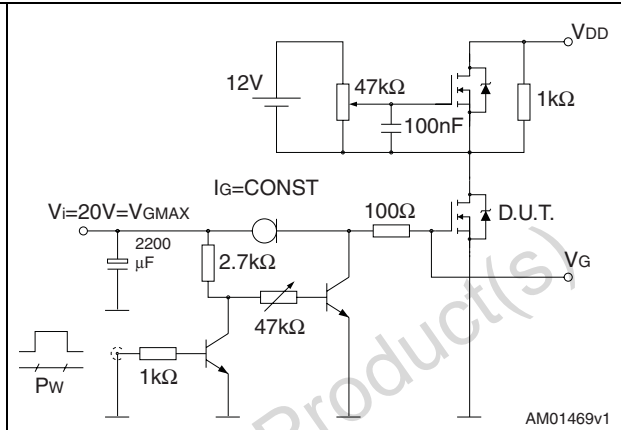


Figure 15. Test circuit for inductive load switching and diode recovery times

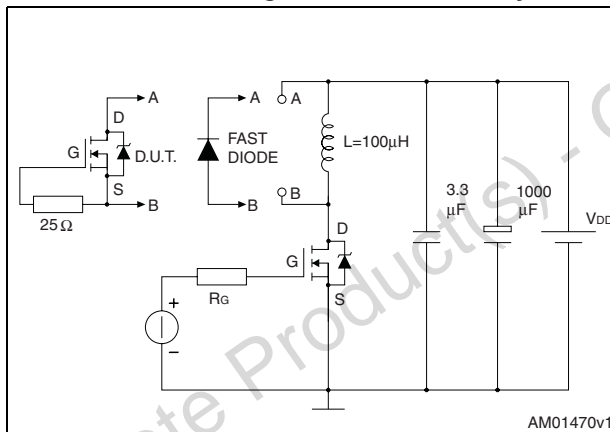


Figure 16. Unclamped inductive load test circuit

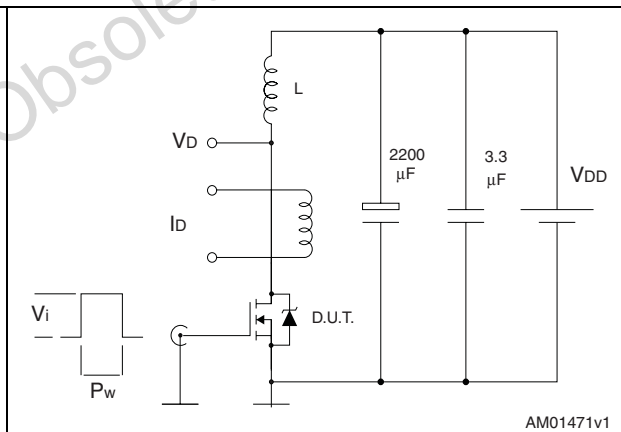


Figure 17. Unclamped inductive waveform

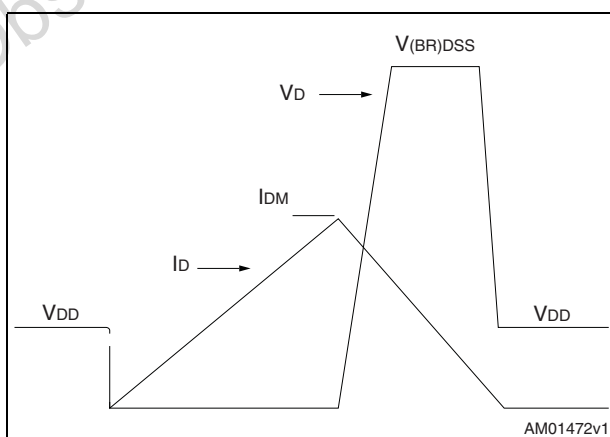
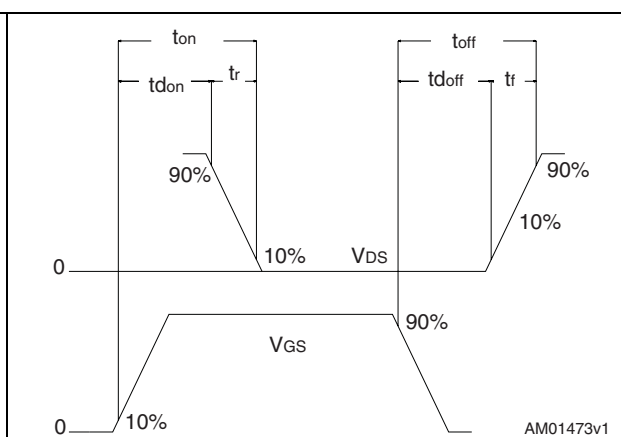


Figure 18. Switching time waveform



4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

Obsolete Product(s) - Obsolete Product(s)

Table 9. PowerFLAT™ (3.3 x 3.3) package dimensions

Dim.	mm.		
	Min.	Typ	Max.
A	0.80	0.90	1.00
A1	0.00	0.02	0.05
b	0.25	0.30	0.35
D		3.30	
D2	2.50	2.65	2.75
e		0.65	
E		3.30	
E2	1.76	1.91	2.01
L	0.30	0.40	0.50

Figure 19. PowerFLAT™ (3.3 x 3.3) package drawing

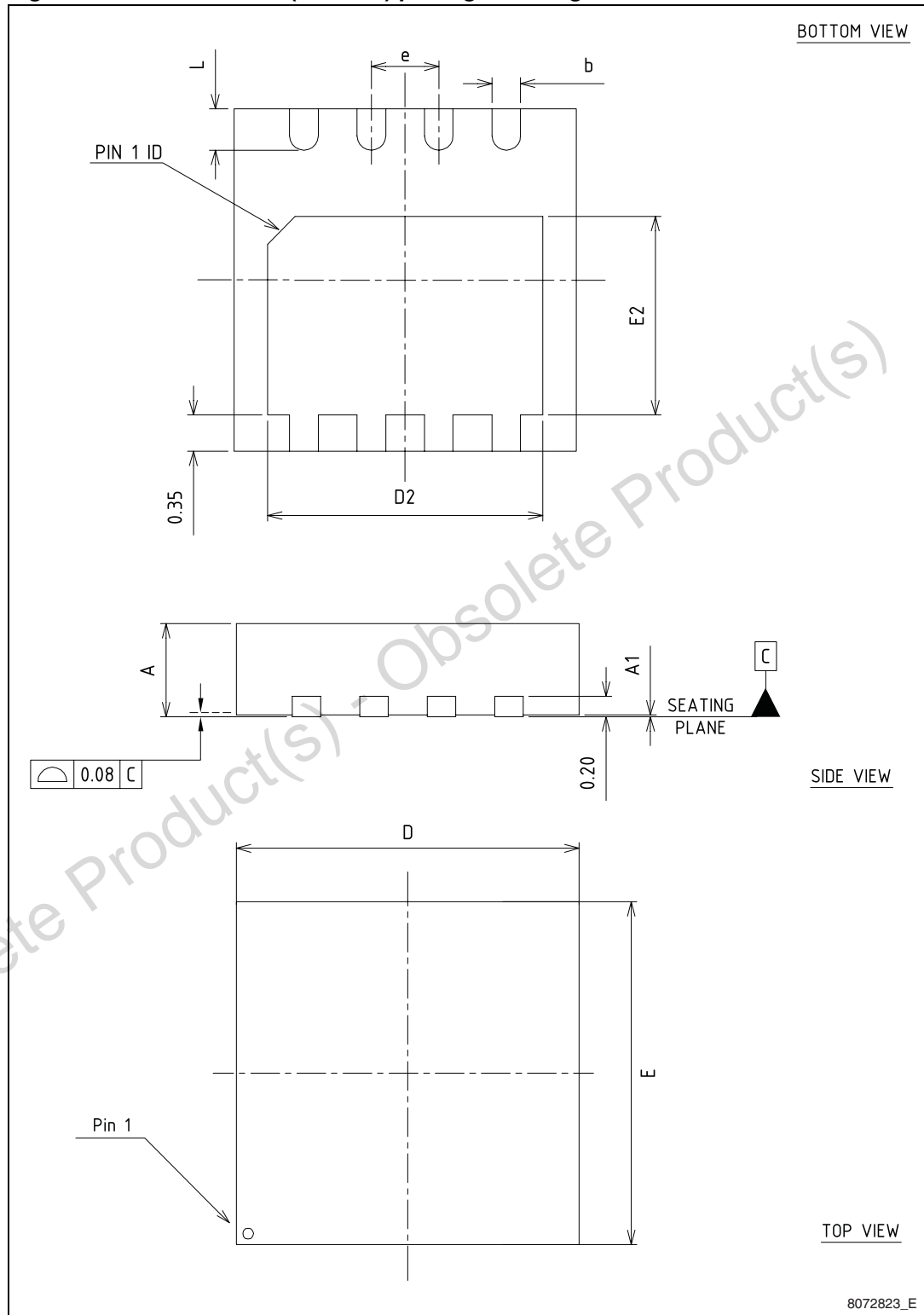
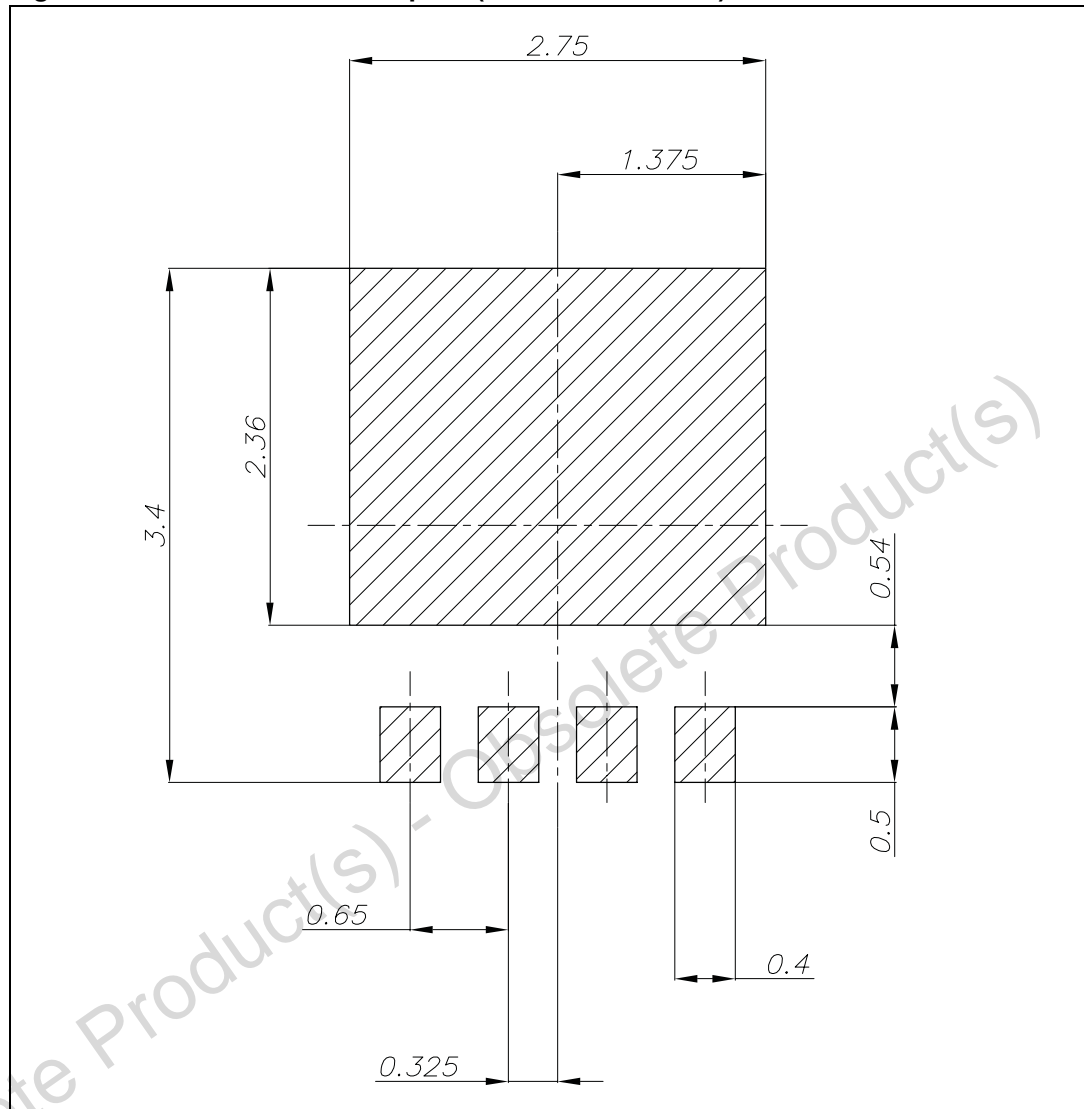


Figure 20. Recommended footprint (dimensions in mm)



5 Revision history

Table 10. Document revision history

Date	Revision	Changes
20-Nov-2009	1	First release.
21-Jun-2011	2	Document status promoted from preliminary data to datasheet.

Obsolete Product(s) - Obsolete Product(s)

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