

N-channel 600 V, 0.30 Ω typ., 8 A MDmesh™ M6 Power MOSFET in a PowerFLAT™ 5x6 HV package

Datasheet - production data

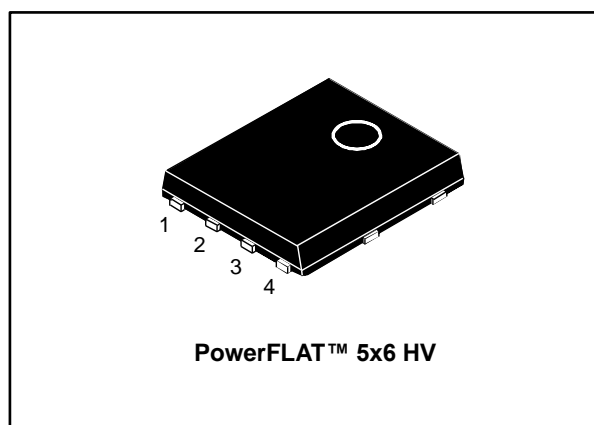
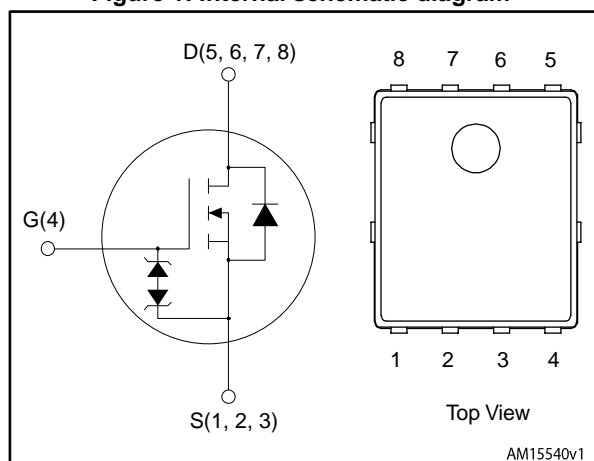


Figure 1: Internal schematic diagram



Features

Order code	V _{DS}	R _{DS(on)} max.	I _D
STL16N60M6	600 V	0.35 Ω	8 A

- Reduced switching losses
- Lower R_{DS(on)} x area vs previous generation
- Low gate input resistance
- 100% avalanche tested
- Zener-protected

Applications

- Switching applications

Description

The new MDmesh™ M6 technology incorporates the most recent advancements to the well-known and consolidated MDmesh family of SJ MOSFETs. STMicroelectronics builds on the previous generation of MDmesh devices through its new M6 technology, which combines excellent R_{DS(on)} * area improvement with one of the most effective switching behaviors available, as well as a user-friendly experience for maximum end-application efficiency.

Table 1: Device summary

Order code	Marking	Package	Packing
STL16N60M6	16N60M6	PowerFLAT™ 5x6 HV	Tape and reel

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1 Electrical ratings

Table 2: Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{GS}	Gate-source voltage	± 25	V
I_D	Drain current (continuous) at $T_C = 25\text{ °C}$	8 ⁽¹⁾	A
I_D	Drain current (continuous) at $T_C = 100\text{ °C}$	5 ⁽¹⁾	A
I_{DM} ⁽²⁾	Drain current (pulsed)	32	A
P_{TOT}	Total dissipation at $T_C = 25\text{ °C}$	52	W
dv/dt ⁽³⁾	Peak diode recovery voltage slope	15	V/ns
dv/dt ⁽⁴⁾	MOSFET dv/dt ruggedness	50	V/ns
T_{stg}	Storage temperature range	-55 to 150	°C
T_j	Operating junction temperature range		

Notes:

(1) This value is limited by package.

(2) Pulse width is limited by safe operating area.

(3) $I_{SD} \leq 8\text{ A}$, $di/dt \leq 400\text{ A}/\mu\text{s}$, $V_{DS\text{ peak}} < V_{(BR)DSS}$, $V_{DD} = 80\% V_{(BR)DSS}$

(4) $V_{DS} \leq 480\text{ V}$

Table 3: Thermal data

Symbol	Parameter	Value	Unit
$R_{thj-case}$	Thermal resistance junction-case	2.4	°C/W
$R_{thj-pcb}$ ⁽¹⁾	Thermal resistance junction-pcb	50	°C/W

Notes:

(1) When mounted on 1 inch² FR-4, 2 Oz copper board

Table 4: Avalanche characteristics

Symbol	Parameter	Value	Unit
I_{AR}	Avalanche current, repetitive or not repetitive (pulse width limited by T_{jmax})	2.5	A
E_{AS}	Single pulse avalanche energy (starting $T_j = 25\text{ °C}$, $I_D = I_{AR}$, $V_{DD} = 50\text{ V}$)	110	mJ

2 Electrical characteristics

($T_C = 25\text{ °C}$ unless otherwise specified)

Table 5: On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$V_{GS} = 0\text{ V}$, $I_D = 1\text{ mA}$	600			V
I_{DSS}	Zero gate voltage drain current	$V_{GS} = 0\text{ V}$, $V_{DS} = 600\text{ V}$			1	μA
		$V_{GS} = 0\text{ V}$, $V_{DS} = 600\text{ V}$, $T_C = 125\text{ °C}^{(1)}$			100	μA
I_{GSS}	Gate-body leakage current	$V_{DS} = 0\text{ V}$, $V_{GS} = \pm 25\text{ V}$			± 5	μA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}$, $I_D = 250\text{ }\mu\text{A}$	3.25	4	4.75	V
$R_{DS(on)}$	Static drain-source on-resistance	$V_{GS} = 10\text{ V}$, $I_D = 6\text{ A}$		0.30	0.35	Ω

Notes:

⁽¹⁾Defined by design, not subject to production test.

Table 6: Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	$V_{DS} = 100\text{ V}$, $f = 1\text{ MHz}$, $V_{GS} = 0\text{ V}$	-	575	-	pF
C_{oss}	Output capacitance		-	33	-	pF
C_{rss}	Reverse transfer capacitance		-	3	-	pF
$C_{oss\text{ eq.}}^{(1)}$	Equivalent output capacitance	$V_{DS} = 0\text{ to }480\text{ V}$, $V_{GS} = 0\text{ V}$	-	104	-	pF
R_G	Intrinsic gate resistance	$f = 1\text{ MHz}$ open drain	-	5.2	-	Ω
Q_g	Total gate charge	$V_{DD} = 480\text{ V}$, $I_D = 12\text{ A}$, $V_{GS} = 0\text{ to }10\text{ V}$ (see Figure 15: "Test circuit for gate charge behavior")	-	16.7	-	nC
Q_{gs}	Gate-source charge		-	3.5	-	nC
Q_{gd}	Gate-drain charge		-	9.4	-	nC

Notes:

⁽¹⁾ $C_{oss\text{ eq.}}$ is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS} .

Table 7: Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 300\text{ V}$, $I_D = 6\text{ A}$, $R_G = 4.7\text{ }\Omega$, $V_{GS} = 10\text{ V}$ (see Figure 14: "Test circuit for resistive load switching times" and Figure 19: "Switching time waveform")	-	13	-	ns
t_r	Rise time		-	7.6	-	ns
$t_{d(off)}$	Turn-off-delay time		-	19.8	-	ns
t_f	Fall time		-	6.8	-	ns

Table 8: Source drain diode

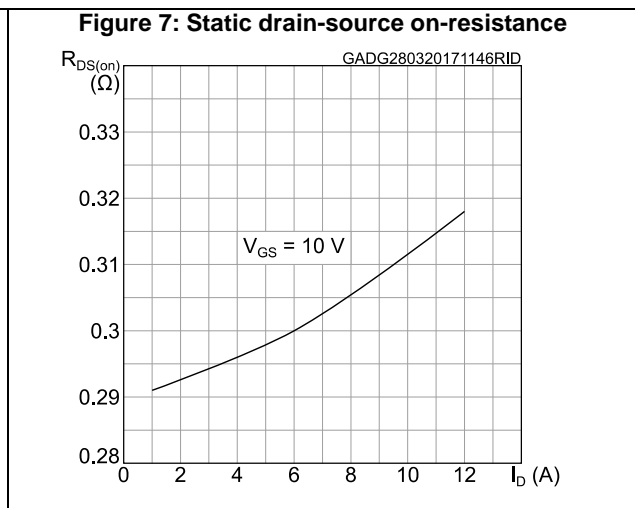
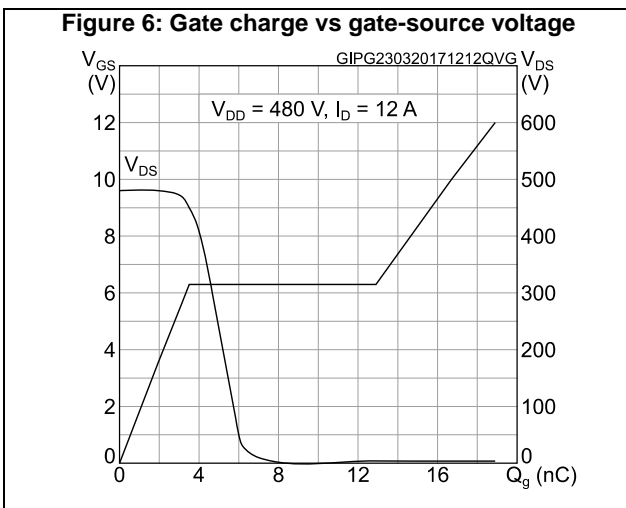
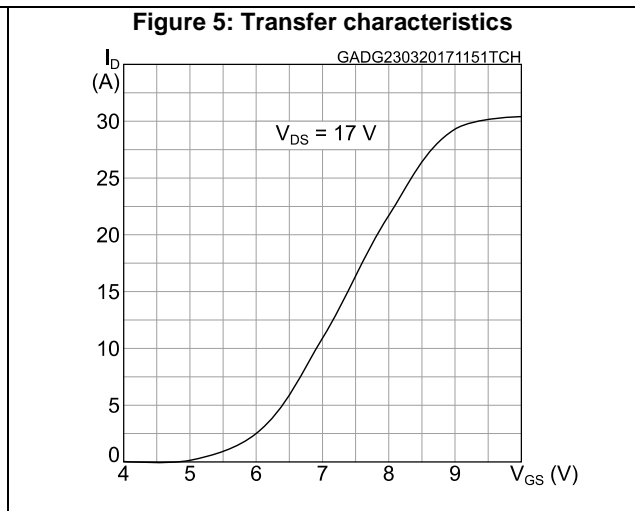
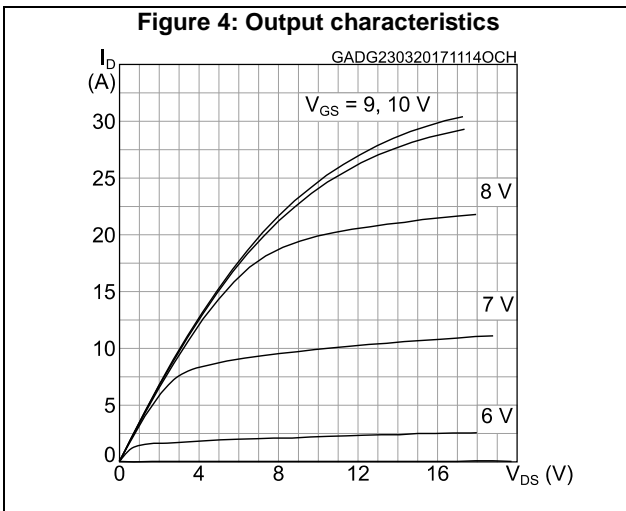
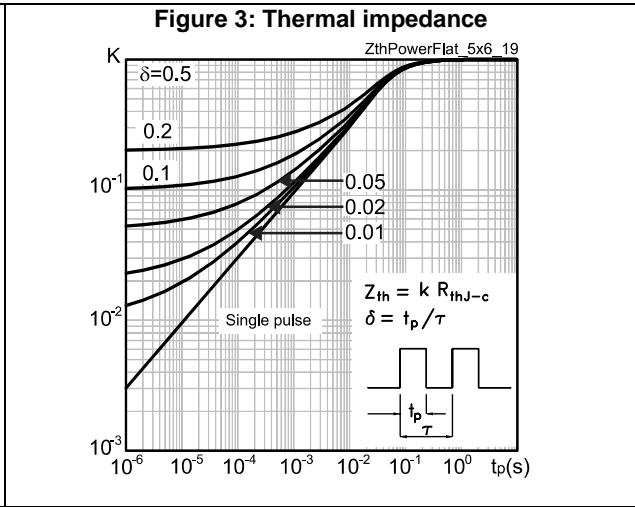
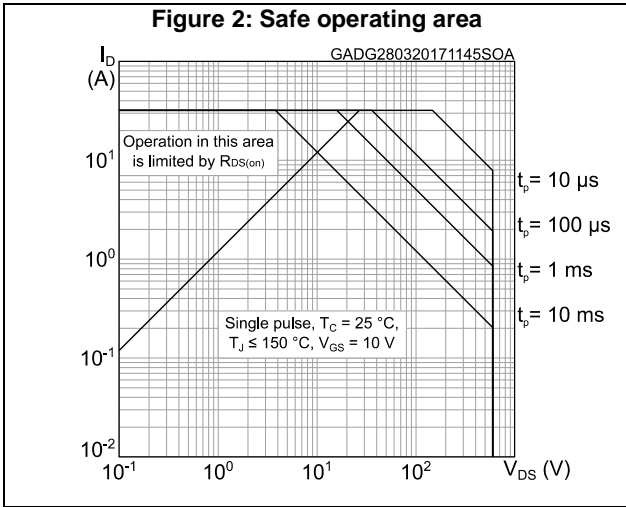
Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		8	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)		-		32	A
$V_{SD}^{(2)}$	Forward on voltage	$V_{GS} = 0\text{ V}$, $I_{SD} = 8\text{ A}$	-		1.6	V
t_{rr}	Reverse recovery time	$I_{SD} = 12\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$, $V_{DD} = 60\text{ V}$ (see Figure 16 : "Test circuit for inductive load switching and diode recovery times")	-	210		ns
Q_{rr}	Reverse recovery charge		-	1.7		μC
I_{RRM}	Reverse recovery current		-	13.8		A
t_{rr}	Reverse recovery time	$I_{SD} = 12\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$, $V_{DD} = 60\text{ V}$, $T_j = 150\text{ }^\circ\text{C}$ (see Figure 16 : "Test circuit for inductive load switching and diode recovery times")	-	310		ns
Q_{rr}	Reverse recovery charge		-	3.2		μC
I_{RRM}	Reverse recovery current		-	15.4		A

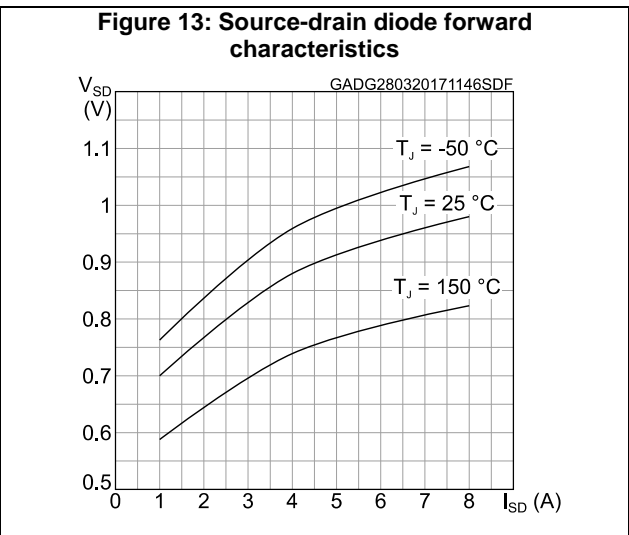
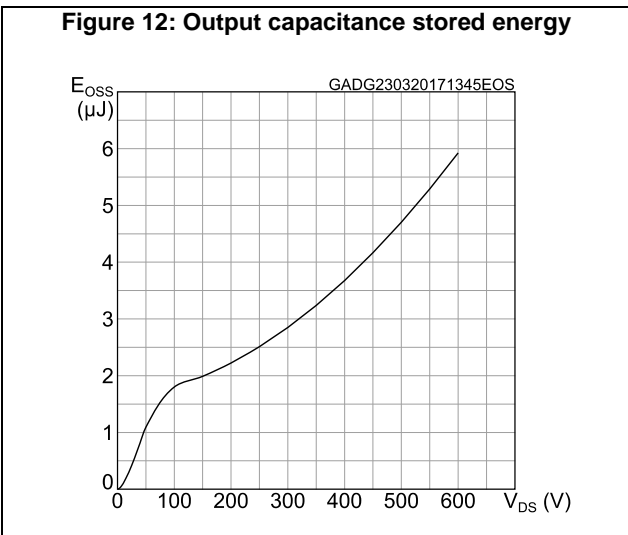
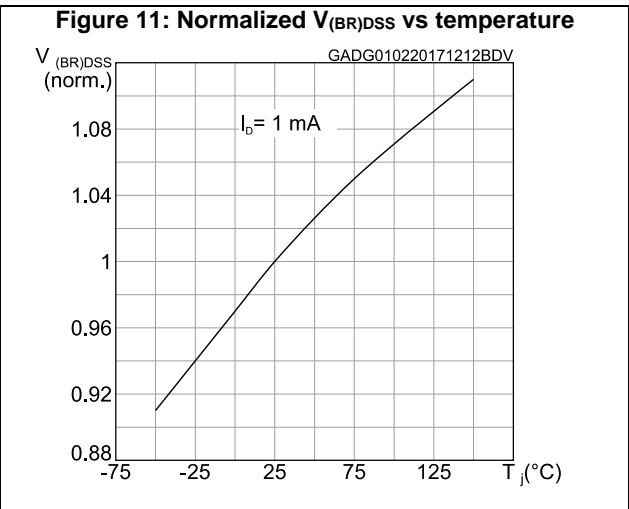
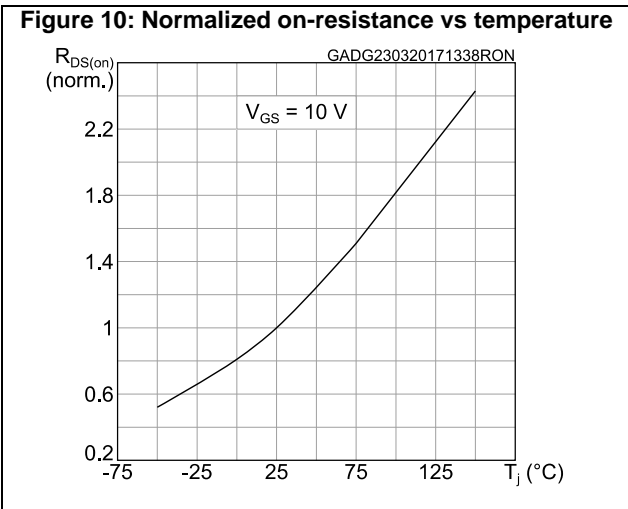
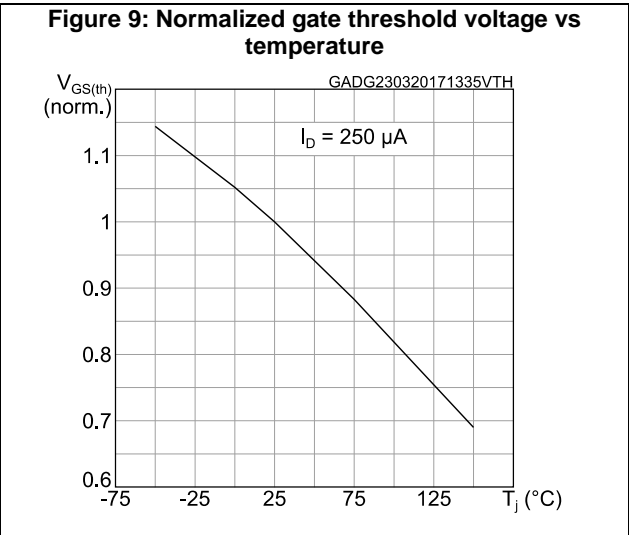
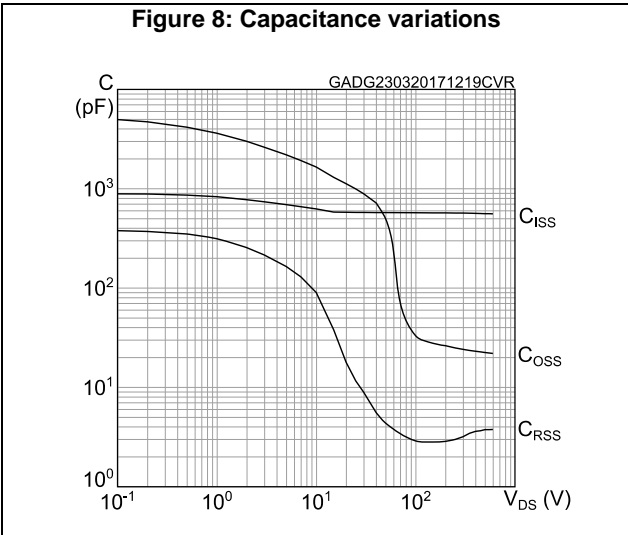
Notes:

(1)Pulse width is limited by safe operating area.

(2)Pulse test: pulse duration = 300 μs , duty cycle 1.5%

2.1 Electrical characteristics (curves)





3 Test circuits

Figure 14: Test circuit for resistive load switching times



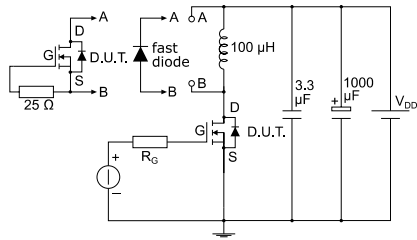
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Figure 15: Test circuit for gate charge behavior



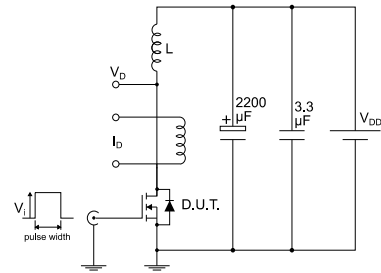
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Figure 16: Test circuit for inductive load switching and diode recovery times



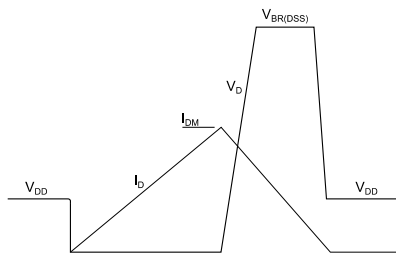
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Figure 17: Unclamped inductive load test circuit



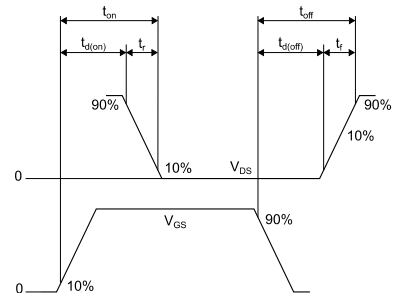
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Figure 18: Unclamped inductive waveform



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Figure 19: Switching time waveform



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4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

4.1 PowerFLAT™ 5x6 HV package information

Figure 20: PowerFLAT™ 5x6 HV package outline

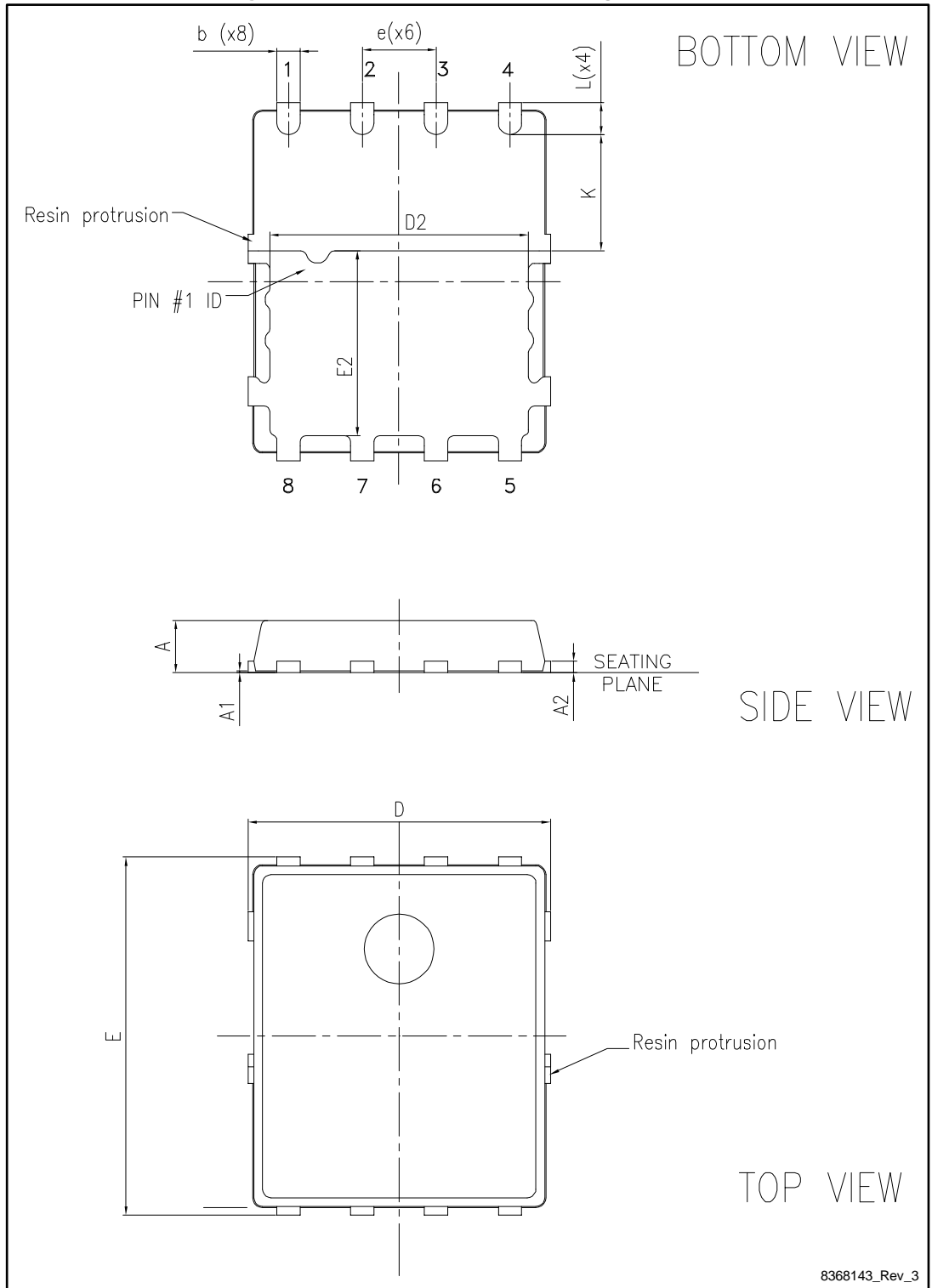
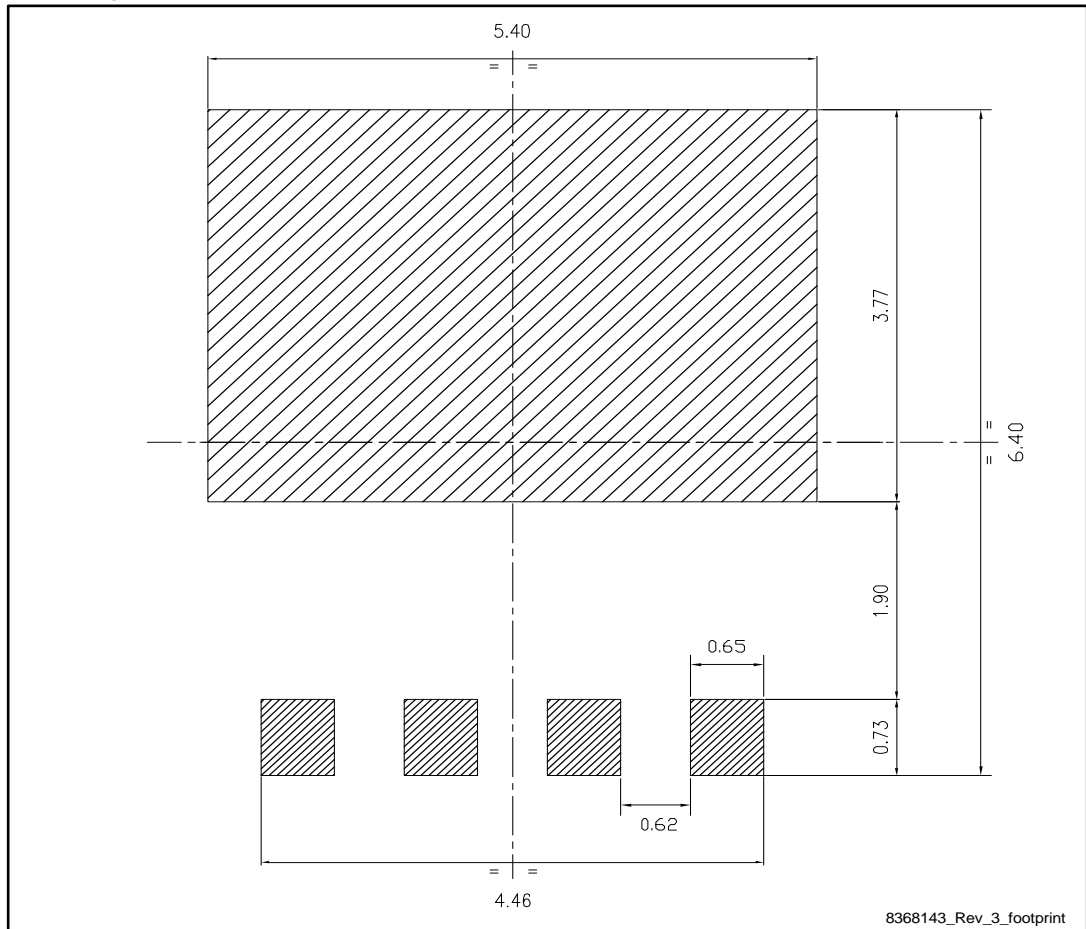


Table 9: PowerFLAT™ 5x6 HV mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	0.80		1.00
A1	0.02		0.05
A2		0.25	
b	0.30		0.50
D	5.10	5.20	5.30
E	6.05	6.15	6.25
E2	3.10	3.20	3.30
D2	4.30	4.40	4.50
e		1.27	
L	0.50	0.55	0.60
K	1.90	2.00	2.10

Figure 21: PowerFLAT™ 5x6 HV recommended footprint (dimensions are in mm)



4.2 PowerFLAT™ 5x6 packing information

Figure 22: PowerFLAT™ 5x6 tape (dimensions are in mm)

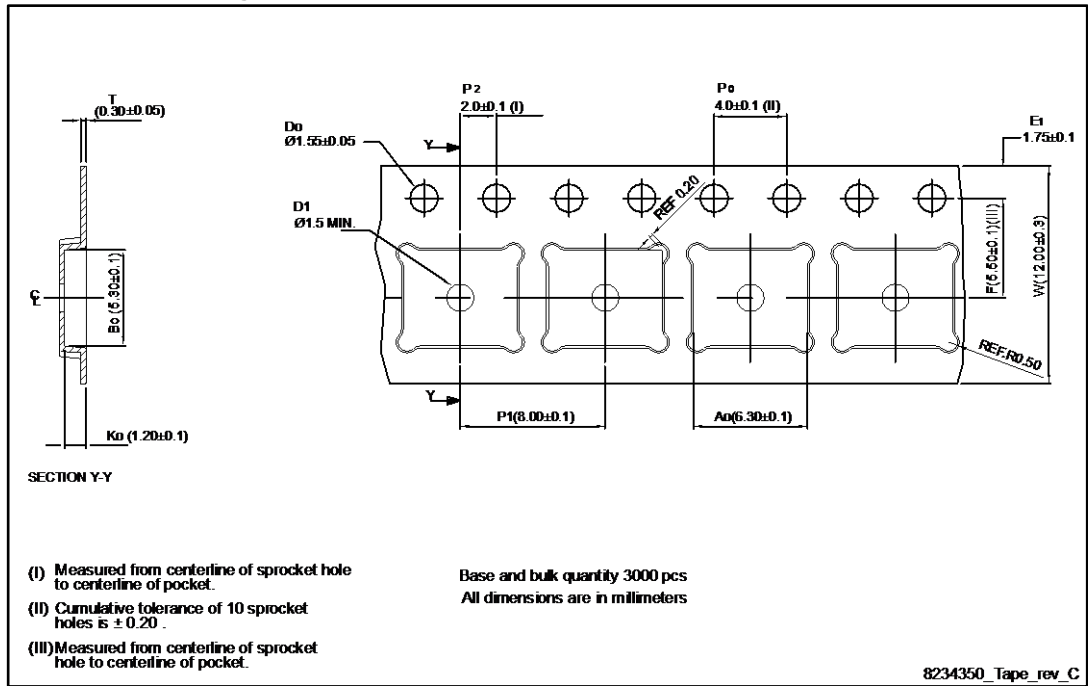


Figure 23: PowerFLAT™ 5x6 package orientation in carrier tape

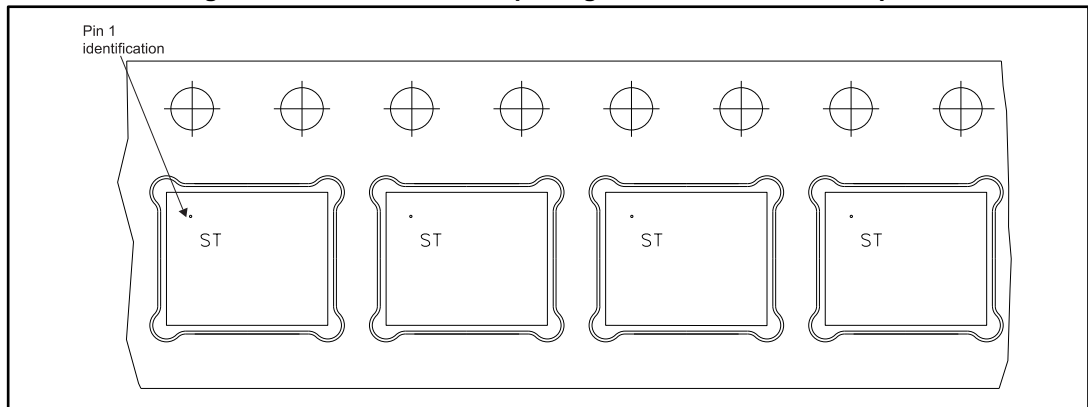
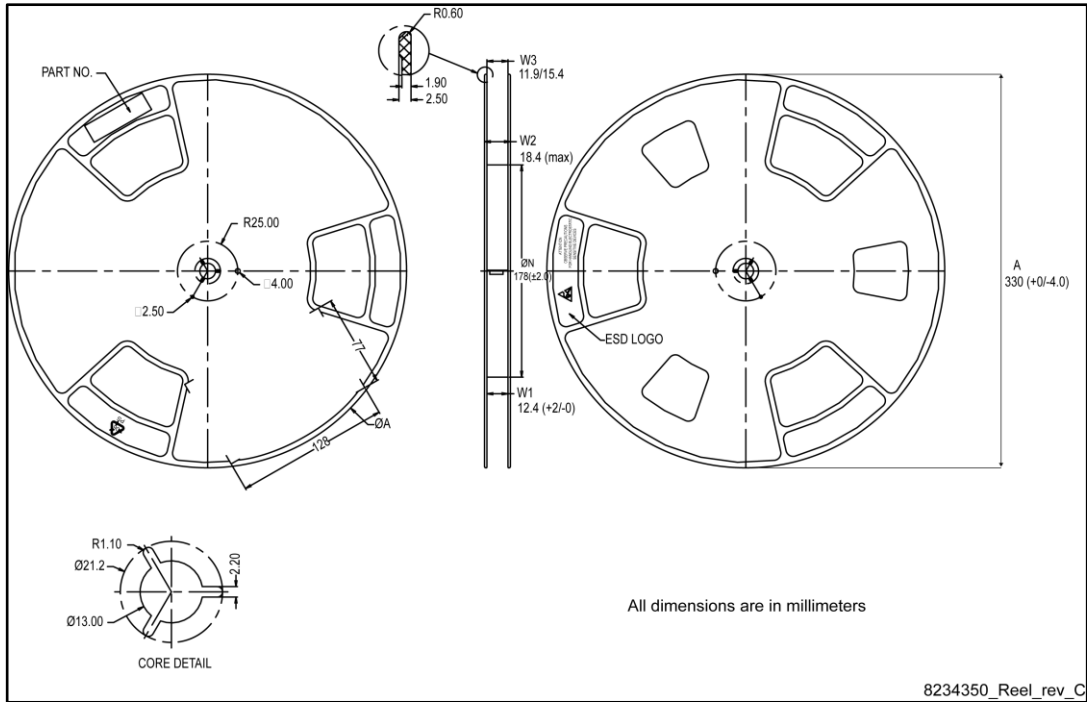


Figure 24: PowerFLAT™ 5x6 reel



5 Revision history

Table 10: Document revision history

Date	Revision	Changes
03-Apr-2017	1	First release

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