



STL18N55M5

N-channel 550 V, 0.180 Ω , 13 A PowerFLAT™ (8x8) HV
ultra low gate charge MDmesh™ V Power MOSFET

Preliminary data

Features

Type	V _{DSS} @ T _{Jmax}	R _{DS(on)} max	I _D
STL18N55M5	600 V	< 0.240 Ω	13 A ⁽¹⁾

1. The value is rated according to R_{thj-case}

- 100% avalanche tested
- Low input capacitance and gate charge
- Low gate input resistance

Application

- Switching applications

Description

MDmesh™ V is a revolutionary Power MOSFET technology based on an innovative proprietary vertical process, which is combined with STMicroelectronics' well-known PowerMESH™ horizontal layout structure. The resulting product has extremely low on-resistance, which is unmatched among silicon-based Power MOSFETs, making it especially suitable for applications which require superior power density and outstanding efficiencies.

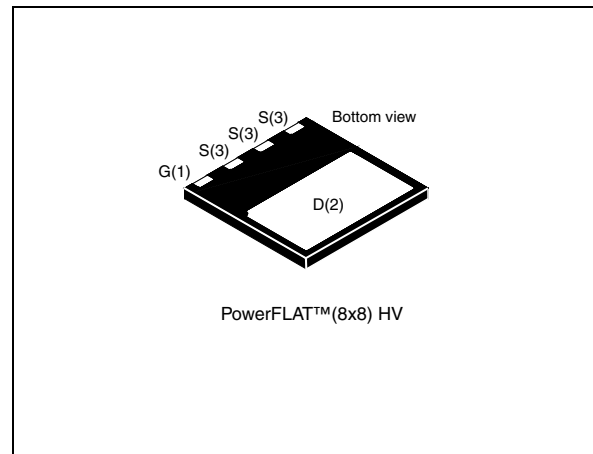


Figure 1. Internal schematic diagram

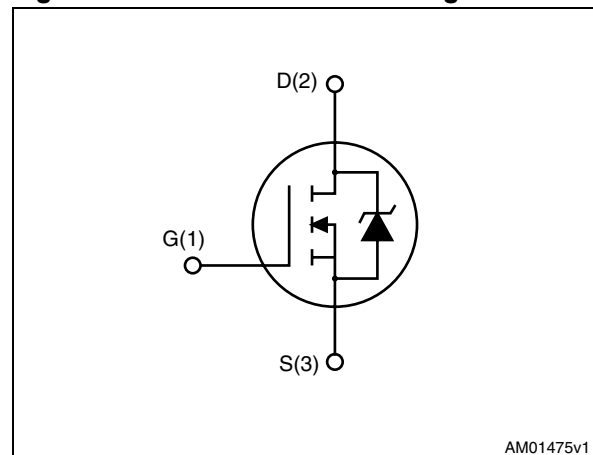


Table 1. Device summary

Order code	Marking	Package	Packaging
STL18N55M5	18N55M5	PowerFLAT™ (8x8) HV	Tape and reel

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1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage ($V_{GS} = 0$)	550	V
V_{GS}	Gate-source voltage	± 25	V
$I_D^{(1)}$	Drain current (continuous) at $T_C = 25\text{ }^\circ\text{C}$	13	A
$I_D^{(1)}$	Drain current (continuous) at $T_C = 100\text{ }^\circ\text{C}$	8	A
$I_{DM}^{(1),(2)}$	Drain current (pulsed)	52	A
$I_D^{(3)}$	Drain current (continuous) at $T_C = 25\text{ }^\circ\text{C}$	2.4	A
$I_D^{(3)}$	Drain current (continuous) at $T_C = 100\text{ }^\circ\text{C}$	1.5	A
$I_{DM}^{(2),(3)}$	Drain current (pulsed)	9.6	A
$P_{TOT}^{(3)}$	Total dissipation at $T_C = 25\text{ }^\circ\text{C}$ (steady state)	3	W
$P_{TOT}^{(1)}$	Total dissipation at $T_C = 25\text{ }^\circ\text{C}$ (steady state)	90	W
I_{AR}	Avalanche current, repetitive or not-repetitive (pulse width limited by T_j max)	4	A
E_{AS}	Single pulse avalanche energy (starting $T_j = 25\text{ }^\circ\text{C}$, $I_D = I_{AR}$, $V_{DD} = 50\text{ V}$)	200	mJ
$dv/dt^{(4)}$	Peak diode recovery voltage slope	15	V/ns
T_{stg}	Storage temperature	- 55 to 150	$^\circ\text{C}$
T_j	Max. operating junction temperature	150	$^\circ\text{C}$

1. The value is rated according to $R_{thj-case}$
2. Pulse width limited by safe operating area
3. When mounted on FR-4 board of 1 inch^2 , 2oz Cu
4. $I_{SD} \leq 13\text{ A}$, $di/dt \leq 400\text{ A}/\mu\text{s}$, $V_{Peak} < V_{(BR)DSS}$

Table 3. Thermal data

Symbol	Parameter	Value	Unit
$R_{thj-case}$	Thermal resistance junction-case max	1.38	$^\circ\text{C}/\text{W}$
$R_{thj-amb}^{(1)}$	Thermal resistance junction-amb max	45	$^\circ\text{C}/\text{W}$

1. When mounted on 1 inch^2 FR-4 board, 2 oz Cu

2 Electrical characteristics

($T_C = 25\text{ }^\circ\text{C}$ unless otherwise specified)

Table 4. On /off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$I_D = 1\text{ mA}$, $V_{GS} = 0$	550			V
I_{DSS}	Zero gate voltage drain current ($V_{GS} = 0$)	$V_{DS} = \text{Max rating}$ $V_{DS} = \text{Max rating}$, $T_C = 125\text{ }^\circ\text{C}$			1 100	μA μA
I_{GSS}	Gate-body leakage current ($V_{DS} = 0$)	$V_{GS} = \pm 25\text{ V}$			100	nA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}$, $I_D = 250\text{ }\mu\text{A}$	3	4	5	V
$R_{DS(on)}$	Static drain-source on resistance	$V_{GS} = 10\text{ V}$, $I_D = 7\text{ A}$		0.180	0.240	Ω

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	$V_{DS} = 100\text{ V}$, $f = 1\text{ MHz}$, $V_{GS} = 0$	-	1340	-	pF
C_{oss}	Output capacitance			38		pF
C_{rss}	Reverse transfer capacitance			3.4		pF
$C_{o(tr)}^{(1)}$	Equivalent capacitance time related	$V_{DS} = 0\text{ to }440\text{ V}$, $V_{GS} = 0$	-	98	-	pF
$C_{o(er)}^{(2)}$	Equivalent capacitance energy related			35		pF
R_G	Intrinsic gate resistance	$f = 1\text{ MHz}$ open drain	-	1.7	-	Ω
Q_g	Total gate charge	$V_{DD} = 440\text{ V}$, $I_D = 13\text{ A}$, $V_{GS} = 10\text{ V}$ (see Figure 3)	-	31	-	nC
Q_{gs}	Gate-source charge			6		nC
Q_{gd}	Gate-drain charge			14		nC

- $C_{oss\text{ eq}}$, time related is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}
- $C_{oss\text{ eq}}$, energy related is defined as a constant equivalent capacitance giving the same stored energy as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}

Table 6. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max	Unit
$t_{d(off)}$	Turn-off delay time	$V_{DD} = 400\text{ V}$, $I_D = 9\text{ A}$,		29		ns
t_r	Rise time	$R_G = 4.7\ \Omega$, $V_{GS} = 10\text{ V}$	-	9.5	-	ns
t_c	Cross time	(see Figure 4),		23		ns
t_f	Fall time	(see Figure 7)		13		ns

Table 7. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		13	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)		-		52	A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD} = 13\text{ A}$, $V_{GS} = 0$	-		1.5	V
t_{rr}	Reverse recovery time	$I_{SD} = 13\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$	-	238		ns
Q_{rr}	Reverse recovery charge	$V_{DD} = 60\text{ V}$ (see Figure 4)		2.8		μC
I_{RRM}	Reverse recovery current			23.5		A
t_{rr}	Reverse recovery time	$I_{SD} = 13\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$	-	278		ns
Q_{rr}	Reverse recovery charge	$V_{DD} = 60\text{ V}$, $T_J = 150\text{ }^\circ\text{C}$		3.3		μC
I_{RRM}	Reverse recovery current	(see Figure 4)		24		A

1. Pulse width limited by safe operating area
2. Pulsed: pulse duration = 300 μs , duty cycle 1.5%

3 Test circuits

Figure 2. Switching times test circuit for resistive load

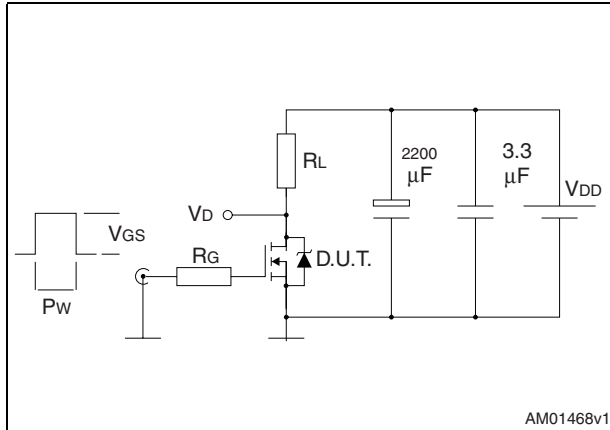


Figure 3. Gate charge test circuit

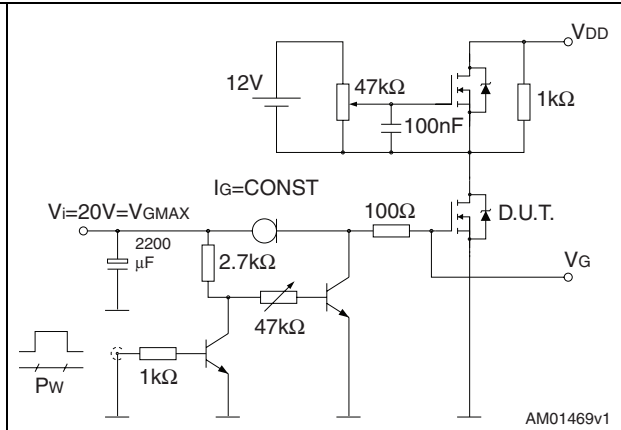


Figure 4. Test circuit for inductive load switching and diode recovery times

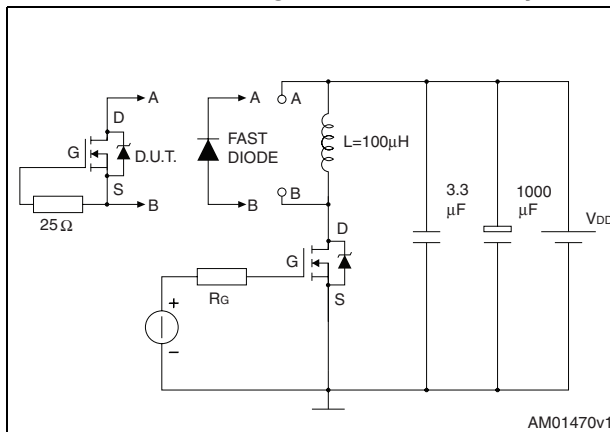


Figure 5. Unclamped inductive load test circuit

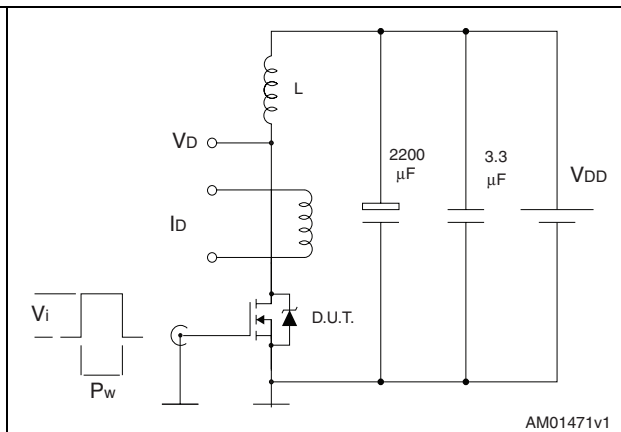


Figure 6. Unclamped inductive waveform

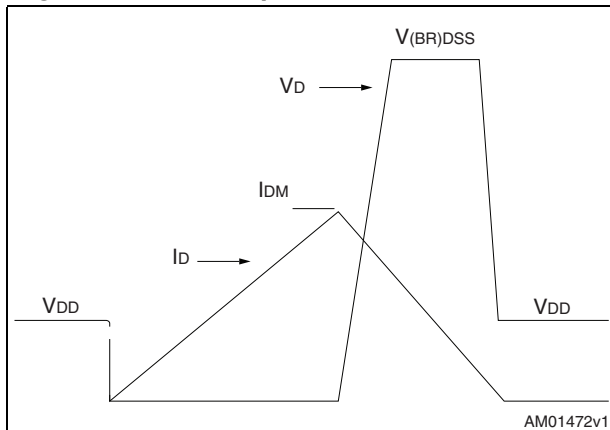
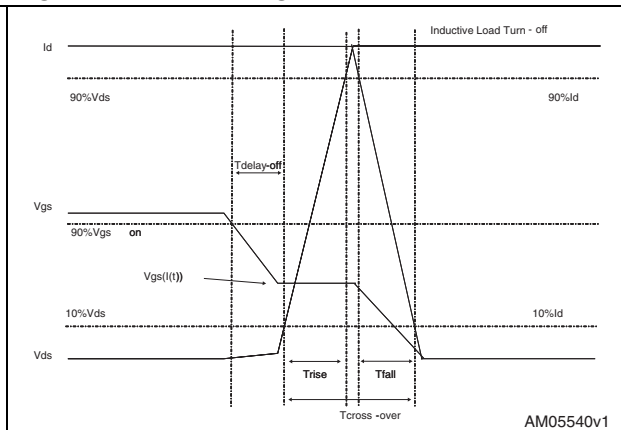


Figure 7. Switching time waveform



4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

Table 8. PowerFLAT™ 8x8 HV mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	0.80	0.90	1.00
A1		0.02	0.05
b	0.95	1.00	1.05
c		0.10	
D		8.00	
E		8.00	
D2	7.05	7.20	7.30
E2	4.15	4.30	4.40
e		2.00	
L	0.40	0.50	0.60

Figure 8. PowerFLAT™ 8x8 HV drawing mechanical data

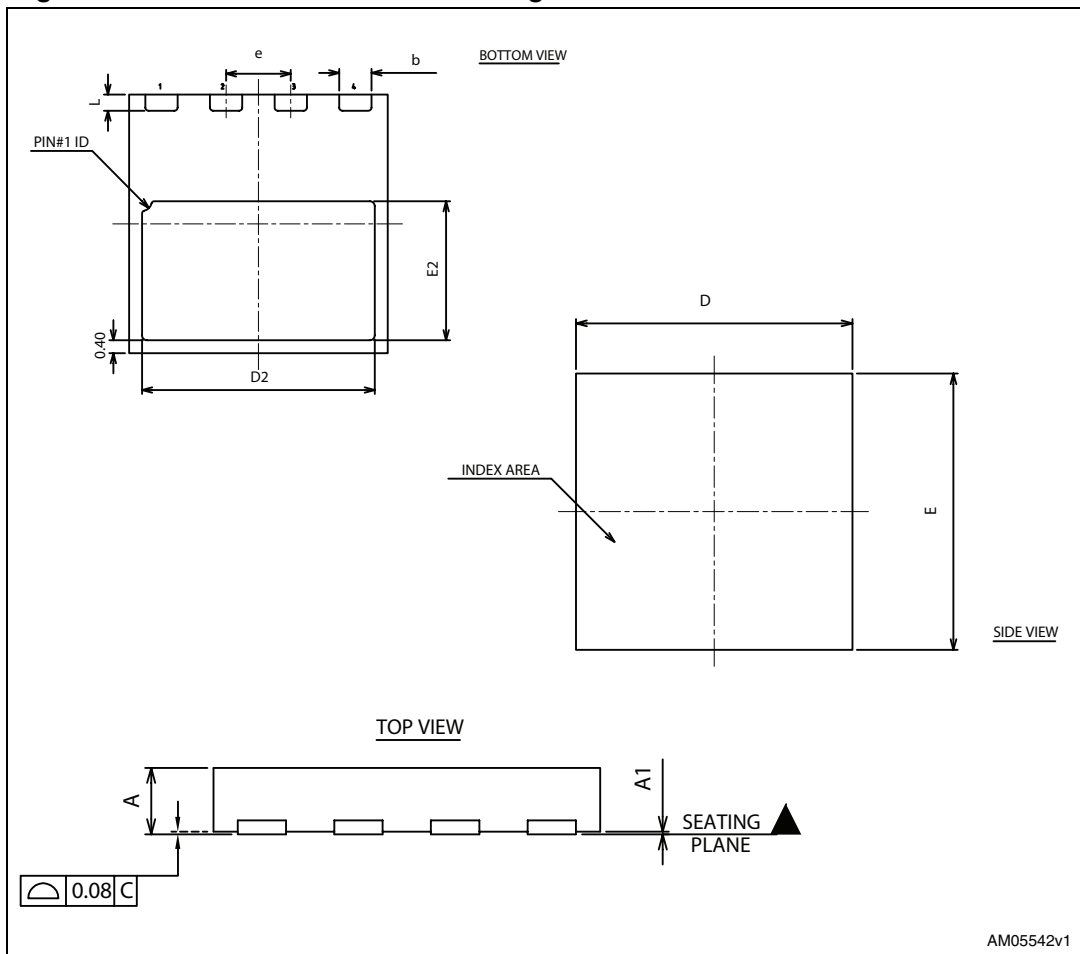
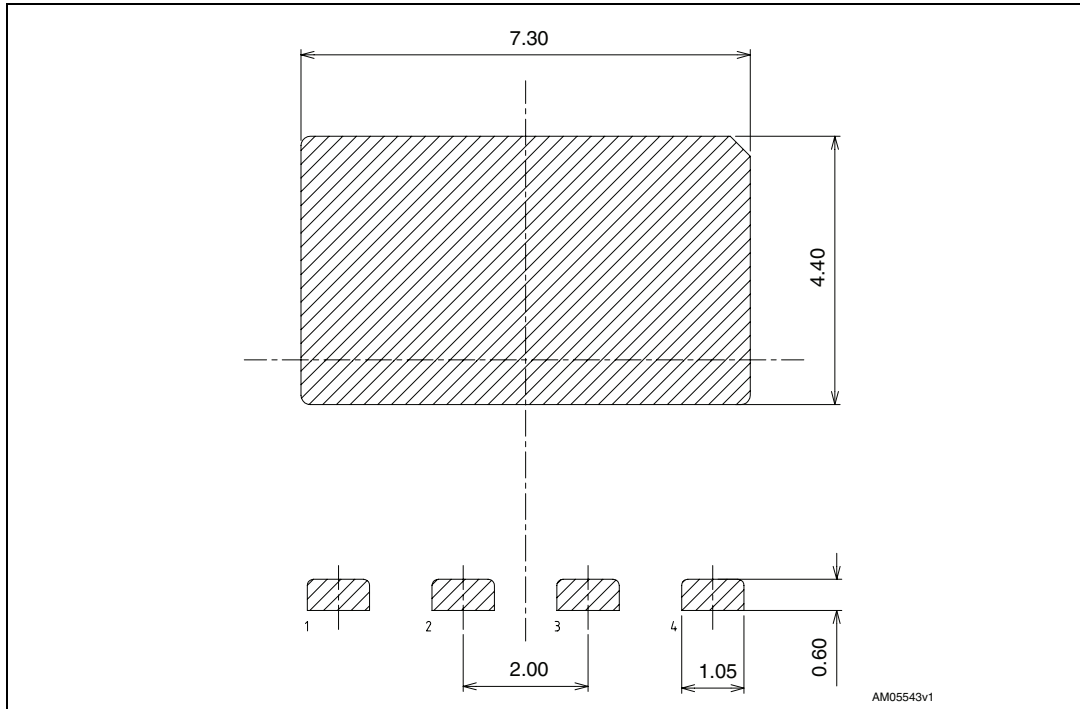


Figure 9. PowerFLAT™ 8x8 HV recommended footprint



5 Revision history

Table 9. Document revision history

Date	Revision	Changes
03-May-2010	1	First release

STL18N55M5

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