STL18N60M2

N-channel 600 V, 0.278 Ω typ., 9 A MDmesh™ M2 Power MOSFET in a PowerFLAT™ 5x6 HV package

Datasheet - production data

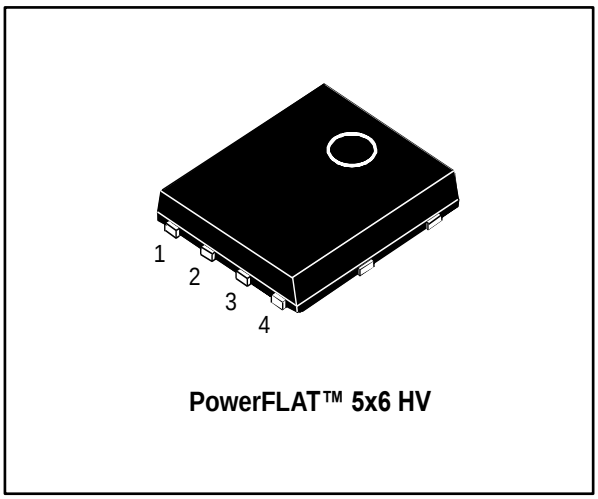
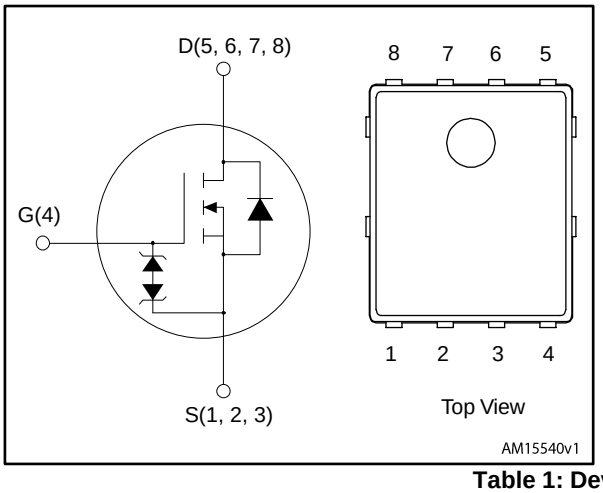


Figure 1: Internal schematic diagram



Features

Order code	V_{DS} @ T_{Jmax}	$R_{DS(on)}$ max.	I_D
STL18N60M2	650 V	0.308 Ω	9 A

- Extremely low gate charge
- Excellent output capacitance (C_{OSS}) profile
- 100% avalanche tested
- Zener-protected

Applications

- Switching applications

Description

This device is an N-channel Power MOSFET developed using MDmesh™ M2 technology. Thanks to its strip layout and an improved vertical structure, the device exhibits low on-resistance and optimized switching characteristics, rendering it suitable for the most demanding high efficiency converters.

Table 1: Device summary

Order code	Marking	Package	Packing
STL18N60M2	18N60M2	PowerFLAT™ 5x6 HV	Tape and reel

Contents

1 Electrical ratings

Table 2: Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{GS}	Gate-source voltage	± 25	V
I_D(1)	Drain current (continuous) at T_C = 25 °C	9	A
I_D(1)	Drain current (continuous) at T_C= 100 °C	5.5	A
I_{DM}(2)	Drain current (pulsed)	36	A
P_{TOT}(2)	Total dissipation at T_C = 25 °C	57	W
I_{AR}	Avalanche current, repetitive or notrepetitive (pulse width limited by T_j max)	2	A
E_{AS}	Single pulse avalanche energy (starting T_j = 25 °C, I_D = I_{AR}, V_{DD} = 50 V)	135	mJ
dv/dt(3)	Peak diode recovery voltage slope	15	V/ns
dv/dt(4)	MOSFET dv/dt ruggedness	50	V/ns
T_{stg}	Storage temperature range	- 55 to 150	°C
T_j	Operating junction temperature range		

Notes:

(1)The value is limited by package.

(2)Pulse width limited by safe operating area.

(3)I_{SD} ≤ 9 A, di/dt ≤ 400 A/µs; $V_{DS(peak)}$ ≤ $V_{(BR)DSS}$, V_{DD} = 400 V.

(4)V_{DS} ≤ 480 V.

Table 3: Thermal data

Symbol	Parameter	Value	Unit
$R_{thj\text{-}case}$	Thermal resistance junction-case	2.2	°C/W
$R_{thj\text{-}pcb}$(1)	Thermal resistance junction-pcb	59	°C/W

Notes:

(1)When mounted on 1inch^2 FR-4 board, 2 oz Cu.

2 Electrical characteristics

(T_C = 25 °C unless otherwise specified)

Table 4: On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V, I_D = 1 mA	600			V
I_{DSS}	Zero gate voltage drain current	V_{GS} = 0 V, V_{DS} = 600 V			1	µA
		V_{GS} = 0 V, V_{DS} = 600 V, T_C = 125 °C (1)			100	µA
I_{GSS}	Gate-body leakage current	V_{DS} = 0 V, V_{GS} = ±25 V			10	µA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 250 µA	2	3	4	V
$R_{DS(on)}$	Static drain-source on-resistance	V_{GS} = 10 V, I_D = 4.5 A		0.278	0.308	Ω

Notes:

(1) Defined by design, not subject to production test.

Table 5: Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	V_{DS} = 100 V, f = 1 MHz, V_{GS} = 0 V	-	791	-	pF
C_{oss}	Output capacitance		-	40	-	pF
C_{rss}	Reverse transfer capacitance			1.3	-	pF
$C_{oss\ eq.}$ (1)	Output equivalent capacitance	V_{DS} = 0 V to 480 V, V_{GS} = 0 V	-	164.5	-	pF
R_G	Intrinsic gate resistance	f = 1 MHz, I_D = 0 A	-	5.6	-	Ω
Q_g	Total gate charge	V_{DD} = 480 V, I_D = 13 A, V_{GS} = 0 to 10 V (see *Figure 15: "Test circuit for gate charge behavior"*)	-	21.5	-	nC
Q_{gs}	Gate-source charge		-	3.2	-	nC
Q_{gd}	Gate-drain charge		-	11.3	-	nC

Notes:

(1)$C_{oss\ eq.}$ is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80 % V_{DS}.

Table 6: Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	V_{DD} = 300 V, I_D = 6.5 A, R_G = 4.7 Ω, V_{GS} = 10 V (see *Figure 14: "Test circuit for resistive load switching times"* and *Figure 19: "Switching time waveform"*)	-	12	-	ns
t_r	Rise time		-	9	-	ns
$t_{d(off)}$	Turn-off-delay time		-	47	-	ns
t_f	Fall time		-	10.6	-	ns

Table 7: Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		9	A
I_{SDM}(1)	Source-drain current (pulsed)		-		36	A
V_{SD}(2)	Forward on voltage	V_{GS} = 0 V, I_{SD} = 13 A	-		1.6	V
t_{rr}	Reverse recovery time	I_{SD} = 13 A, di/dt = 100 A/µs, V_{DD} = 60 V (see *Figure 16: "Test circuit for inductive load switching and diode recovery times"*)	-	305		ns
Q_{rr}	Reverse recovery charge		-	3.3		µC
I_{RRM}	Reverse recovery current		-	22		A
t_{rr}	Reverse recovery time	I_{SD} = 13 A, di/dt = 100 A/µs, V_{DD} = 60 V, T_j = 150 °C (see *Figure 16: "Test circuit for inductive load switching and diode recovery times"*)	-	417		ns
Q_{rr}	Reverse recovery charge		-	4.6		µC
I_{RRM}	Reverse recovery current		-	22.2		A

Notes:

(1)Pulse width is limited by safe operating area.

(2)Pulse test: pulse duration = 300 µs, duty cycle 1.5 %.

2.1 Electrical characteristics (curves)

Figure 2: Safe operating area

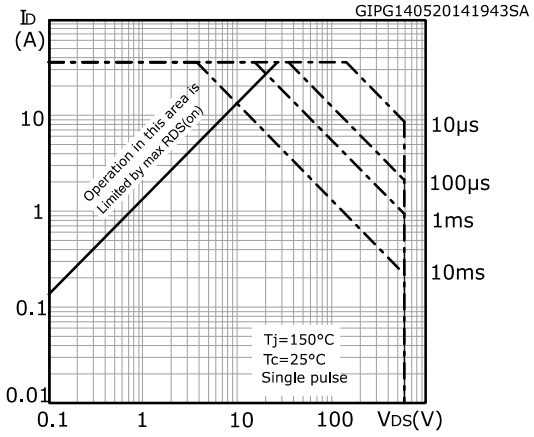


Figure 3: Thermal impedance

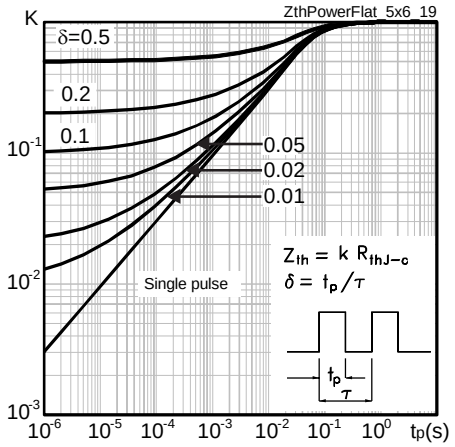


Figure 4: Output characteristics

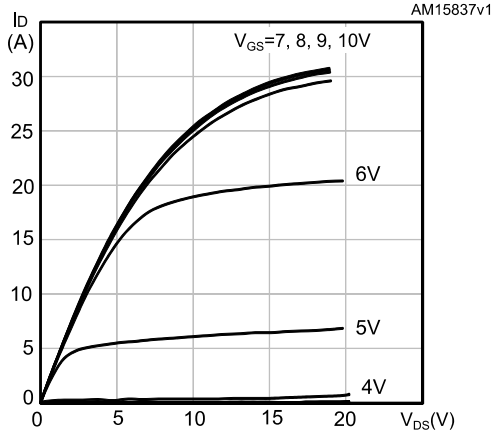


Figure 5: Transfer characteristics

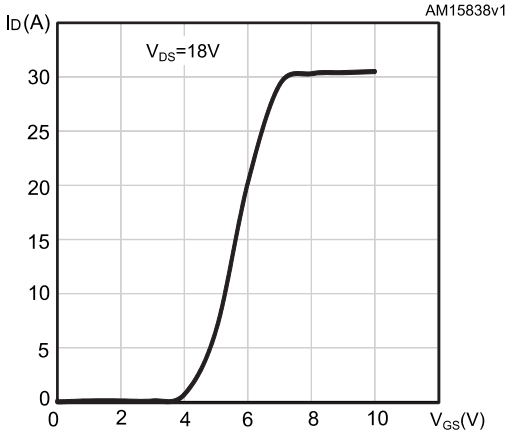


Figure 6: Gate charge vs gate-source voltage

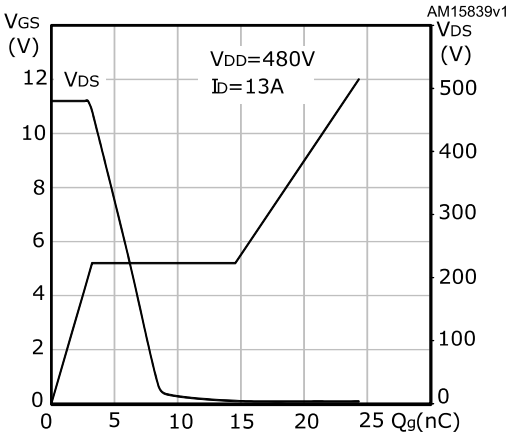


Figure 7: Static drain-source on-resistance

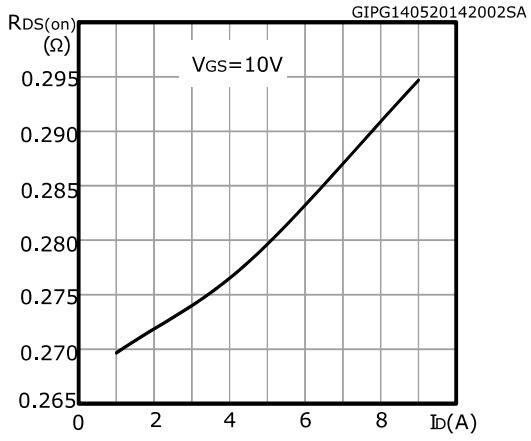


Figure 8: Capacitance variations

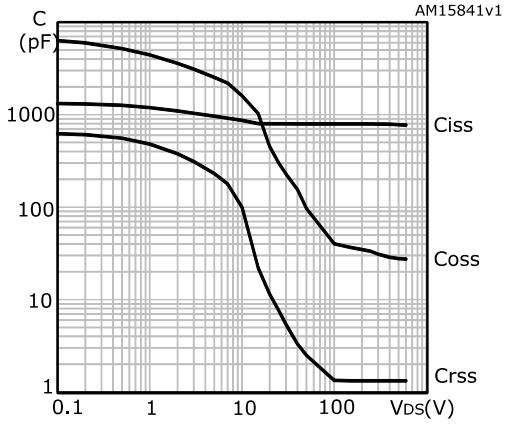


Figure 9: Output capacitance stored energy

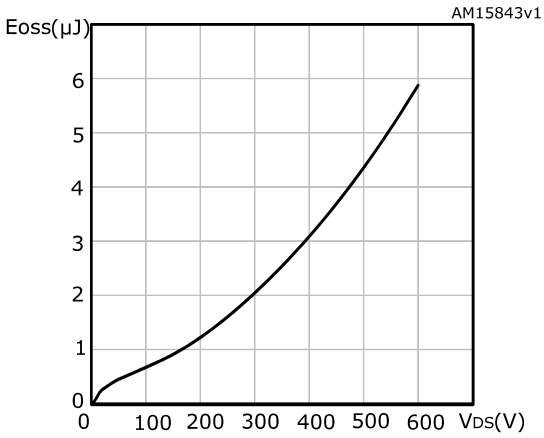


Figure 10: Normalized gate threshold voltage vs temperature

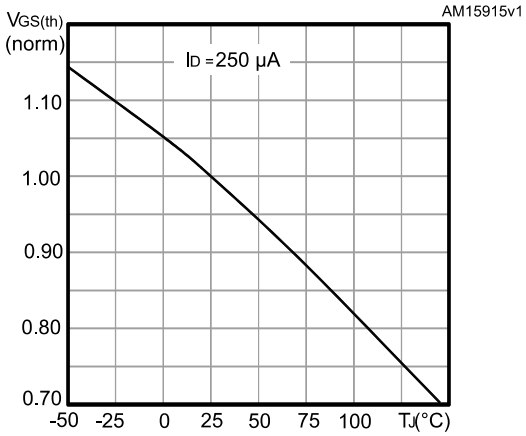


Figure 11: Normalized on-resistance vs temperature

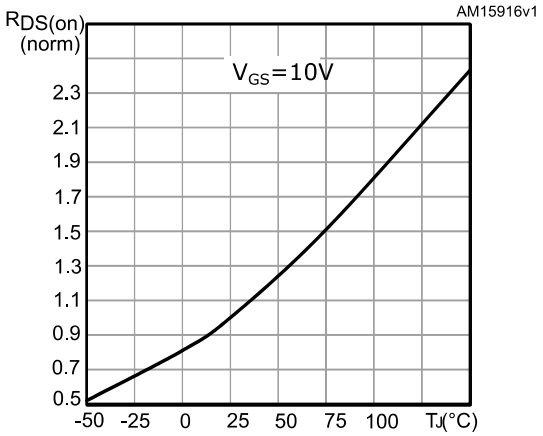


Figure 12: Normalized $V_{(BR)DSS}$ vs temperature

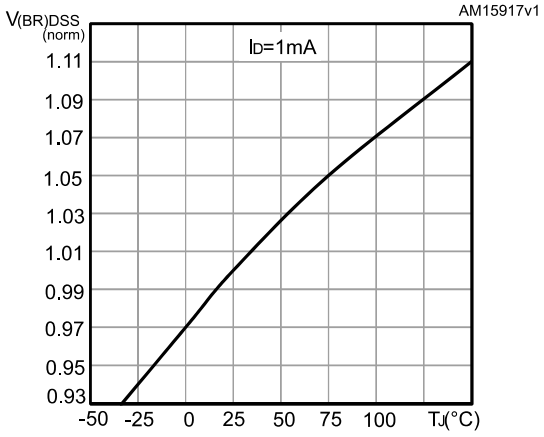
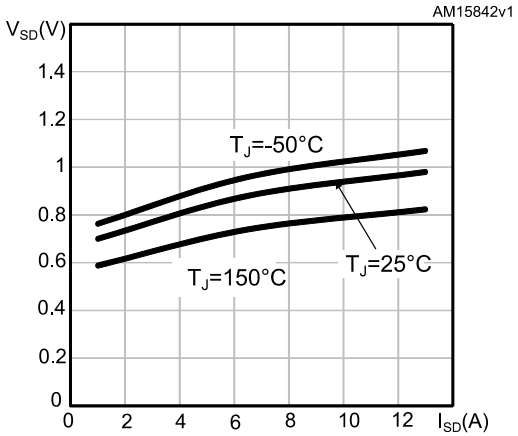


Figure 13: Source-drain diode forward characteristics



3 Test circuits

Figure 14: Test circuit for resistive load switching times

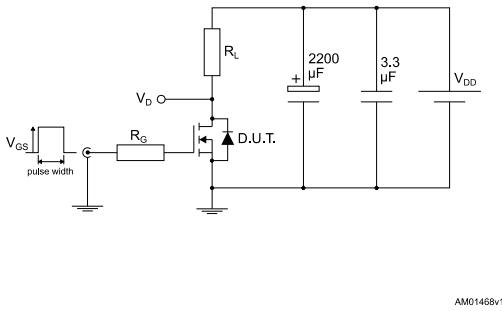


Figure 15: Test circuit for gate charge behavior

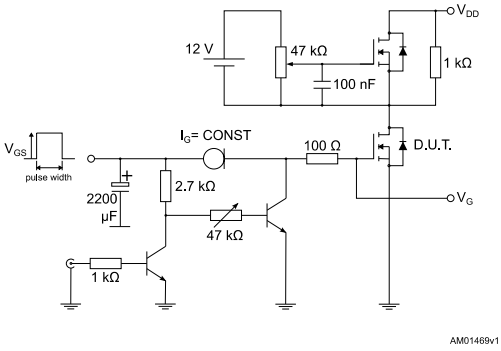


Figure 16: Test circuit for inductive load switching and diode recovery times

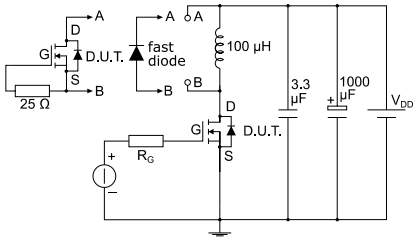


Figure 17: Unclamped inductive load test circuit

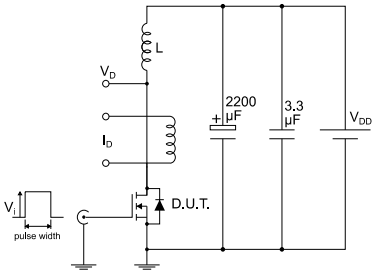


Figure 18: Unclamped inductive waveform

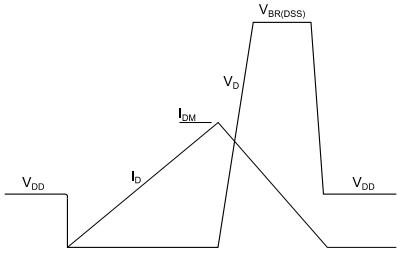
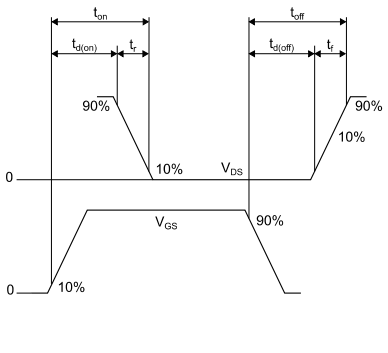


Figure 19: Switching time waveform



4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: ***www.st.com***. ECOPACK® is an ST trademark.

4.1 PowerFLAT™ 5x6 HV package information

Figure 20: PowerFLAT™ 5x6 HV package outline

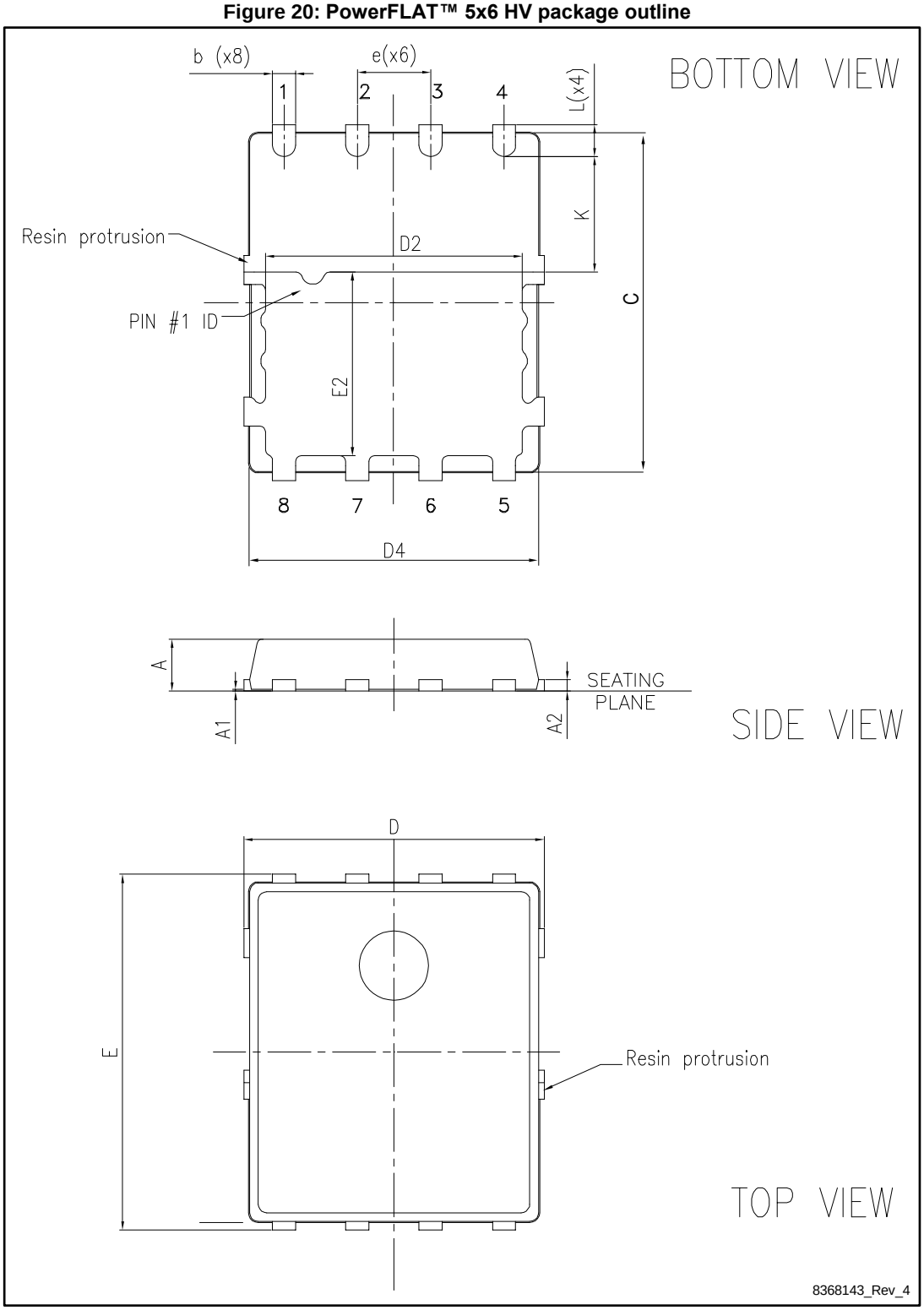
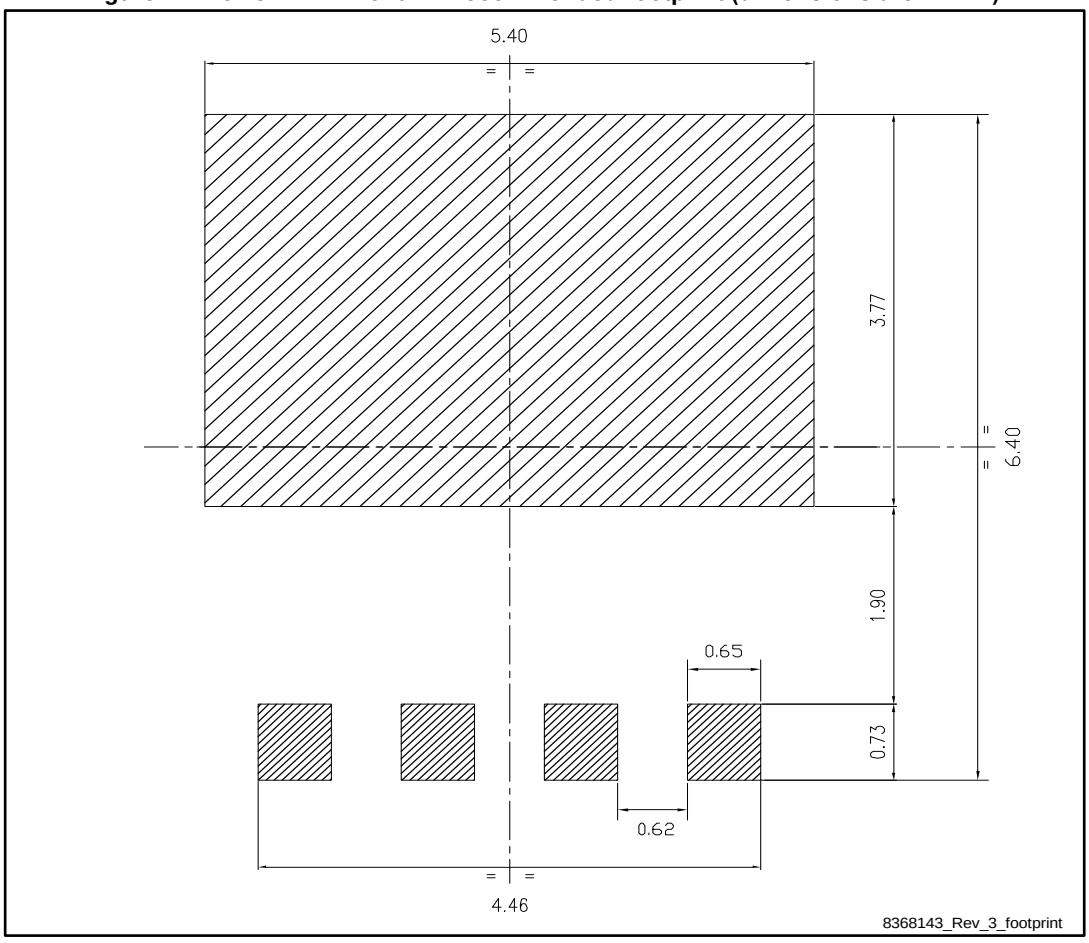


Table 8: PowerFLAT™ 5x6 HV mechanical data

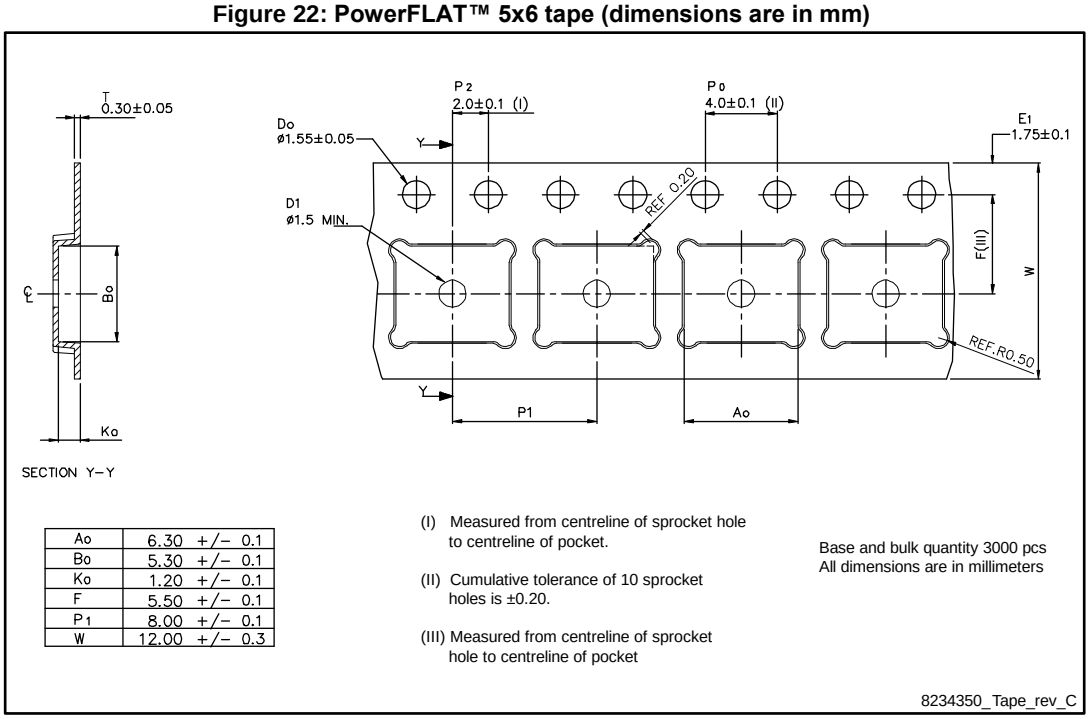
Dim.	mm		
	Min.	Typ.	Max.
A	0.80		1.00
A1	0.02		0.05
A2		0.25	
b	0.30		0.50
C	5.8	6	6.1
D	5.10	5.20	5.30
E	6.05	6.15	6.25
E2	3.10	3.20	3.30
D2	4.30	4.40	4.50
D4	4.8	5	5.1
e		1.27	
L	0.50	0.55	0.60
K	1.90	2.00	2.10

Figure 21: PowerFLAT™ 5x6 HV recommended footprint (dimensions are in mm)



4.2 PowerFLAT™ 5x6 packing information

Figure 22: PowerFLAT™ 5x6 tape (dimensions are in mm)



Ao	6.30 +/– 0.1
Bo	5.30 +/– 0.1
Ko	1.20 +/– 0.1
F	5.50 +/– 0.1
P1	8.00 +/– 0.1
W	12.00 +/– 0.3

Figure 23: PowerFLAT™ 5x6 package orientation in carrier tape

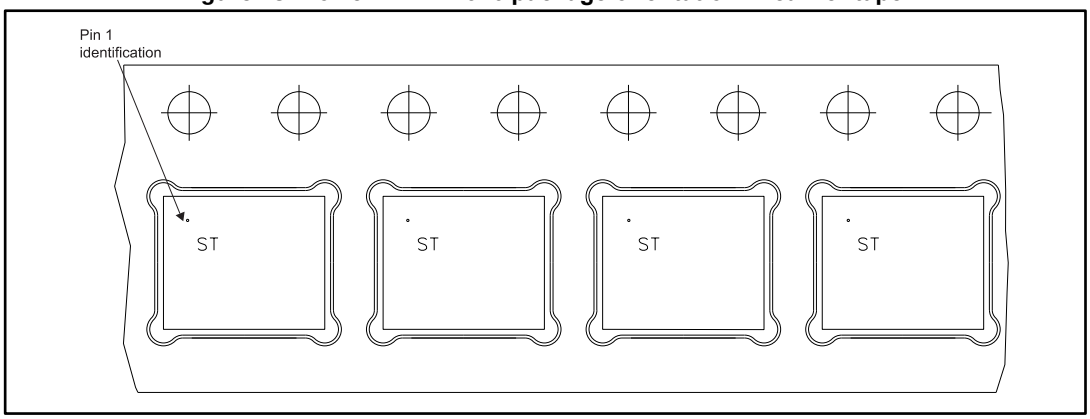
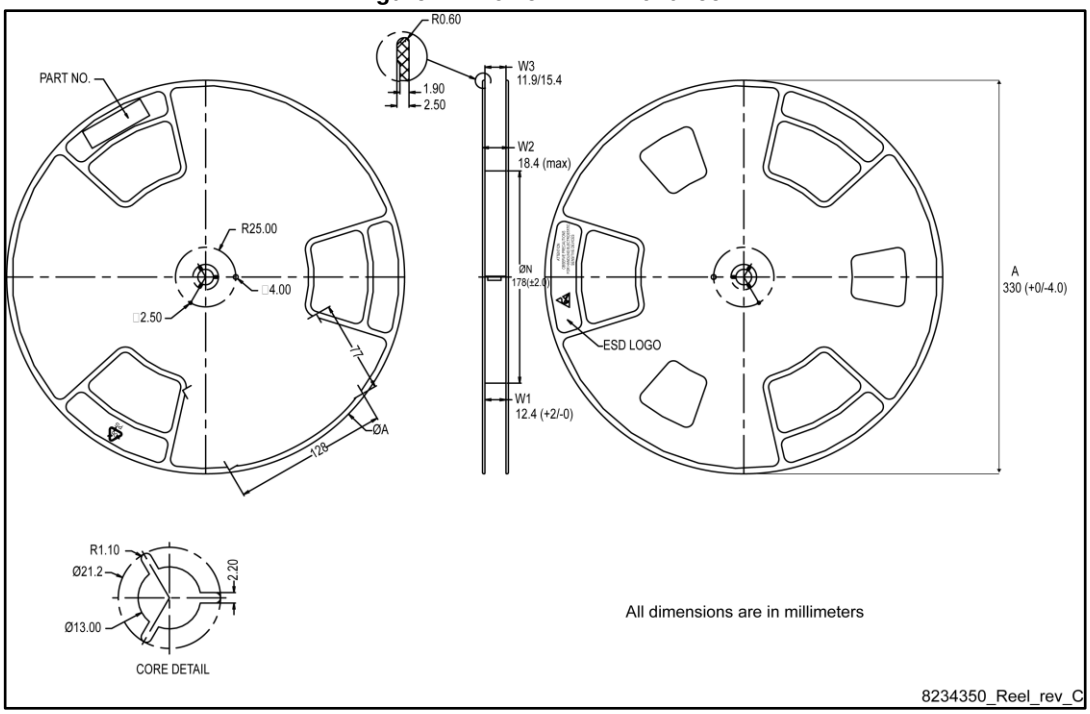


Figure 24: PowerFLAT™ 5x6 reel



5 Revision history

Table 9: Document revision history

Date	Revision	Changes
12-Jun-2014	1	First release.
02-Aug-2017	2	Updated title, features and description in cover page. Updated *Table 4: "On/off states"*, *Figure 3: "Thermal impedance"*, *Figure 11: "Normalized on-resistance vs temperature"* and *Section 4: "Package information"*. Minor text changes.

IMPORTANT NOTICE – PLEASE READ CAREFULLY

STMicroelectronics NV and its subsidiaries (“ST”) reserve the right to make changes, corrections, enhancements, modifications, and improvements to ST products and/or to this document at any time without notice. Purchasers should obtain the latest relevant information on ST products before placing orders. ST products are sold pursuant to ST’s terms and conditions of sale in place at the time of order acknowledgement.

Purchasers are solely responsible for the choice, selection, and use of ST products and ST assumes no liability for application assistance or the design of Purchasers’ products.

No license, express or implied, to any intellectual property right is granted by ST herein.

Resale of ST products with provisions different from the information set forth herein shall void any warranty granted by ST for such product.

ST and the ST logo are trademarks of ST. All other product or service names are the property of their respective owners.

Information in this document supersedes and replaces information previously supplied in any prior versions of this document.