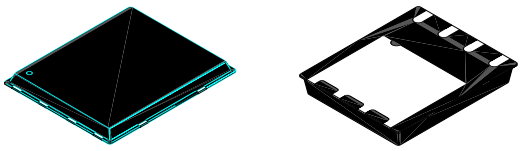
STL20NF20

N-channel 200 V, 0.10 Ω, 15 A PowerFLAT™ (5x6) low gate charge STripFET™ Power MOSFET

Features

Type	V_{DSS}	$R_{DS(on)}$	I_D	P_W
STL20NF20	200 V	< 0.125 Ω	15 A	60 W

- Exceptional dv/dt capability
- Low gate charge
- 100% avalanche tested



PowerFLAT™ (5x6)

Application

- Switching applications

Description

This Power MOSFET series realized with STMicroelectronics unique STripFET™ process has specifically been designed to minimize input capacitance and gate charge. It is therefore suitable as primary switch in advanced high-efficiency isolated DC-DC converters.

Figure 1. Internal schematic diagram

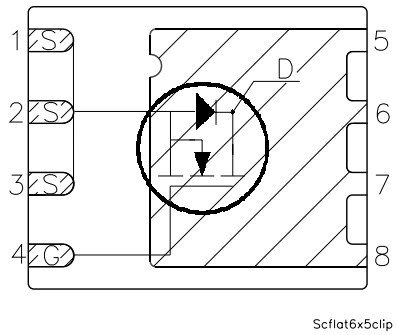


Table 1. Device summary

Order code	Marking	Package	Packaging
STL20NF20	20NF20	PowerFLAT™ (5x6)	Tape and reel

Contents

1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage (V_{GS} = 0)	200	V
V_{GS}	Gate- source voltage	± 20	V
I_D (1)	Drain current (continuous) at T_C = 25 °C	15	A
I_D (1)	Drain current (continuous) at T_C = 100 °C	11	A
I_D (3)	Drain current (continuous) at T_C = 25 °C	2.8	A
I_{DM} (2)	Drain current (pulsed)	12	A
P_{TOT} (1)	Total dissipation at T_C = 25 °C	60	W
P_{TOT} (3)	Total dissipation at T_C = 25 °C	4	W
	Derating factor	0.72	W/°C
dv/dt (4)	Peak diode recovery voltage slope	15	V/ns
T_{stg}	Storage temperature	-55 to 150	°C
T_j	Max. operating junction temperature		

1. This value is rated according Rthj-c
2. Pulse width limited by safe operating area
3. This value is according to Rthj-pcb
4. $I_{SD} \leq 15$ A, di/dt $\leq$ 400 A/µs, $V_{DD} \leq V_{(BR)DSS}$

Table 3. Thermal data

Symbol	Parameter	Value	Unit
$R_{thj\text{-}case}$	Thermal resistance junction-case max	2.08	°C/W
$R_{thj\text{-}pcb}$ (1)	Thermal resistance junction-pcb max	31.3	°C

1. When mounted on FR-4 board of 1 inch², 2 oz Cu, t < 10 sec

Table 4. Avalanche characteristics

Symbol	Parameter	Max value	Unit
I_{AR}	Avalanche current, repetitive or not-repetitive (pulse width limited by T_j max)	2.8	A
E_{AS}	Single pulse avalanche energy (starting T_j = 25 °C, $I_D = I_{AR}$, V_{DD} = 50 V)	110	mJ

2 Electrical characteristics

(T_{CASE}=25°C unless otherwise specified)

Table 5. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	I_D = 1 mA, V_{GS} = 0	200			V
I_{DSS}	Zero gate voltage drain current (V_{GS} = 0) V_{DS} = Max rating V_{DS} = Max rating, T_C = 125 °C				1 10	µA µA
I_{GSS}	Gate-body leakage current (V_{DS} = 0)	V_{GS} = ± 20 V			±100	nA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 250 µA	2	3	4	V
$R_{DS(on)}$	Static drain-source on resistance	V_{GS} = 10 V, I_D = 2.8 A		0.10	0.125	Ω

Table 6. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
g_{fs} (1)	Forward transconductance	V_{DS} = 25 V, I_D= 10 A	-	13		S
C_{iss} C_{oss} C_{rss}	Input capacitance Output capacitance Reverse transfer capacitance	V_{DS} = 25 V, f = 1 MHz, V_{GS} = 0	-	940 197 30		pF pF pF
$t_{d(on)}$ t_r $t_{d(off)}$ t_r	Turn-on delay time Rise time Turn-off delay time Fall time	V_{DD} = 100 V, I_D = 10 A, R_G= 4.7 Ω V_{GS} = 10 V *(see Figure 13)*	-	15 30 40 10		ns ns ns ns
Q_g Q_{gs} Q_{gd}	Total gate charge Gate-source charge Gate-drain charge	V_{DD} = 160 V, I_D = 10 A, V_{GS} = 10 V *(see Figure 14)*	-	28 5.6 14.5	39	nC nC nC

1. Pulsed: Pulse duration = 300 µs, duty cycle 1.5%.

Table 7. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD} I_{SDM}(1)	Source-drain current Source-drain current (pulsed)		-		2.8 12	A A
V_{SD}(2)	Forward on voltage	I_{SD} = 10 A, V_{GS} = 0	-		1.6	V
t_{rr} Q_{rr} I_{RRM}	Reverse recovery time Reverse recovery charge Reverse recovery current	I_{SD} = 10 A, di/dt = 100A/µs V_{DD} = 50 V *(see Figure 18)*	-	155 775 10		ns nC A
t_{rr} Q_{rr} I_{RRM}	Reverse recovery time Reverse recovery charge Reverse recovery current	I_{SD} = 10 A, di/dt = 100 A/µs V_{DD} = 50 V, T_j = 150 °C *(see Figure 18)*	-	183 1061 11.6		ns nC A

1. Pulse width limited by safe operating area.
2. Pulsed: Pulse duration = 300 µs, duty cycle 1.5%.

2.1 Electrical characteristics (curves)

Figure 2. Safe operating area

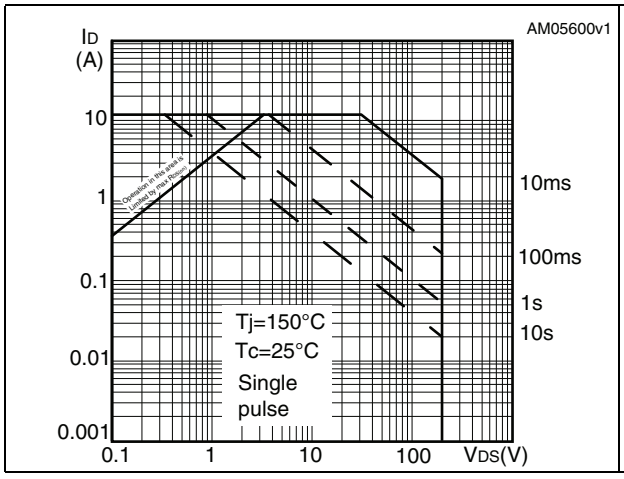


Figure 3. Thermal impedance area

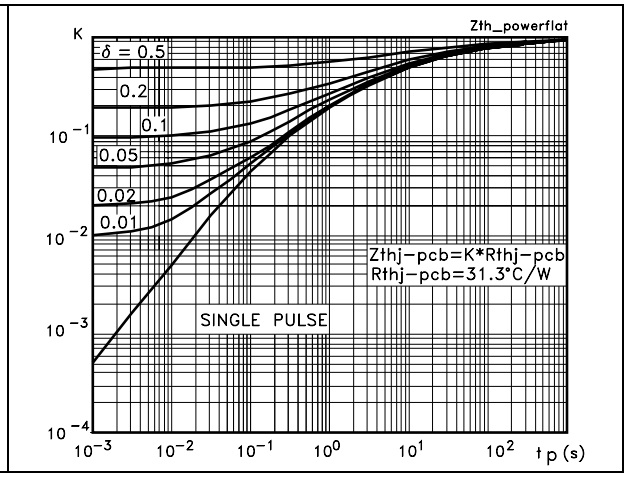


Figure 4. Output characteristics

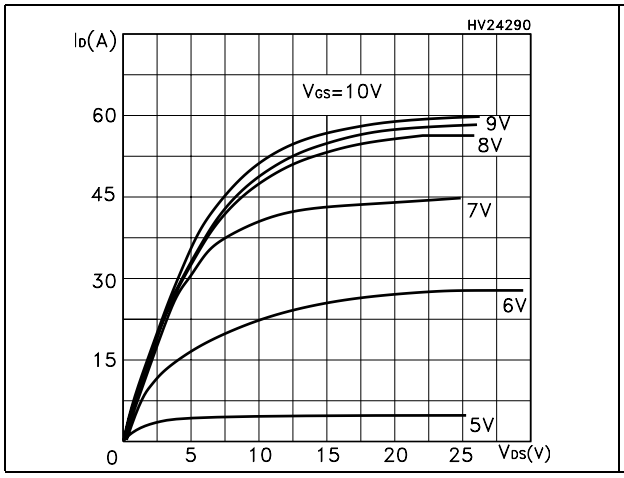


Figure 5. Transfer characteristics

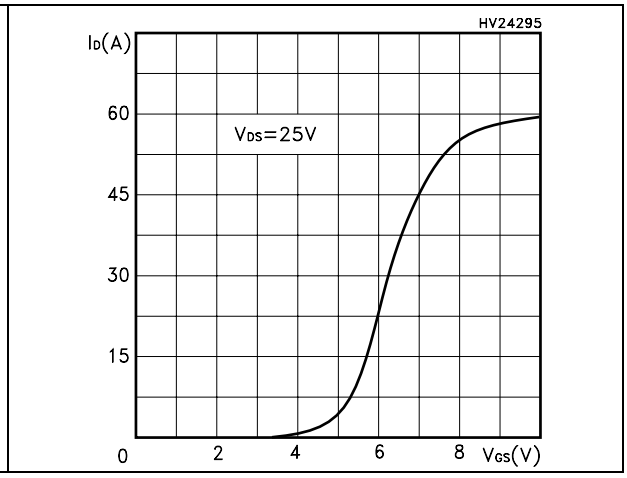


Figure 6. Transconductance

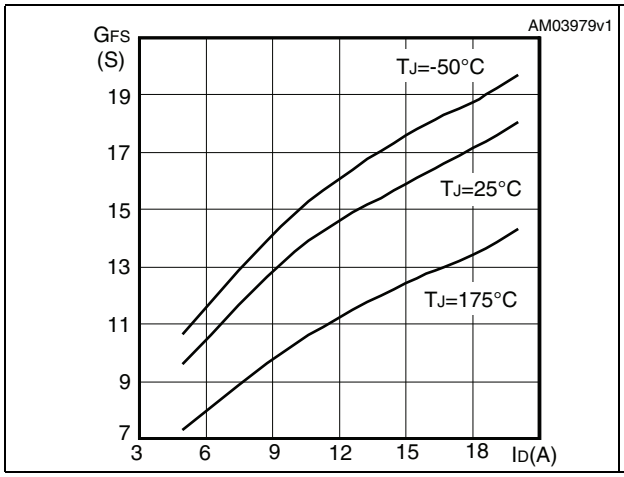


Figure 7. Static drain-source on resistance

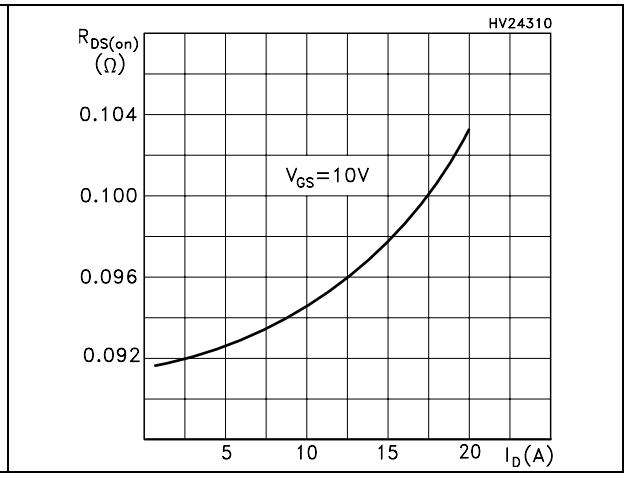


Figure 8. Gate charge vs gate-source voltage

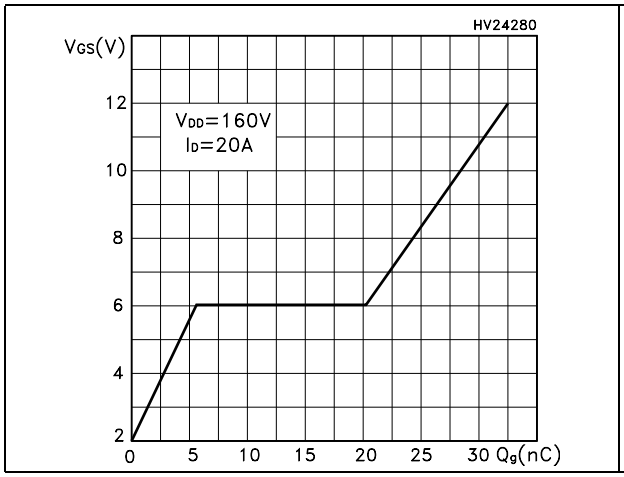


Figure 9. Capacitance variations

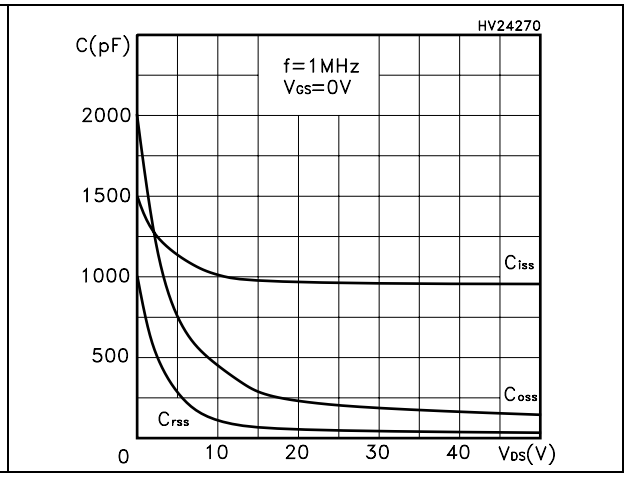


Figure 10. Normalized gate threshold voltage vs temperature

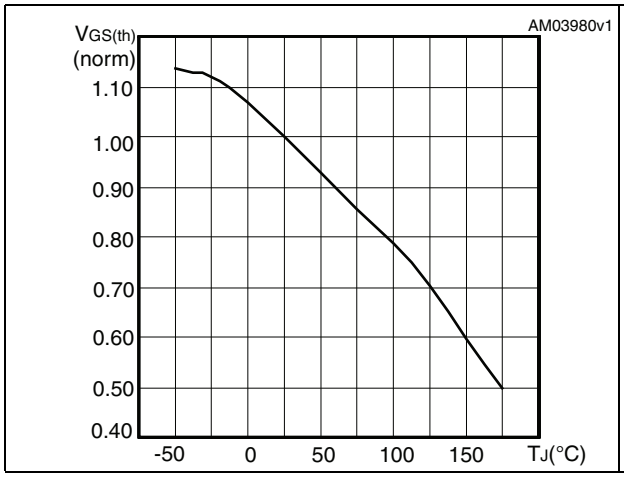


Figure 11. Normalized on resistance vs temperature

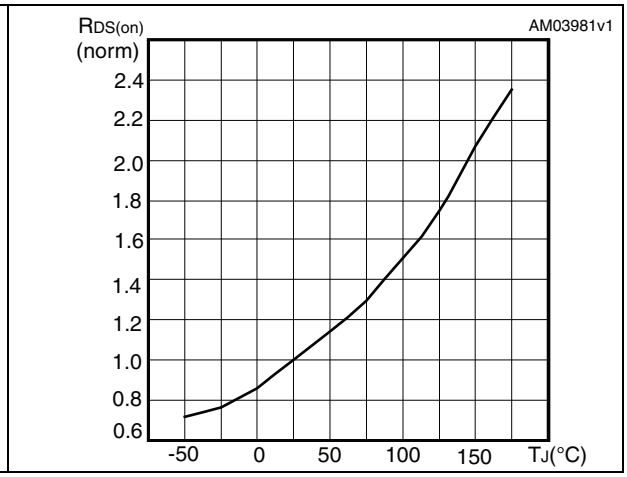
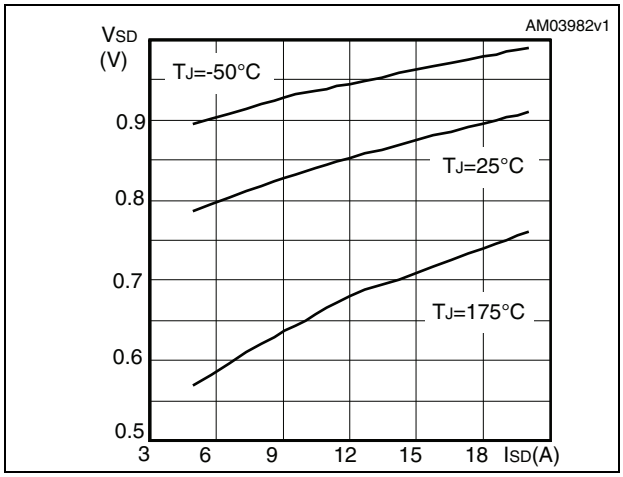


Figure 12. Source-drain diode forward characteristics



3 Test circuits

Figure 13. Switching times test circuit for resistive load

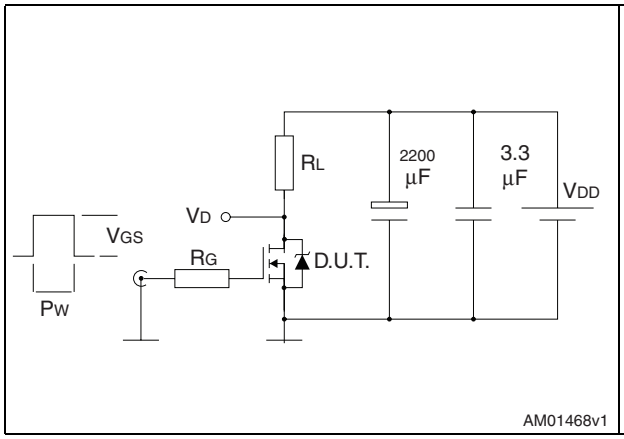


Figure 14. Gate charge test circuit

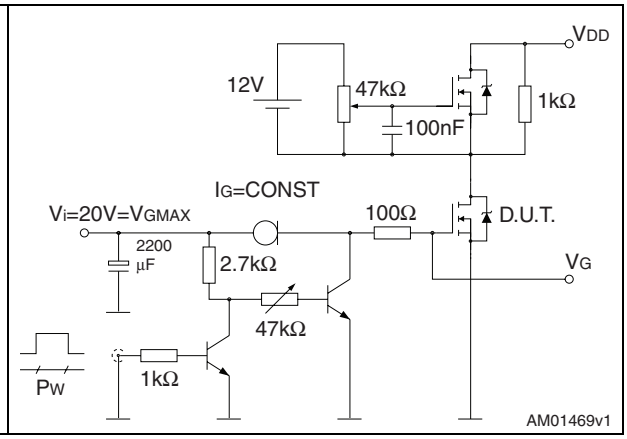


Figure 15. Test circuit for inductive load switching and diode recovery times

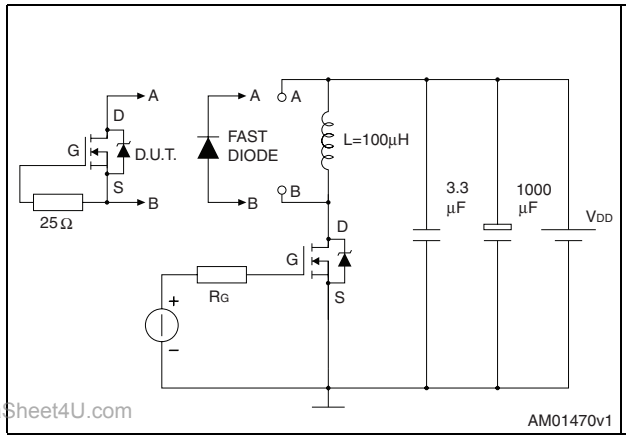


Figure 16. Unclamped inductive load test circuit

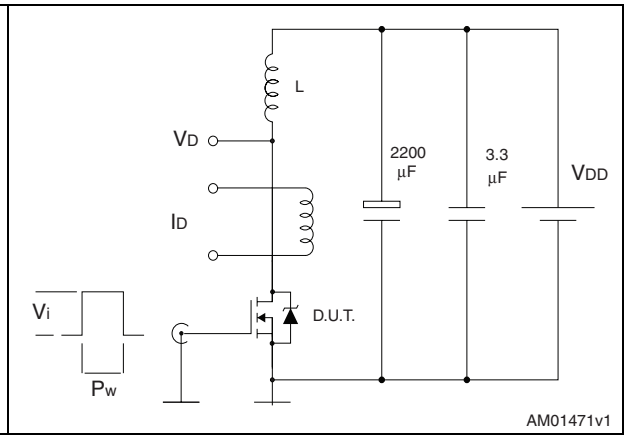


Figure 17. Unclamped inductive waveform

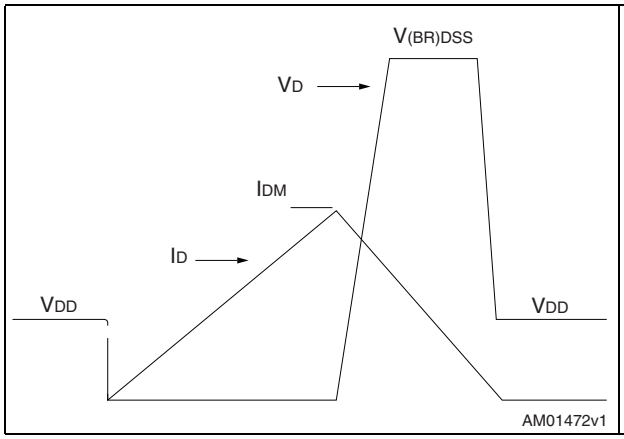
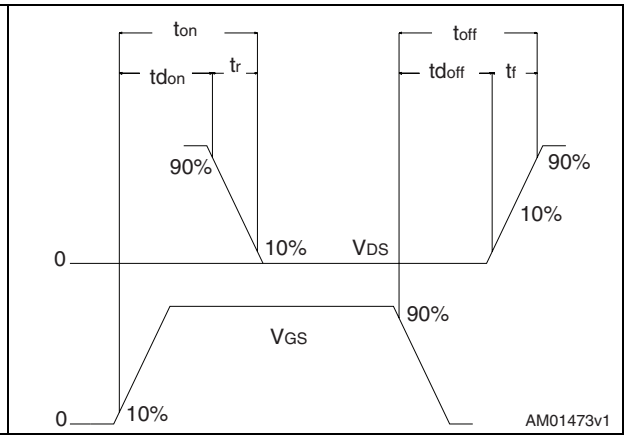


Figure 18. Switching time waveform

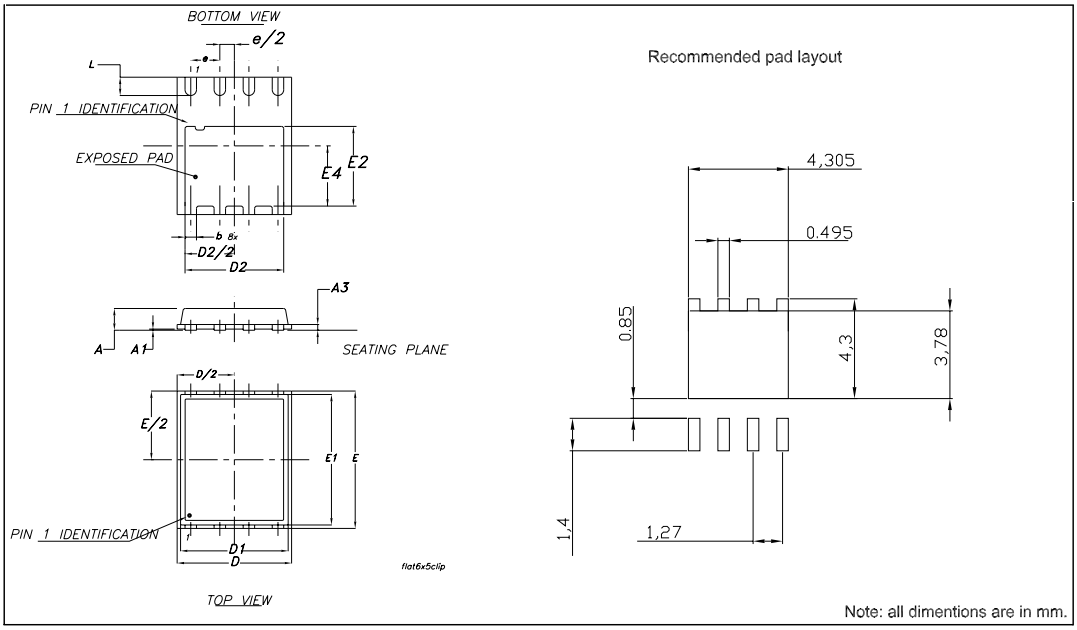


4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

PowerFLAT™(6x5) mechanical data

DIM.	mm.			inch		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	0.80	0.83	0.93	0.031	0.32	0.036
A1		0.02	0.05		0.0007	0.0019
A3		0.20			0.007	
b	0.35	0.40	0.47	0.013	0.015	0.018
D		5.00			0.196	
D1		4.75			0.187	
D2	4.15	4.20	4.25	0.163	0.165	0.167
E		6.00			0.236	
E1		5.75			0.226	
E2	3.43	3.48	3.53	0.135	0.137	0.139
E4	2.58	2.63	2.68		0.103	0.105
e		1.27			0.050	
L	0.70	0.80	0.90	0.027	0.031	0.035



5 Revision history

Table 8. Document revision history

Date	Revision	Changes
11-Dec-2009	1	First release.

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