

## Automotive-grade N-channel 40 V, 1.3 mΩ typ., 120 A STripFET™ F7 Power MOSFET in a PowerFLAT™ 5x6 package

Datasheet - production data

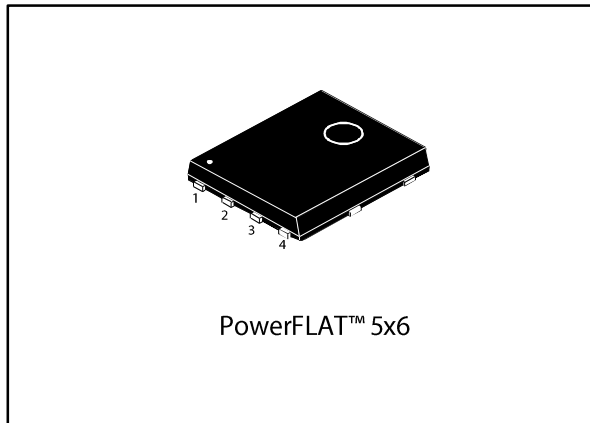
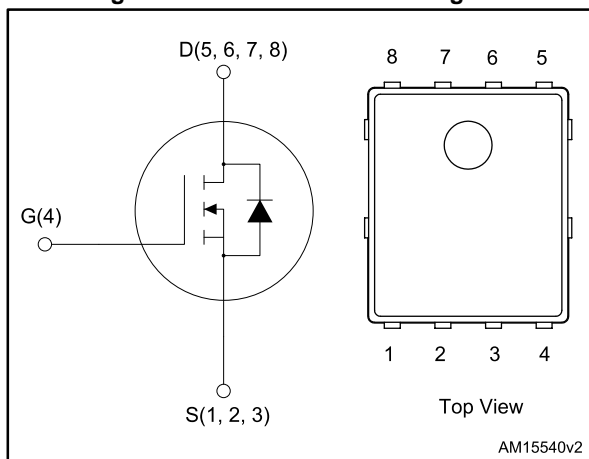


Figure 1: Internal schematic diagram



### Features

Order code	V <sub>DS</sub>	R <sub>DS(on)</sub> max	I <sub>D</sub>
STL210N4F7AG	40 V	1.6 mΩ	120 A

- Designed for automotive applications and AEC-Q101 qualified
- Among the lowest R<sub>DS(on)</sub> on the market
- Excellent figure of merit (FoM)
- Low C<sub>rss</sub>/C<sub>iss</sub> ratio for EMI immunity
- High avalanche ruggedness
- Wettable flank package

### Applications

- Switching applications

### Description

This N-channel Power MOSFET utilizes STripFET™ F7 technology with an enhanced trench gate structure that results in very low on-state resistance, while also reducing internal capacitance and gate charge for faster and more efficient switching.

Table 1: Device summary

Order code	Marking	Package	Packaging
STL210N4F7AG	210N4F7	PowerFLAT™ 5x6	Tape and reel

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# 1 Electrical ratings

**Table 2: Absolute maximum ratings**

Symbol	Parameter	Value	Unit
V <sub>DS</sub>	Drain-source voltage	40	V
V <sub>GS</sub>	Gate-source voltage	± 20	V
I <sub>D</sub> <sup>(1)</sup>	Drain current (continuous) at T <sub>C</sub> = 25 °C	120	A
I <sub>D</sub> <sup>(1)</sup>	Drain current (continuous) at T <sub>C</sub> = 100 °C	120	A
I <sub>DM</sub> <sup>(1)(2)</sup>	Drain current (pulsed)	480	A
P <sub>TOT</sub>	Total dissipation at T <sub>C</sub> = 25 °C	150	W
I <sub>AV</sub>	Avalanche current, repetitive or not repetitive (pulse width limited by maximum junction temperature)	40	A
E <sub>AS</sub>	Single pulse avalanche energy (T <sub>j</sub> = 25 °C, I <sub>D</sub> = 20 A, V <sub>DD</sub> = 25 V)	300	mJ
T <sub>j</sub>	Operating junction temperature	-55 to 175	°C
T <sub>stg</sub>	Storage temperature		

**Notes:**

<sup>(1)</sup>Drain current is limited by package, the current capability of the silicon is 229 A at 25 °C.

<sup>(2)</sup>Pulse width limited by safe operating area

**Table 3: Thermal data**

Symbol	Parameter	Value	Unit
R <sub>thj-pcb</sub> <sup>(1)</sup>	Thermal resistance junction-pcb max.	31.3	°C/W
R <sub>thj-case</sub>	Thermal resistance junction-case max.	1.0	°C/W

**Notes:**

<sup>(1)</sup>When mounted on FR-4 board of 1 inch<sup>2</sup>, 2oz Cu, t < 10 sec

## 2 Electrical characteristics

( $T_C = 25\text{ }^\circ\text{C}$  unless otherwise specified)

**Table 4: On /off states**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$V_{GS} = 0\text{ V}$ , $I_D = 250\text{ }\mu\text{A}$	40			V
$I_{DSS}$	Zero gate voltage drain current	$V_{GS} = 0\text{ V}$ $V_{DS} = 40\text{ V}$			1	$\mu\text{A}$
$I_{GSS}$	Gate-body leakage current	$V_{GS} = 20\text{ V}$ , $V_{DS} = 0\text{ V}$			100	nA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}$ , $I_D = 250\text{ }\mu\text{A}$	2		4	V
$R_{DS(on)}$	Static drain-source on-resistance	$V_{GS} = 10\text{ V}$ , $I_D = 16\text{ A}$		1.3	1.6	m $\Omega$

**Table 5: Dynamic**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$C_{iss}$	Input capacitance	$V_{DS} = 25\text{ V}$ , $f = 1\text{ MHz}$ , $V_{GS} = 0\text{ V}$	-	3600	-	pF
$C_{oss}$	Output capacitance		-	1240	-	pF
$C_{riss}$	Reverse transfer capacitance		-	56	-	pF
$Q_g$	Total gate charge	$V_{DD} = 20\text{ V}$ , $I_D = 40\text{ A}$ , $V_{GS} = 10\text{ V}$ (see <a href="#">Figure 14: "Test circuit for gate charge behavior"</a> )	-	43	-	nC
$Q_{gs}$	Gate-source charge		-	19	-	nC
$Q_{gd}$	Gate-drain charge		-	5	-	nC

**Table 6: Switching times**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 20\text{ V}$ , $I_D = 20\text{ A}$ , $R_G = 4.7\text{ }\Omega$ , $V_{GS} = 10\text{ V}$ (see <a href="#">Figure 13: "Test circuit for resistive load switching times"</a> and <a href="#">Figure 18: "Switching time waveform"</a> )	-	27	-	ns
$t_r$	Rise time		-	6	-	ns
$t_{d(off)}$	Turn-off delay time		-	34	-	ns
$t_f$	Fall time		-	6	-	ns

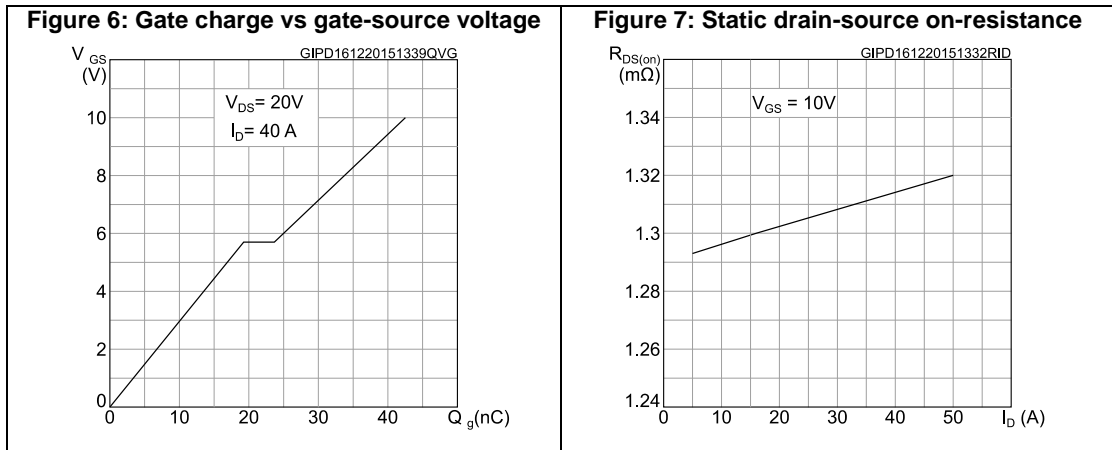
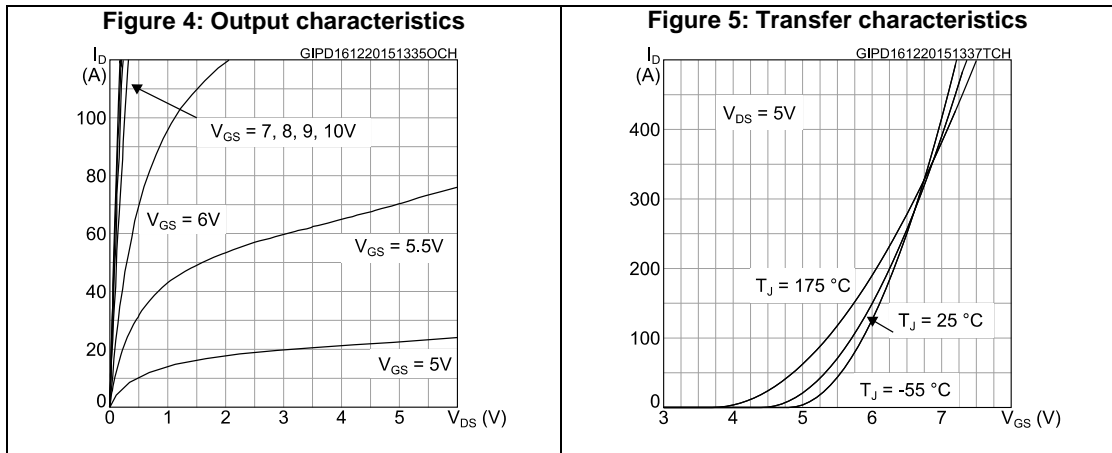
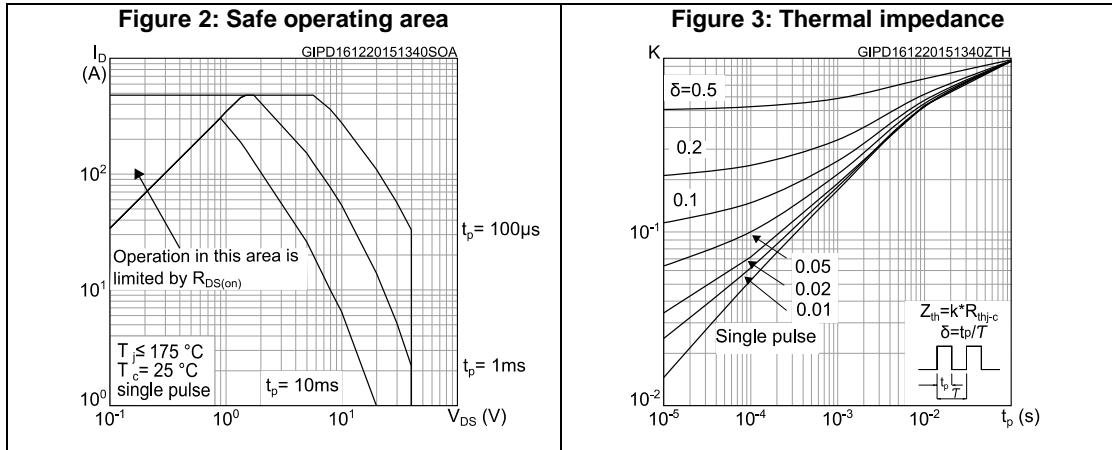
Table 7: Source-drain diode

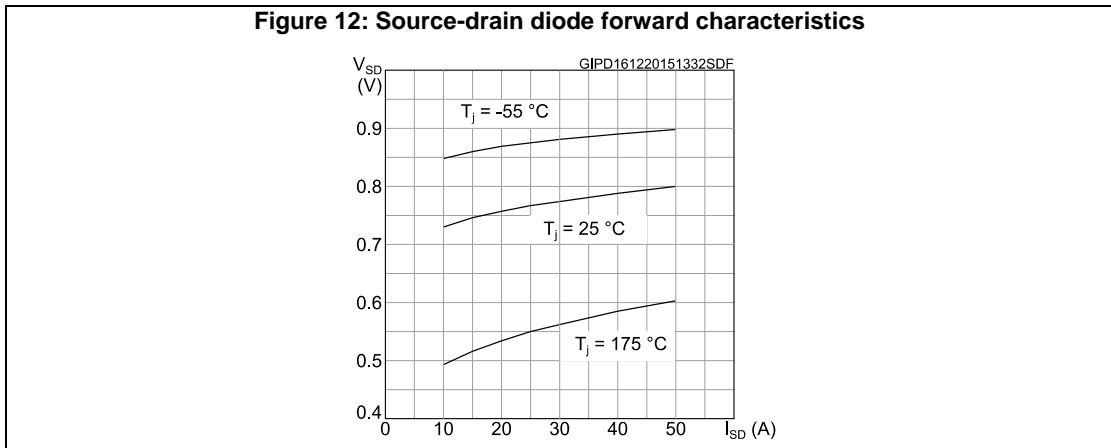
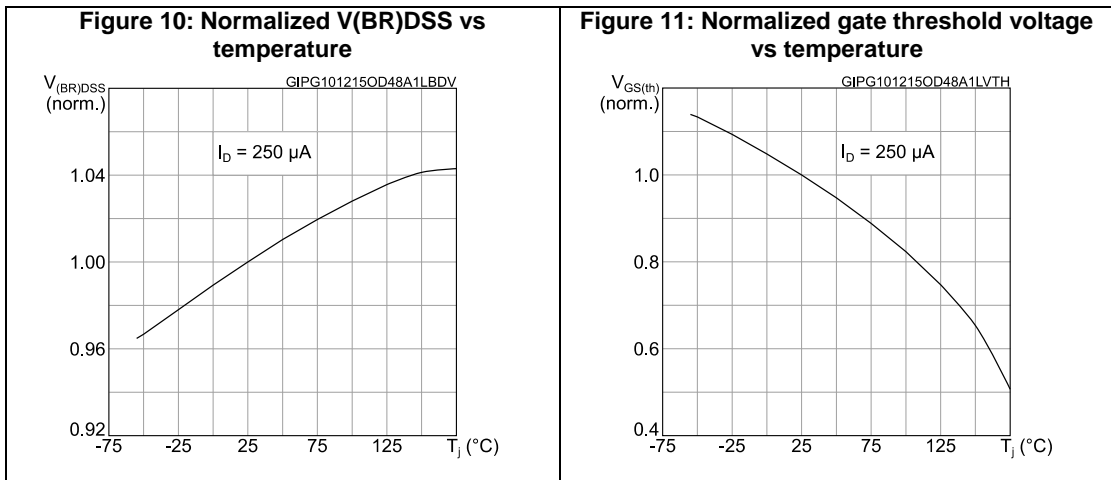
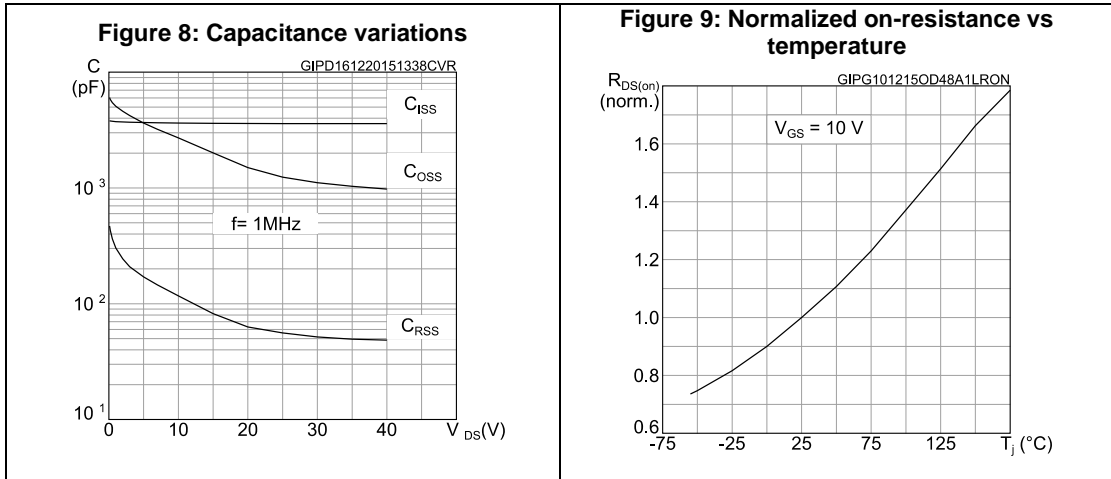
Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{SD}^{(1)}$	Forward on voltage	$I_{SD} = 40 \text{ A}$ , $V_{GS} = 0 \text{ V}$	-		1.2	V
$t_{rr}$	Reverse recovery time	$I_D = 40 \text{ A}$ , $di/dt = 100 \text{ A}/\mu\text{s}$ $V_{DD} = 32 \text{ V}$ (see <i>Figure 15: "Test circuit for inductive load switching and diode recovery times"</i> )	-	53		ns
$Q_{rr}$	Reverse recovery charge		-	71		nC
$I_{RRM}$	Reverse recovery current		-	2.7		A

**Notes:**

<sup>(1)</sup>Pulsed: pulse duration = 300  $\mu\text{s}$ , duty cycle 1.5%

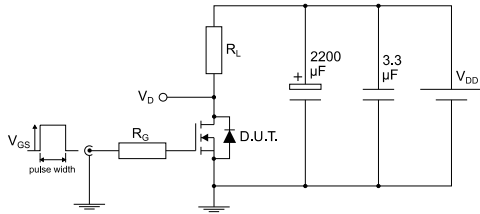
## 2.1 Electrical characteristics (curves)





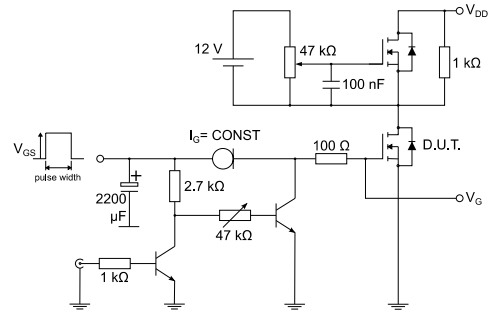
### 3 Test circuits

**Figure 13: Test circuit for resistive load switching times**



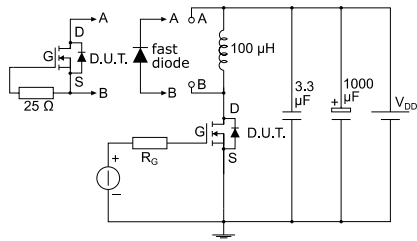
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**Figure 14: Test circuit for gate charge behavior**



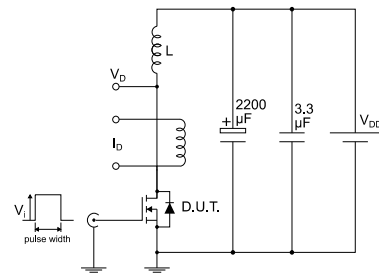
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**Figure 15: Test circuit for inductive load switching and diode recovery times**



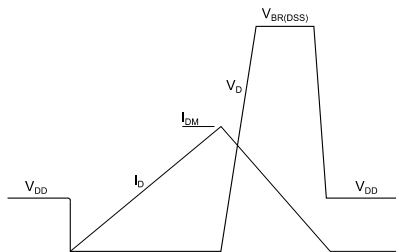
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**Figure 16: Unclamped inductive load test circuit**



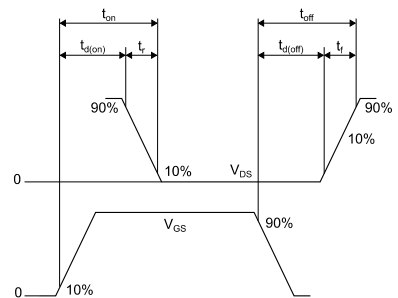
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**Figure 17: Unclamped inductive waveform**



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**Figure 18: Switching time waveform**



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## 4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com). ECOPACK® is an ST trademark.

### 4.1 PowerFLAT™ 5x6 WF type C package information

Figure 19: PowerFLAT™ 5x6 WF type C package outline

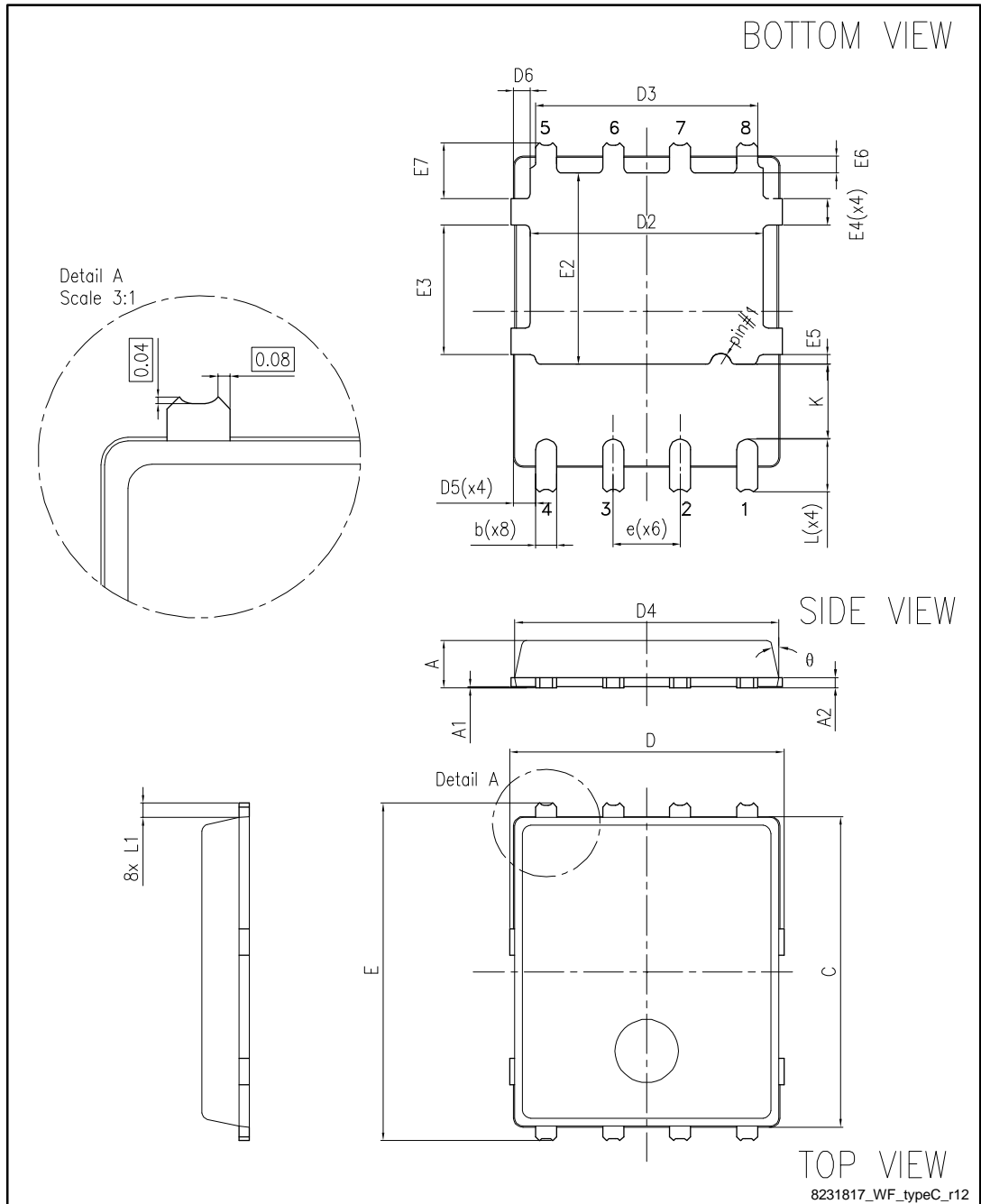
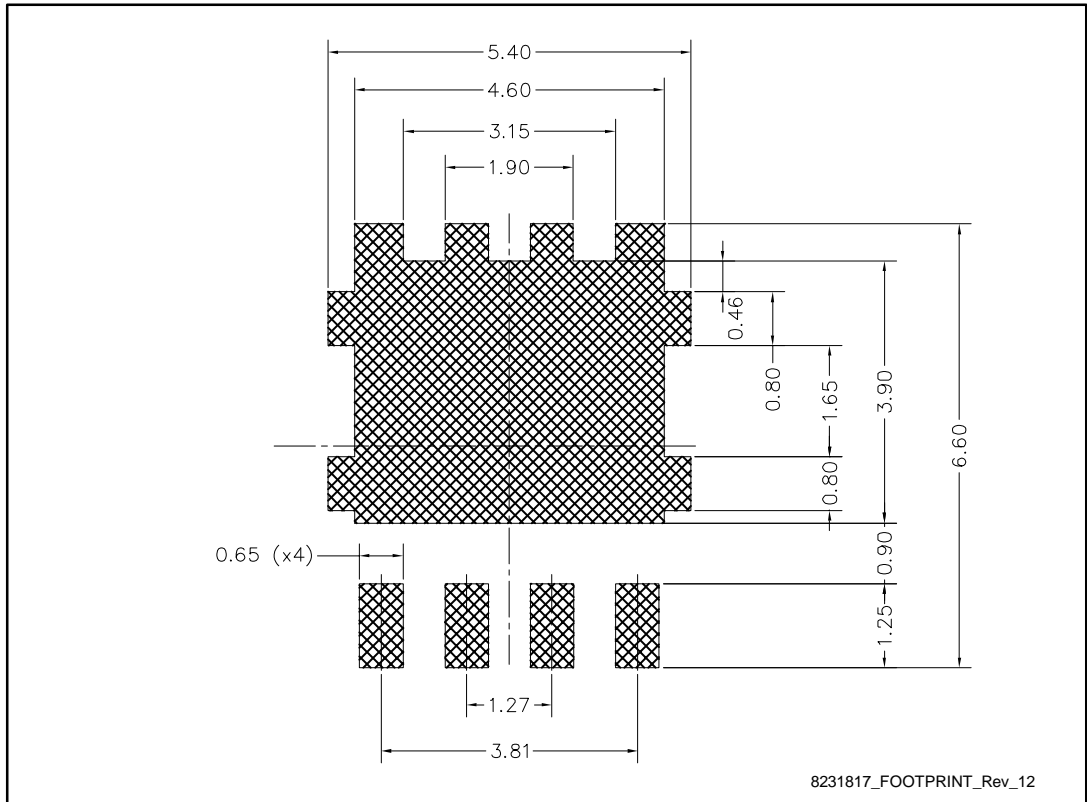


Table 8: PowerFLAT™ 5x6 WF type C mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	0.80		1.00
A1	0.02		0.05
A2		0.25	
b	0.30		0.50
C	5.80	6.00	6.20
D	5.00	5.20	5.40
D2	4.15		4.45
D3	4.05	4.20	4.35
D4	4.80	5.0	5.20
D5	0.25	0.4	0.55
D6	0.15	0.3	0.45
e		1.27	
E	6.20	6.40	6.60
E2	3.50		3.70
E3	2.35		2.55
E4	0.40		0.60
E5	0.08		0.28
E6	0.2	0.325	0.450
E7	0.85	1.00	1.15
K	1.05		1.35
L	0.90	1.00	1.10
L1	0.175	0.275	0.375
θ	0°		12°

Figure 20: PowerFLAT™ 5x6 recommended footprint (dimensions are in mm)



## 4.2 PowerFLAT™ 5x6 packing information

Figure 21: PowerFLAT™ 5x6 WF tape

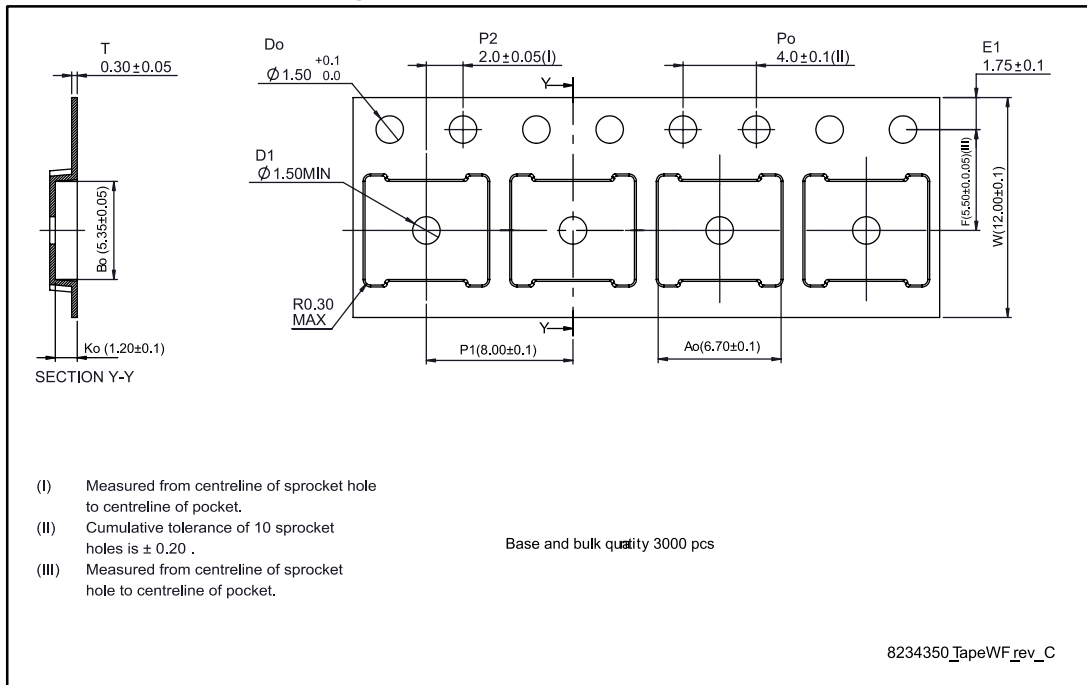


Figure 22: PowerFLAT™ 5x6 package orientation in carrier tape

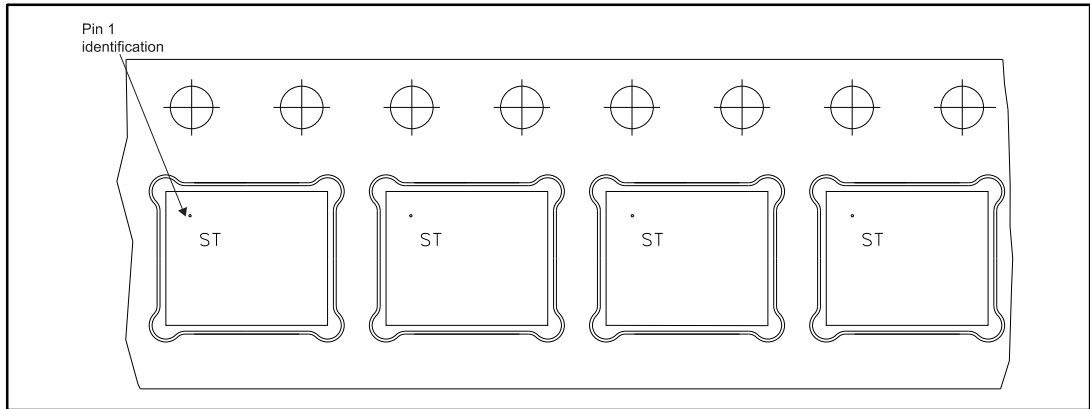
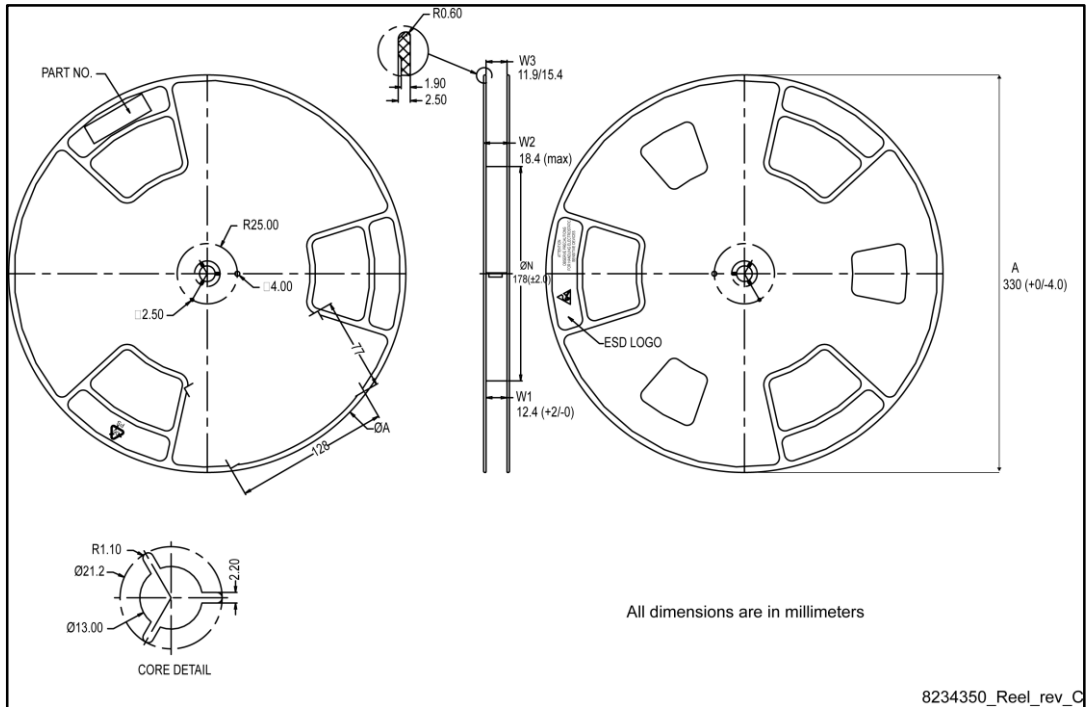


Figure 23: PowerFLAT™ 5x6 reel



## 5 Revision history

Table 9: Document revision history

Date	Revision	Changes
07-Jan-2016	1	First release.

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