STL23N85K5

N-channel 850 V, 0.23 Ω, 18 A PowerFLAT™ 8x8 HV Zener-protected SuperMESH 5™ Power MOSFET

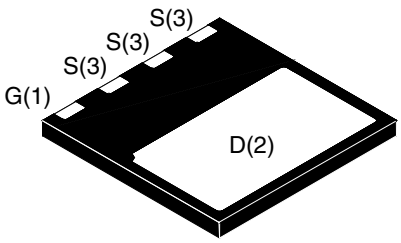
Preliminary data

Features

Type	V_{DSS}	$R_{DS(on)}$max	I_D	P_W
STL23N85K5	850 V	< 0.275 Ω	18(1)	210

1. The value is rated according to $R_{thj\text{-}c}$.

- PowerFLAT™ 8x8 HV worldwide best $R_{DS(on)}$
- Worldwide best FOM (figure of merit)
- Ultra low gate charge
- 100% avalanche tested
- Zener-protected



PowerFLAT™8x8 HV

Application

- Switching applications

Description

SuperMESH 5™ is a revolutionary avalanche-rugged very high voltage Power MOSFET technology based on an innovative proprietary vertical structure. The result is a drastic reduction in on-resistance and ultra low gate charge for applications which require superior power density and high efficiency.

Figure 1. Internal schematic diagram

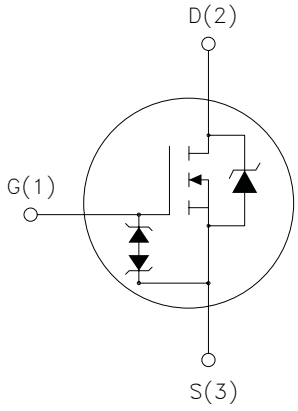


Table 1. Device summary

Order code	Marking	Package	Packaging
STL23N85K5	23N85K5	PowerFLAT™ 8x8 HV	Tube

Contents

1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{GS}	Gate-source voltage	± 30	V
I_D (1)	Drain current (continuous) at T_C = 25 °C	18	A
I_D (1)	Drain current (continuous) at T_C = 100 °C	11	A
I_{DM} (1),(2)	Drain current (pulsed)	72	A
I_D(3)	Drain current (continuous) at T_C = 25 °C	2.1	A
I_D(3)	Drain current (continuous) at T_C = 100 °C	1.35	A
I_{DM}(2),(3)	Drain current (pulsed)	8.4	A
P_{TOT}(1)	Total dissipation at T_C = 25 °C (steady state)	210	W
P_{TOT}(3)	Total dissipation at T_C = 25 °C (steady state)	3	W
I_{AR}	Avalanche current, repetitive or not-repetitive (pulse width limited by T_j max)	TBD	A
E_{AS}	Single pulse avalanche energy (starting T_j = 25 °C, I_D = I_{AR}, V_{DD} = 50 V)	TBD	mJ
dv/dt (4)	Peak diode recovery voltage slope	TBD	V/ns
T_{stg}	Storage temperature	- 55 to 150	°C
T_j	Max. operating junction temperature	150	°C

1. The value is rated according to $R_{thj\text{-}case}$.
2. Pulse width limited by safe operating area.
3. When mounted on FR-4 board of inch², 2oz Cu.
4. I_{SD} ≤ TBD A, di/dt ≤ 100 A/µs, $V_{Peak} < V_{(BR)DSS}$.

Table 3. Thermal data

Symbol	Parameter	Value	Unit
$R_{thj\text{-}case}$	Thermal resistance junction-case max (drain)	0.6	°C/W
$R_{thj\text{-}amb}$ (1)	Thermal resistance junction-amb max	45	°C/W
T_l	Maximum lead temperature for soldering purpose	300	°C

1. When mounted on FR-4 board of inch², 2oz Cu.

2 Electrical characteristics

(T_{CASE} = 25 °C unless otherwise specified).

Table 4. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	I_D = 1 mA, V_{GS}= 0	850			V
I_{DSS}	Zero gate voltage drain current (V_{GS} = 0)	V_{DS} = max rating, V_{DS} = Max rating,Tc=125 °C			1 50	µA µA
I_{GSS}	Gate body leakage current (V_{DS} = 0)	V_{GS} = ± 20 V			±10	µA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 100 µA	3	4	5	V
$R_{DS(on)}$	Static drain-source on resistance	V_{GS} = 10 V, I_D= 8.5 A		0.230	0.275	Ω

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	V_{DS} =100 V, f=1 MHz, V_{GS}=0	-	1650	-	pF
C_{oss}	Output capacitance			115		pF
C_{rss}	Reverse transfer capacitance			2		pF
$C_{o(tr)}$(1)	Equivalent capacitance time related	V_{GS} = 0, V_{DS} = 0 to 680 V	-	TBD	-	pF
$C_{o(er)}$(2)	Equivalent capacitance energy related		-	TBD	-	pF
R_G	Intrinsic gate resistance	f = 1 MHz open drain	-	3.5	-	Ω
Q_g	Total gate charge	V_{DD} = 680 V, I_D = 8.5 A	-	35	-	nC
Q_{gs}	Gate-source charge	V_{GS} =10 V		TBD		nC
Q_{gd}	Gate-drain charge	*(see Figure 3)*		TBD		nC

1. Time related is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}.
2. Energy related is defined as a constant equivalent capacitance giving the same stored energy as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}.

Table 6. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	V_{DD} = 400 V, I_D = 8.5 A, R_G=4.7 Ω, V_{GS}=10 V *(see Figure 5)*	-	TBD	-	ns
t_r	Rise time			TBD		ns
$t_{d(off)}$	Turn-off delay time			TBD		ns
t_f	Fall time			TBD		ns

Table 7. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		TBD	A
I_{SDM}	Source-drain current (pulsed)				TBD	A
V_{SD} (1)	Forward on voltage	I_{SD}= 8.5 A, V_{GS}=0	-		1.5	V
t_{rr}	Reverse recovery time	I_{SD}= 17 A, V_{DD}= 60 V di/dt = 100 A/µs, *(see Figure 4)*	-	TBD		ns
Q_{rr}	Reverse recovery charge			TBD		µC
I_{RRM}	Reverse recovery current			TBD		A
t_{rr}	Reverse recovery time	I_{SD}= 17 A,V_{DD}= 60 V di/dt=100 A/µs, T_j=150 °C*(see Figure 4)*	-	TBD		ns
Q_{rr}	Reverse recovery charge			TBD		µC
I_{RRM}	Reverse recovery current			TBD		A

1. Pulsed: pulse duration = 300µs, duty cycle 1.5%.

Table 8. Gate-source Zener diode

Symbol	Parameter	Test conditions	Min	Typ.	Max	Unit
BV_{GSO}	Gate-source breakdown voltage	Igs ± 1mA, (open drain)	30	-	-	V

The built-in-back Zener diodes have specifically been designed to enhance not only the device's ESD capability, but also to make them safely absorb possible voltage transients that may occasionally be applied from gate to source. In this respect the Zener voltage is appropriate to achieve an efficient and cost-effective intervention to protect the device's integrity. These integrated Zener diodes thus avoid the usage of external components.

3 Test circuits

Figure 2. Switching times test circuit for resistive load

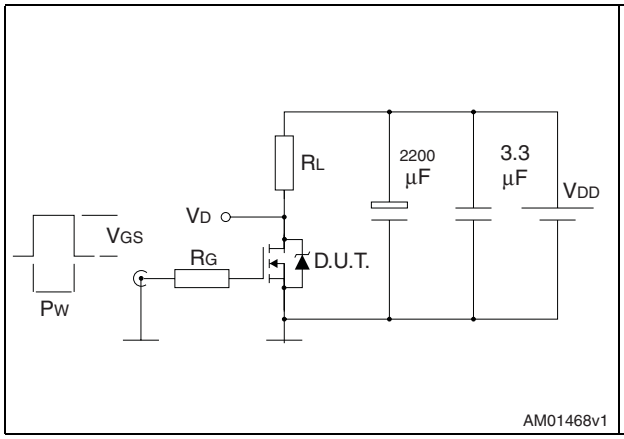


Figure 3. Gate charge test circuit

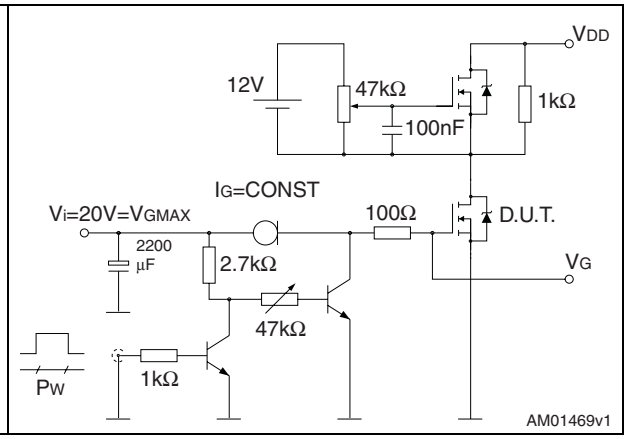


Figure 4. Test circuit for inductive load switching and diode recovery times

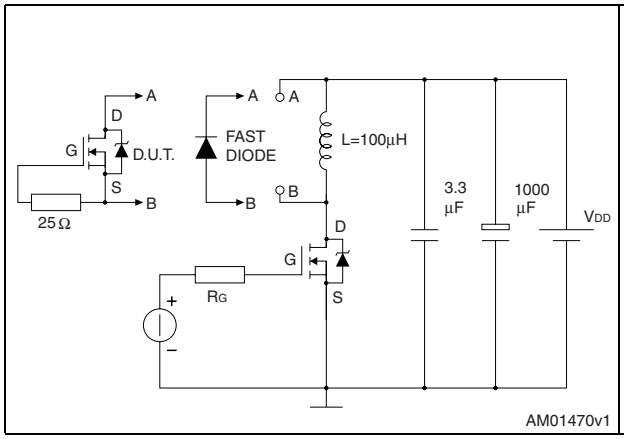


Figure 5. Unclamped inductive load test circuit

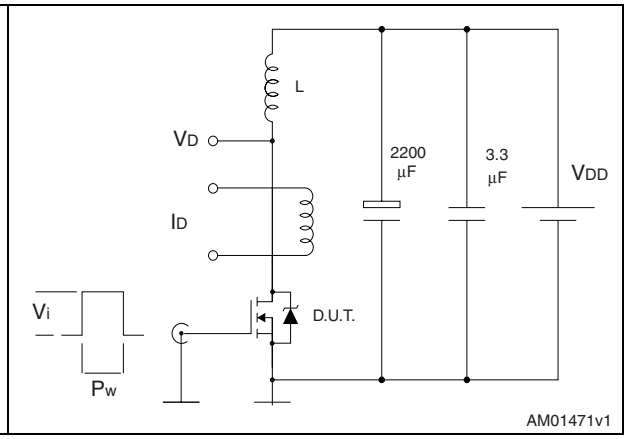


Figure 6. Unclamped inductive waveform

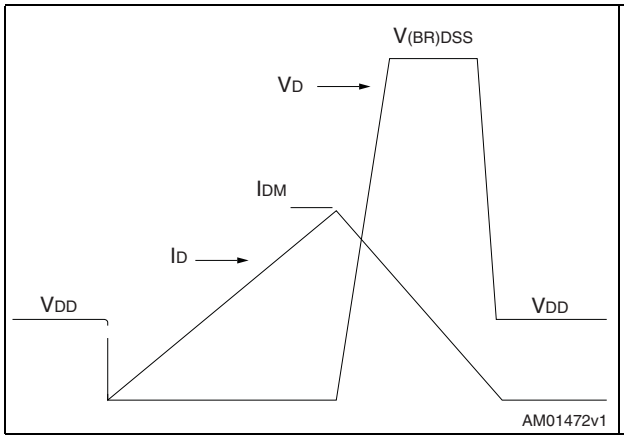
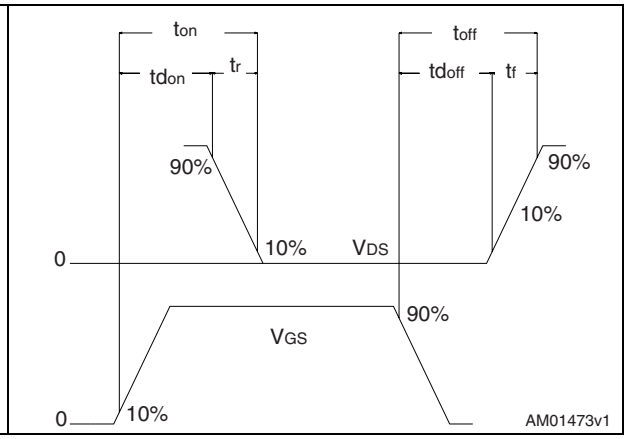


Figure 7. Switching time waveform



4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

Table 9. PowerFLAT™ 8x8 HV mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	0.80	0.90	1.00
A1		0.02	0.05
b	0.95	1.00	1.05
c		0.10	
D		8.00	
E		8.00	
D2	7.05	7.20	7.30
E2	4.15	4.30	4.40
e		2.00	
L	0.40	0.50	0.60

Figure 8. PowerFLAT™ 8x8 HV drawing mechanical data

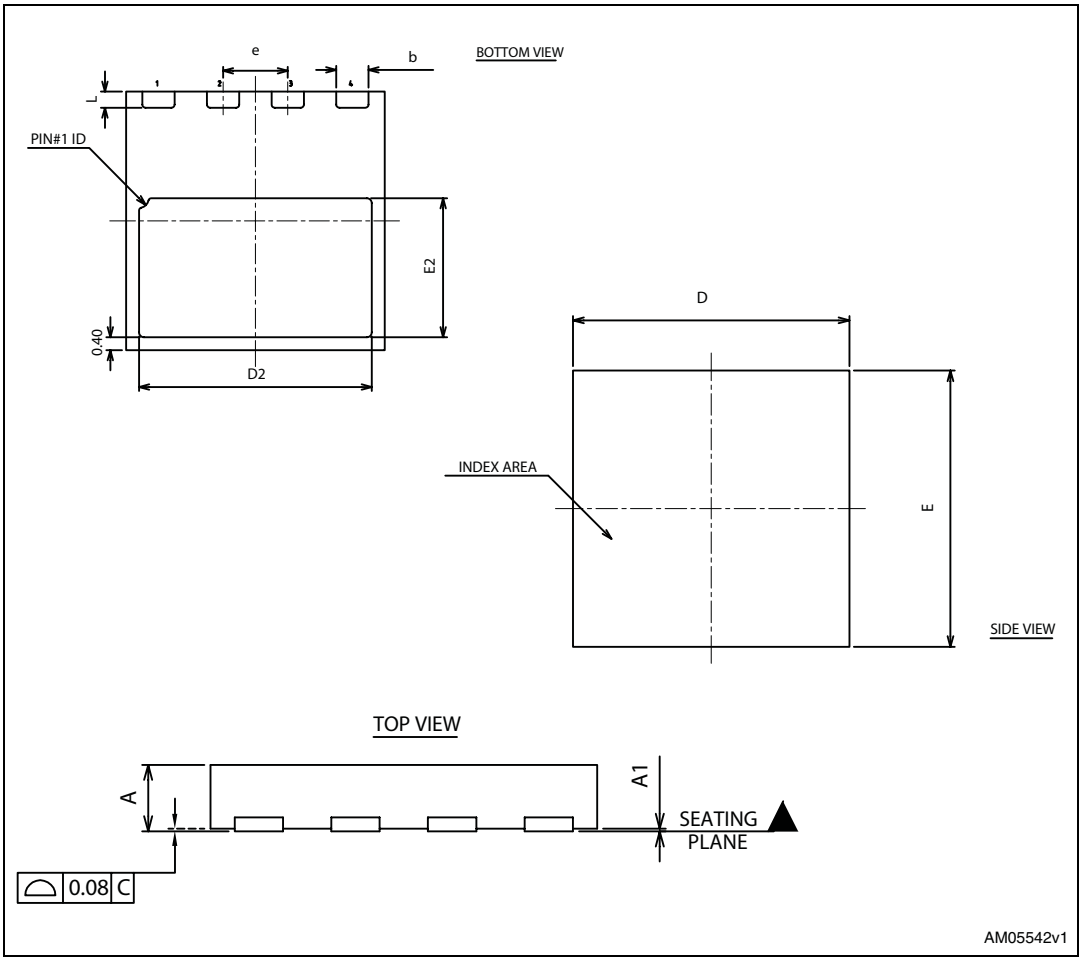
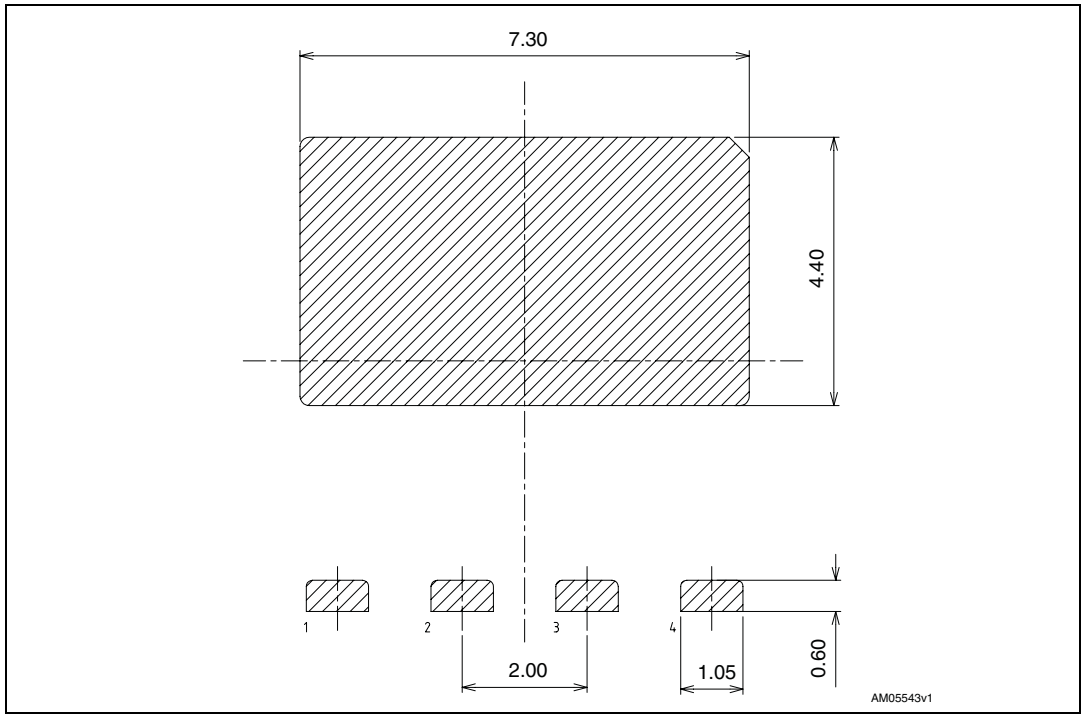


Figure 9. PowerFLAT™ 8x8 HV recommended footprint



5 Revision history

Table 10. Document revision history

Date	Revision	Changes
26-Apr-2010	1	First release.

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