



STL34NF06

N-CHANNEL 60V - 0.024Ω - 34A PowerFLAT™ LOW GATE CHARGE STripFET™II MOSFET

PRELIMINARY DATA

TYPE	V _{DSS}	R _{DS(on)}	I _D
STL34NF06	60 V	< 0.028Ω	34 A

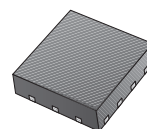
- TYPICAL R_{DS(on)} = 0.024Ω
- IMPROVED DIE-TO-FOOTPRINT RATIO
- VERY LOW PROFILE PACKAGE

DESCRIPTION

This Power MOSFET is the second generation of STMicroelectronics unique "STripFET™" technology. The resulting transistor shows extremely low on-resistance and minimal gate charge. The new PowerFLAT™ package allow a significant reduction in board space without compromising performance.

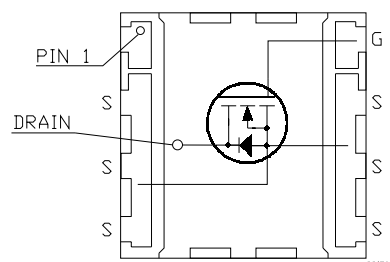
APPLICATIONS

- DC-DC CONVERTERS
- BATTERY MANAGEMENT IN NOMADIC EQUIPMENT



**PowerFLAT™ (5x5)
(Chip Scale Package)**

INTERNAL SCHEMATIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V _{DS}	Drain-source Voltage (V _{GS} = 0)	60	V
V _{DGR}	Drain-gate Voltage (R _{GS} = 20 kΩ)	60	V
V _{GS}	Gate- source Voltage	± 20	V
I _D	Drain Current (continuous) at T _C = 25°C (*)	34	A
	Drain Current (continuous) at T _C = 100°C	20	A
I _{DM} (•)	Drain Current (pulsed)	136	A
P _{TOT}	Total Dissipation at T _C = 25°C	70	W
	Derating Factor	0.56	W/°C
E _{AS} (1)	Single Pulse Avalanche Energy	250	mJ
T _{stg}	Storage Temperature	-55 to 150	°C
T _j	Max. Operating Junction Temperature		

(•) Pulse width limited by safe operating area

(1) Starting T_j = 25°C, I_D = 17A, V_{DD} = 42V

(*) Current Limited by Wire Bonding is 20A

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STL34NF06**THERMAL DATA**

Rthj-case	Thermal Resistance Junction-case Max	1.8	°C/W
Rthj-pcb (#)	Thermal Resistance Junction-ambient Max	31.2	°C/W

(*) When mounted on 1inch² FR4 Board, 2oz of Cu, t ≤ 10 sec.

ELECTRICAL CHARACTERISTICS (T_{CASE} = 25 °C UNLESS OTHERWISE SPECIFIED)
OFF

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V _{(BR)DSS}	Drain-source Breakdown Voltage	I _D = 250 μA, V _{GS} = 0	60			V
I _{DSS}	Zero Gate Voltage Drain Current (V _{GS} = 0)	V _{DS} = Max Rating V _{DS} = Max Rating, T _C = 125 °C			1 10	μA μA
I _{GSS}	Gate-body Leakage Current (V _{DS} = 0)	V _{GS} = ± 20V			±100	nA

ON (1)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V _{GS(th)}	Gate Threshold Voltage	V _{DS} = V _{GS} , I _D = 250μA	2			V
R _{DS(on)}	Static Drain-source On Resistance	V _{GS} = 10V, I _D = 17A		0.024	0.028	Ω

DYNAMIC

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
g _{fs} (1)	Forward Transconductance	V _{DS} = 30 V, I _D = 17 A		TBD		S
C _{iss}	Input Capacitance	V _{DS} = 25V, f = 1 MHz, V _{GS} = 0		920		pF
C _{oss}	Output Capacitance			225		pF
C _{rss}	Reverse Transfer Capacitance			80		pF

1. Pulsed: Pulse duration = 300 μs, duty cycle 1.5 %.

ELECTRICAL CHARACTERISTICS (CONTINUED)**SWITCHING ON**

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on Delay Time	$V_{DD} = 30V$, $I_D = 17 A$		11		ns
t_r	Rise Time	$R_G = 4.7\Omega$, $V_{GS} = 10V$ (see test circuit, Figure 3)		50		ns
Q_g	Total Gate Charge	$V_{DD} = 48V$, $I_D = 34 A$, $V_{GS} = 10V$		32	43	nC
Q_{gs}	Gate-Source Charge			6.5		nC
Q_{gd}	Gate-Drain Charge			14.4		nC

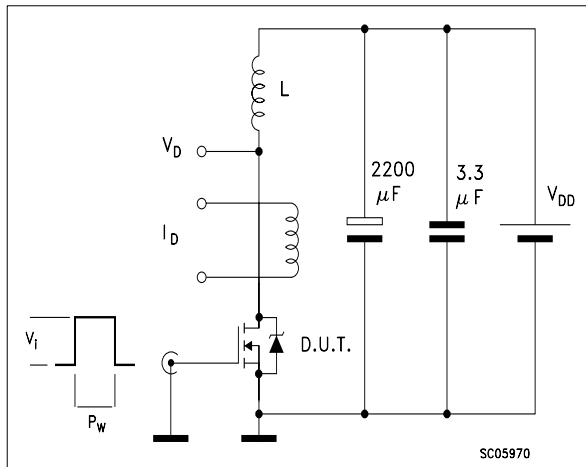
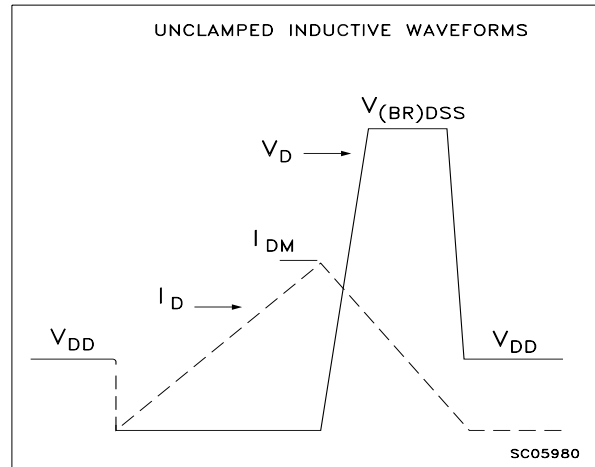
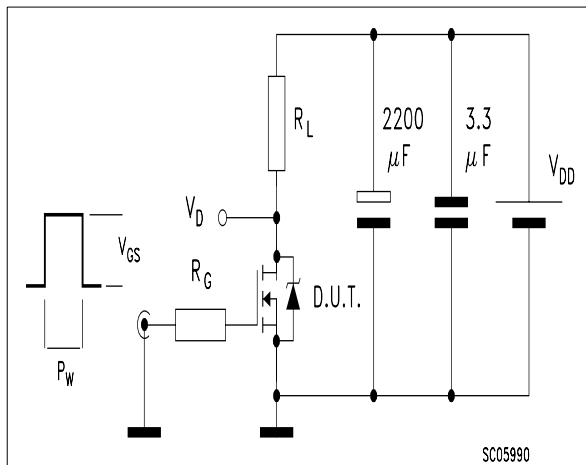
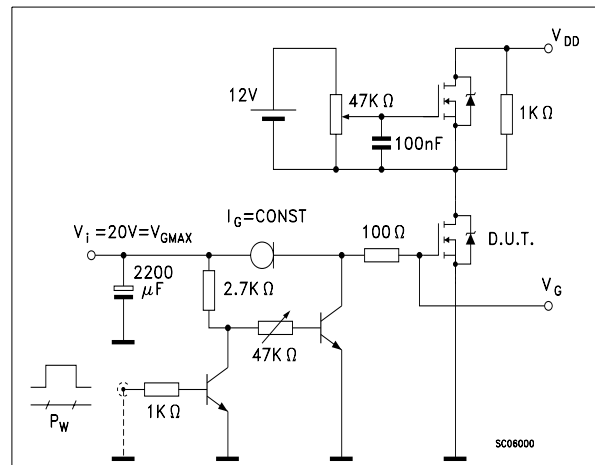
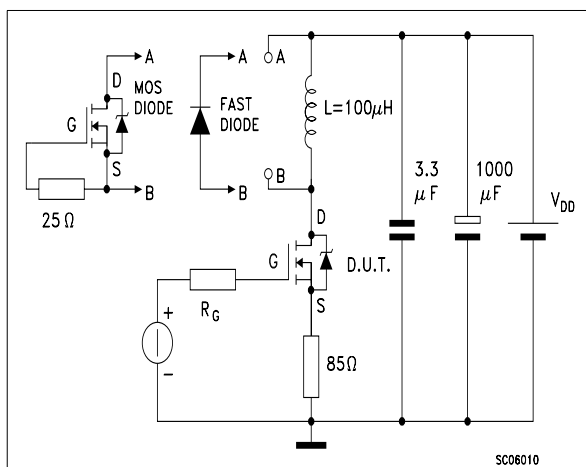
SWITCHING OFF

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{d(off)}$	Turn-Off-Delay Time	$V_{DD} = 30V$, $I_D = 17A$, $R_G = 4.7\Omega$, $V_{GS} = 10V$		27		ns
t_f	Fall Time	(see test circuit, Figure 3)		11		ns

SOURCE DRAIN DIODE

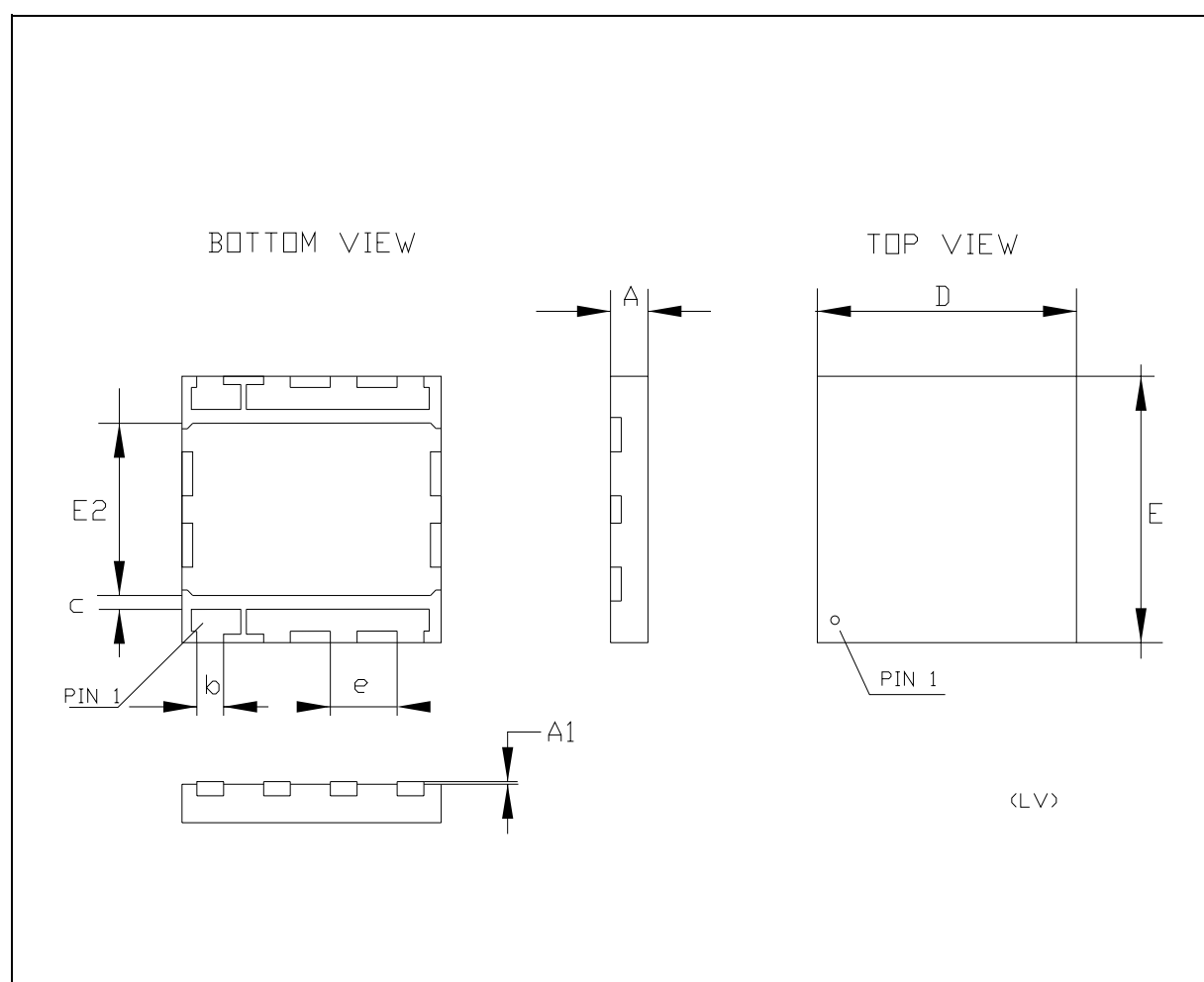
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$I_{SD} (3)$	Source-drain Current				34	A
$I_{SDM} (2)$	Source-drain Current (pulsed)				136	A
$V_{SD} (1)$	Forward On Voltage	$I_{SD} = 34 A$, $V_{GS} = 0$			1.2	V
t_{rr}	Reverse Recovery Time	$I_{SD} = 34 A$, $di/dt = 100A/\mu s$, $V_{DD} = 10V$, $T_j = 150^\circ C$ (see test circuit, Figure 5)		63		ns
Q_{rr}	Reverse Recovery Charge			151		nC
I_{RRM}	Reverse Recovery Current			4.8		A

Note: 1. Pulsed: Pulse duration = 300 μs , duty cycle 1.5 %.
 2. Pulse width limited by safe operating area.
 3. Current Limited by Wire Bonding is 20A

STL34NF06**Fig. 1: Unclamped Inductive Load Test Circuit****Fig. 2: Unclamped Inductive Waveform****Fig. 3: Switching Times Test Circuit For Resistive Load****Fig. 4: Gate Charge test Circuit****Fig. 5: Test Circuit For Inductive Load Switching And Diode Recovery Times**

PowerFLAT™(5x5) MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A		0.90	1.00		0.035	0.039
A1		0.02	0.05		0.001	0.002
b	0.43	0.51	0.58	0.017	0.020	0.023
c	0.33	0.41	0.48	0.013	0.016	0.019
D		5.00			0.197	
E		5.00			0.197	
E2	3.10	3.18	3.25	0.122	0.125	0.128
e		1.27			0.050	



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