



STL35N15F3

N-channel 150 V, 0.0355 Ω , 7 A STripFET™ III Power MOSFET
in PowerFLAT™ 5x6 package

Datasheet — production data

Features

Order code	V _{DSS}	R _{DS(on)} max	I _D
STL35N15F3	150 V	< 0.04 Ω	7 A ⁽¹⁾

1. The value is rated according R_{thj-pcb}

- Improved die-to-footprint ratio
- Very low profile package (1mm max)
- Very low thermal resistance
- Low on-resistance

Application

- Switching application

Description

This device is an N-channel enhancement mode Power MOSFET produced using STMicroelectronics' STripFET™ III technology, which is specifically designed to minimize on-resistance and gate charge to provide superior switching performance.



Figure 1. Internal schematic diagram

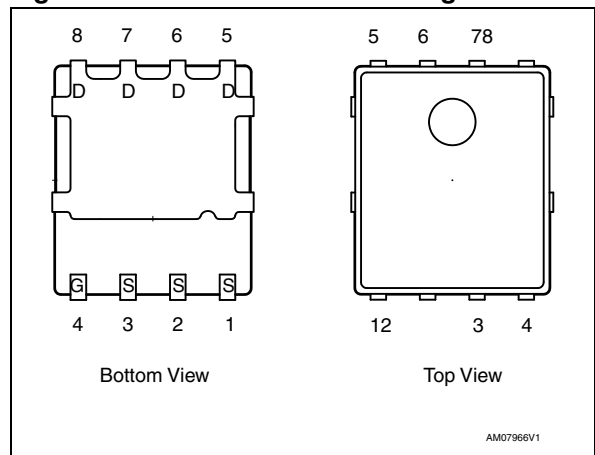


Table 1. Device summary

Order code	Marking	Package	Packaging
STL35N15F3	L35N15F3	PowerFLAT™ 5x6	Tape and reel

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1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage	150	V
V_{GS}	Gate-source voltage	± 20	V
$I_D^{(1)}$	Drain current (continuous) at $T_C = 25\text{ }^\circ\text{C}$	33	A
$I_D^{(2)}$	Drain current (continuous) at $T_{pcb} = 25\text{ }^\circ\text{C}$	7	A
$I_D^{(2)}$	Drain current (continuous) at $T_{pcb} = 100\text{ }^\circ\text{C}$	4.3	A
$I_{DM}^{(3),(2)}$	Drain current (pulsed)	28	A
$P_{TOT}^{(1)}$	Total dissipation at $T_C = 25\text{ }^\circ\text{C}$	80	W
$P_{TOT}^{(2)}$	Total dissipation at $T_{pcb} = 25\text{ }^\circ\text{C}$	4	W
T_J T_{stg}	Operating junction temperature Storage temperature	-55 to 150	$^\circ\text{C}$

1. The value is rated according to R_{thj-c}
2. The value is rated according to $R_{thj-pcb}$
3. Pulse width limited by safe operating area

Table 3. Thermal resistance

Symbol	Parameter	Value	Unit
$R_{thj-case}$	Thermal resistance junction-case	1.56	$^\circ\text{C/W}$
$R_{thj-pcb}^{(1)}$	Thermal resistance junction-pcb	31.3	$^\circ\text{C/W}$

1. When mounted on FR-4 board of 1inch², 2oz Cu, $t < 10\text{ sec}$

2 Electrical characteristics

($T_{CASE} = 25\text{ }^{\circ}\text{C}$ unless otherwise specified)

Table 4. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$I_D = 1\text{ mA}$, $V_{GS} = 0$	150			V
I_{DSS}	Zero gate voltage drain current ($V_{GS} = 0$)	$V_{DS} = 150\text{ V}$ $V_{DS} = 150\text{ V}$, $T_C = 125\text{ }^{\circ}\text{C}$			1 10	μA μA
I_{GSS}	Gate body leakage current ($V_{DS} = 0$)	$V_{GS} = \pm 20\text{ V}$			± 100	nA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}$, $I_D = 250\text{ }\mu\text{A}$	2		4	V
$R_{DS(on)}$	Static drain-source on-resistance	$V_{GS} = 10\text{ V}$, $I_D = 3.5\text{ A}$		0.0355	0.04	Ω

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	$V_{DS} = 25\text{ V}$, $f = 1\text{ MHz}$, $V_{GS} = 0$	-	1905	-	pF
C_{oss}	Output capacitance			171		pF
C_{rss}	Reverse transfer capacitance			28		pF
Q_g	Total gate charge	$V_{DD} = 15\text{ V}$, $I_D = 6\text{ A}$	-	49.4	-	nC
Q_{gs}	Gate-source charge	$V_{GS} = 10\text{ V}$		7.3		nC
Q_{gd}	Gate-drain charge	Figure 14		22.6		nC
R_G	Gate input resistance	$f = 1\text{ MHz}$ Gate DC Bias = 0 Test signal level = 20 mV open drain	-1	.7	-	Ω

Table 6. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 75\text{ V}$, $I_D = 3.5\text{ A}$, $R_G = 4.7\text{ }\Omega$, $V_{GS} = 10\text{ V}$ Figure 13	-	14	-	ns
t_r	Rise time			11		ns
$t_{d(off)}$	Turn-off delay time			57		ns
t_f	Fall time			20		ns

Table 7. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		7	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)		-		28	A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD}=6\text{ A}$, $V_{GS}=0$	-		1.3	V
t_{rr}	Reverse recovery time	$I_{SD}=6\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$, $V_{DD}=120\text{ V}$, $T_j=150\text{ }^\circ\text{C}$	-	124		ns
Q_{rr}	Reverse recovery charge			670		nC
I_{RRM}	Reverse recovery current			11		A

1. Pulse width limited by safe operating area

2. Pulsed: pulse duration=300 μs , duty cycle 1.5%

2.1 Electrical characteristics

Figure 2. Safe operating area

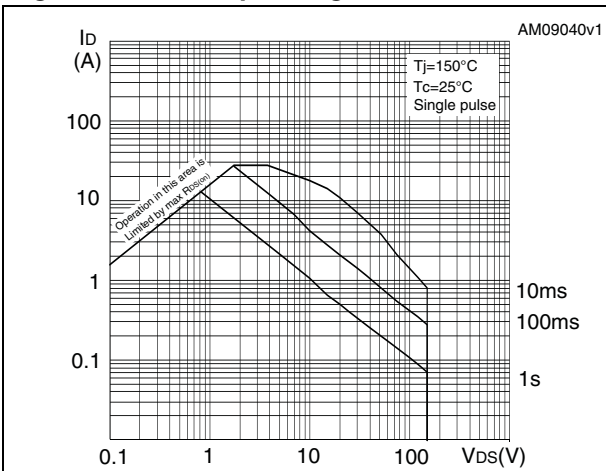


Figure 3. Thermal impedance

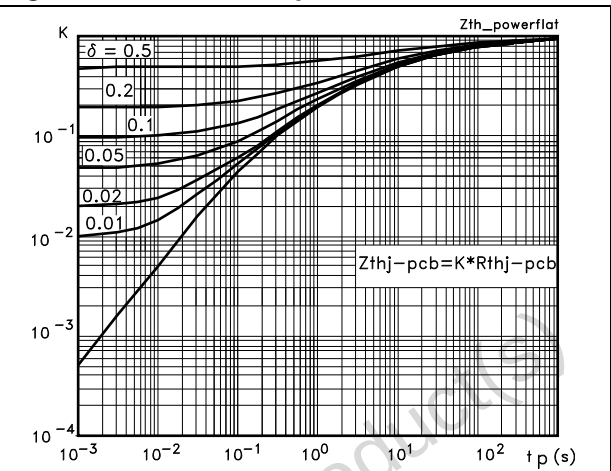


Figure 4. Output characteristics

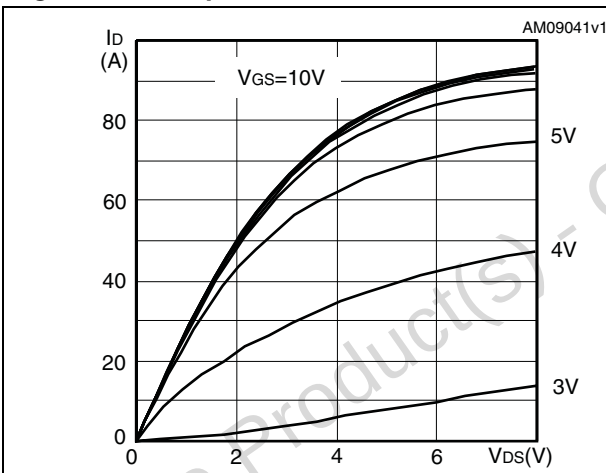


Figure 5. Transfer characteristics

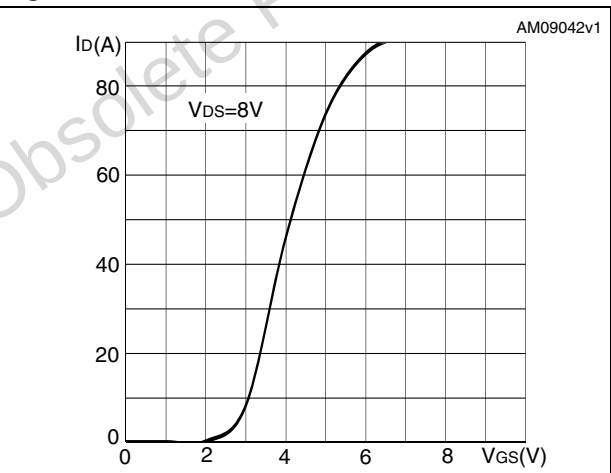


Figure 6. Normalized $B_{V_{DSS}}$ vs temperature

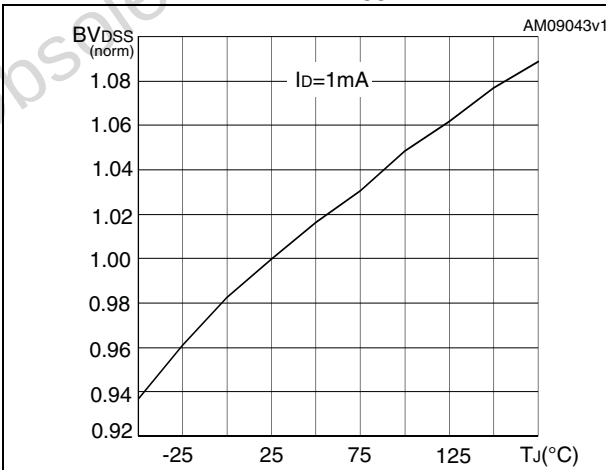


Figure 7. Static drain-source on-resistance

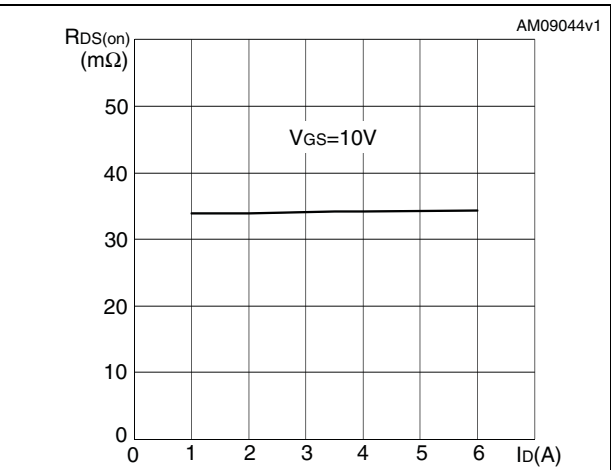


Figure 8. Gate charge vs gate-source voltage Figure 9. Capacitance variations

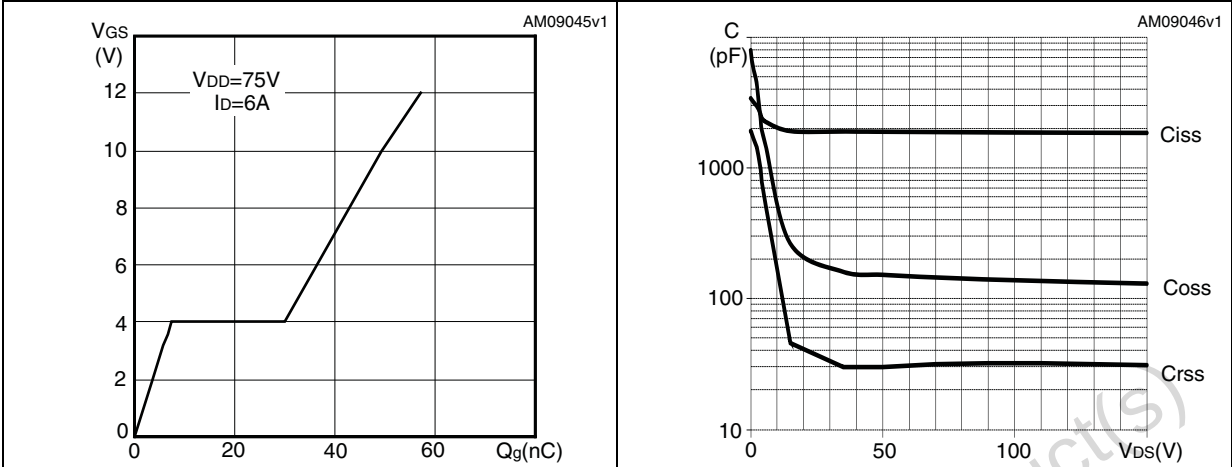


Figure 10. Normalized gate threshold voltage vs temperature Figure 11. Normalized on-resistance vs temperature

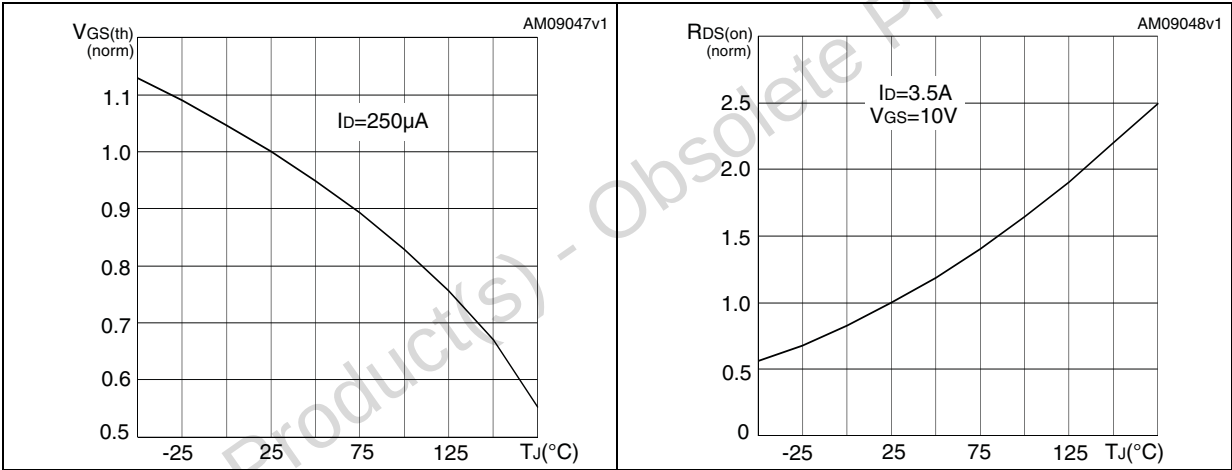
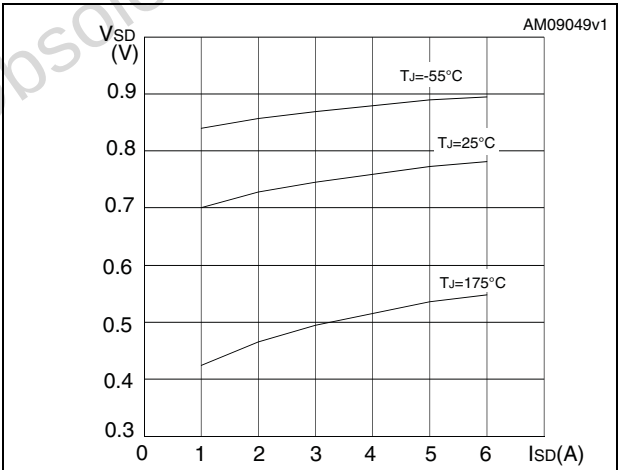
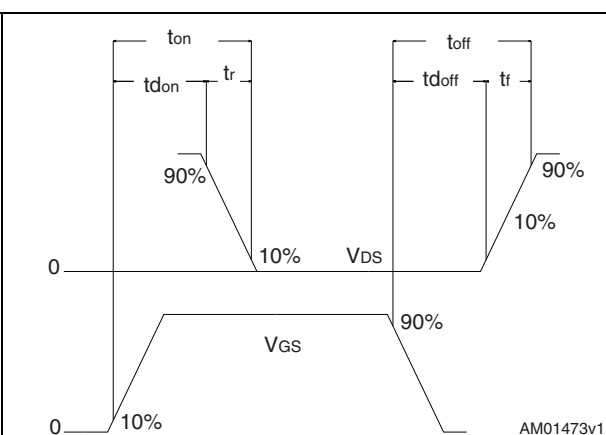
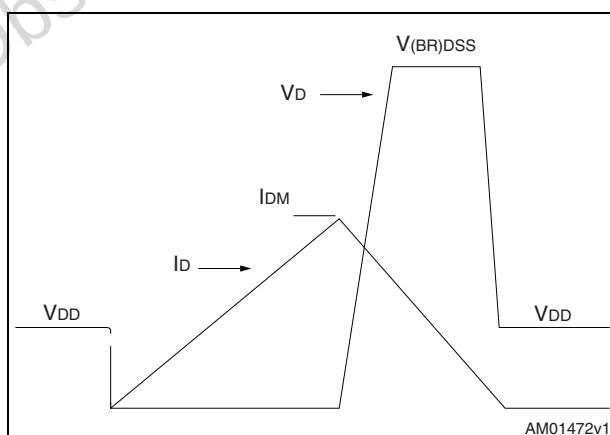
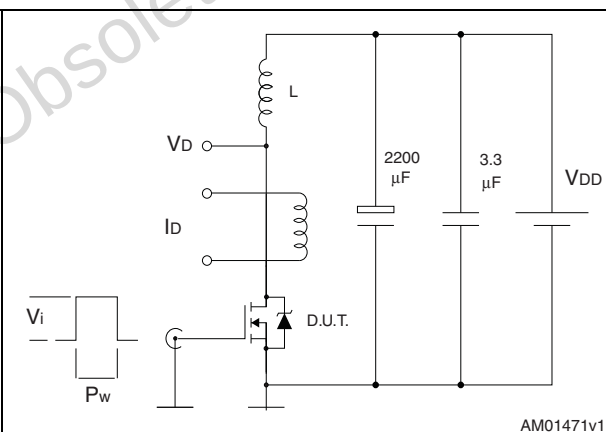
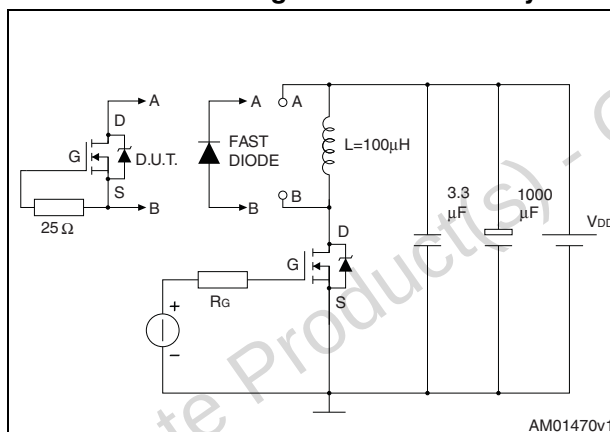
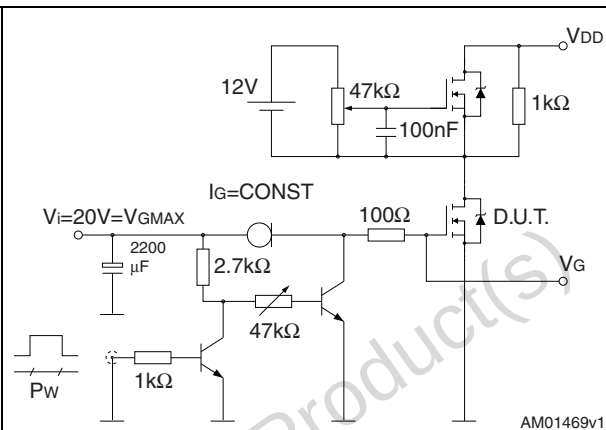
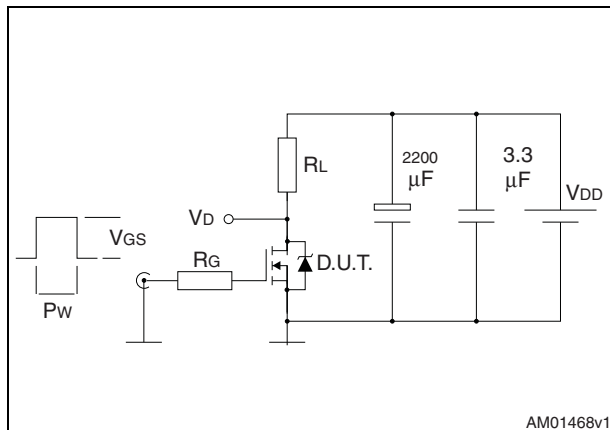


Figure 12. Source-drain diode forward characteristics





4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

Table 8. PowerFLAT™ 5x6 type C-B mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	0.800	.830	.93
A1	0	0.02	0.05
A3		0.20	
b	0.350	.400	.47
D5		.00	
D1		4.75	
D2	4.15	4.20	4.25
E6		.00	
E1		5.75	
E2	3.43	3.48	3.53
E4	2.58	2.63	2.68
e1		.27	
L	0.700	.800	.90

Bottom View

Dimensions: L , e , $e/2$, 1 , $D/2$, D , $b \times 8$, $E2$, $E4$.

Callouts: PIN 1 IDENTIFICATION, EXPOSED PAD.

Top View

Dimensions: $D/2$, $E/2$, $E1$, E , $D1$, D .

Callouts: PIN 1 IDENTIFICATION, 1.

Side View

Dimensions: A , $A1$, $A3$.

Callouts: SEATING PLANE, C.

Feature Callouts:

- Surface texture: $\sqrt{\text{ }}$ 0.1 C
- Radius: R 0.08 C

Table 9. PowerFLAT™ 5x6 type S-C mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A0	.80		1.00
A1	0.02		0.05
A2		0.25	
b0	.30		0.50
D5		.20	
E6		.15	
D2	4.11		4.31
E2	3.50		3.70
e1		.27	
e1		0.65	
L	0.715		1.015
K1	.05		1.35

Figure 20. PowerFLAT™ 5x6 type S-C mechanical data

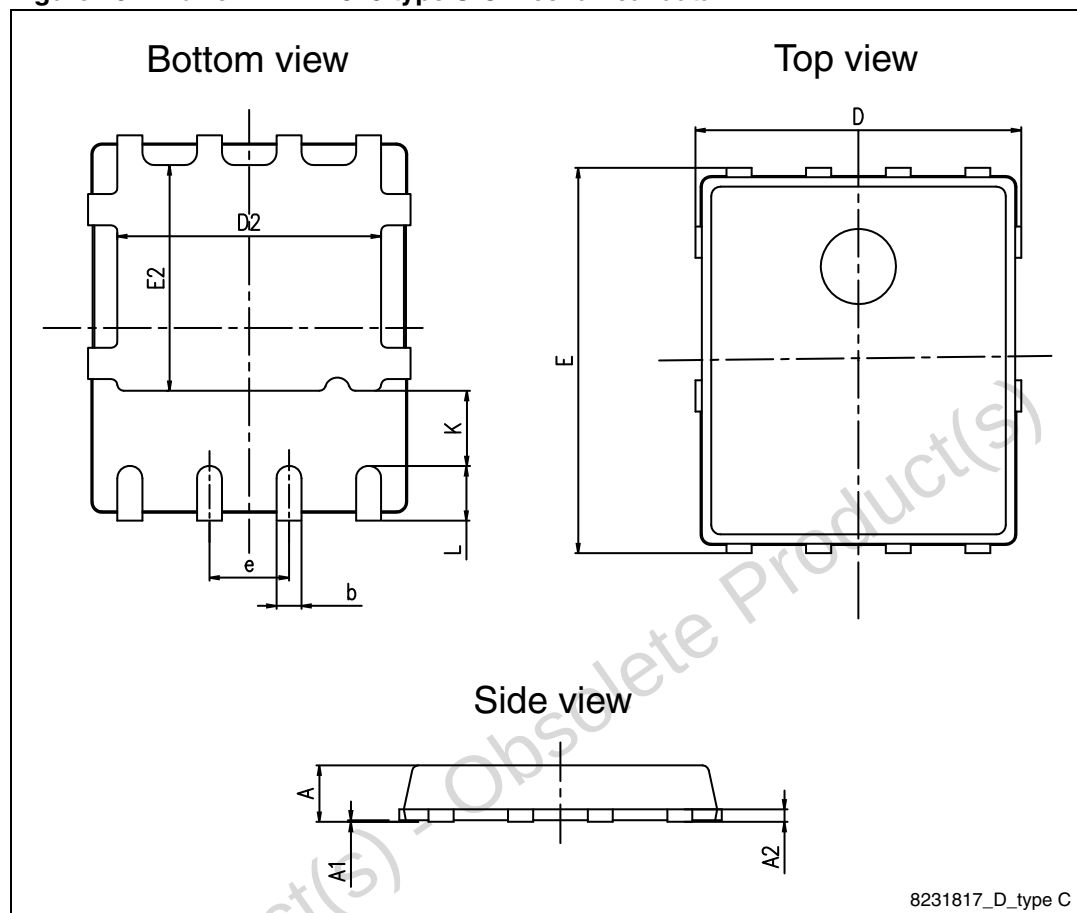
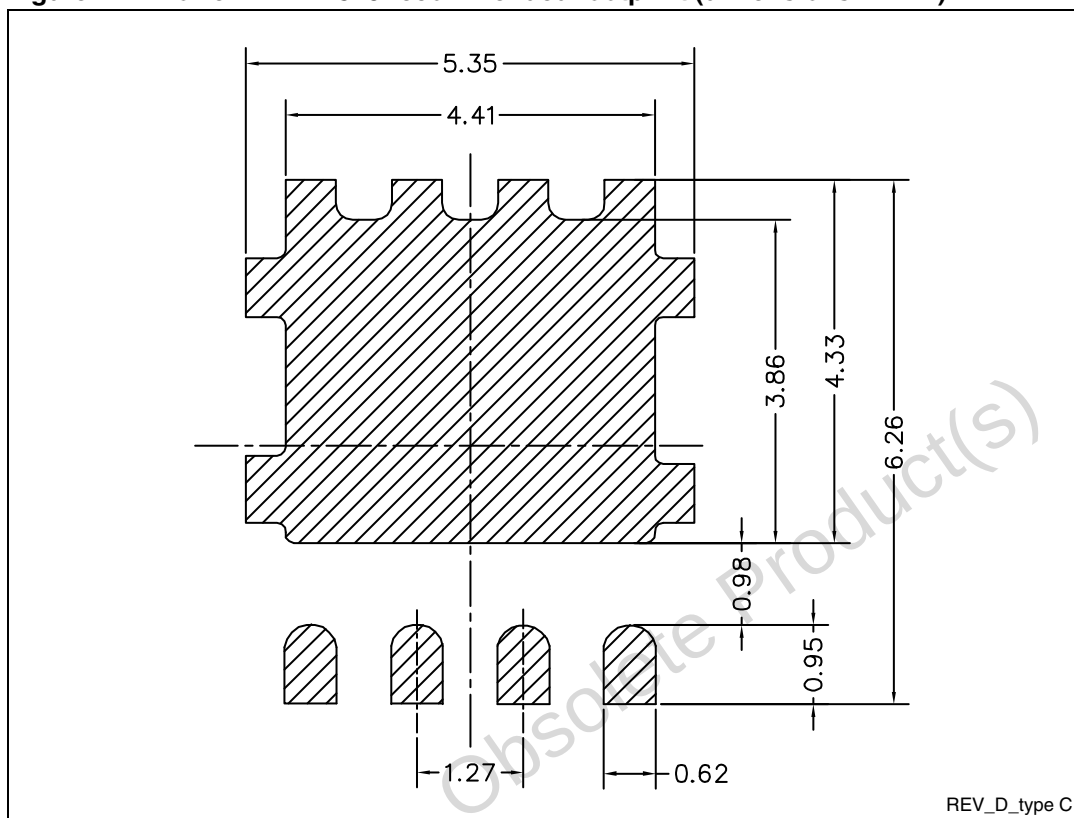


Figure 21. PowerFLAT™ 5x6 recommended footprint (dimensions in mm)



5 P ackaging mechanical data

Figure 22. PowerFLAT™ 5x6 tape

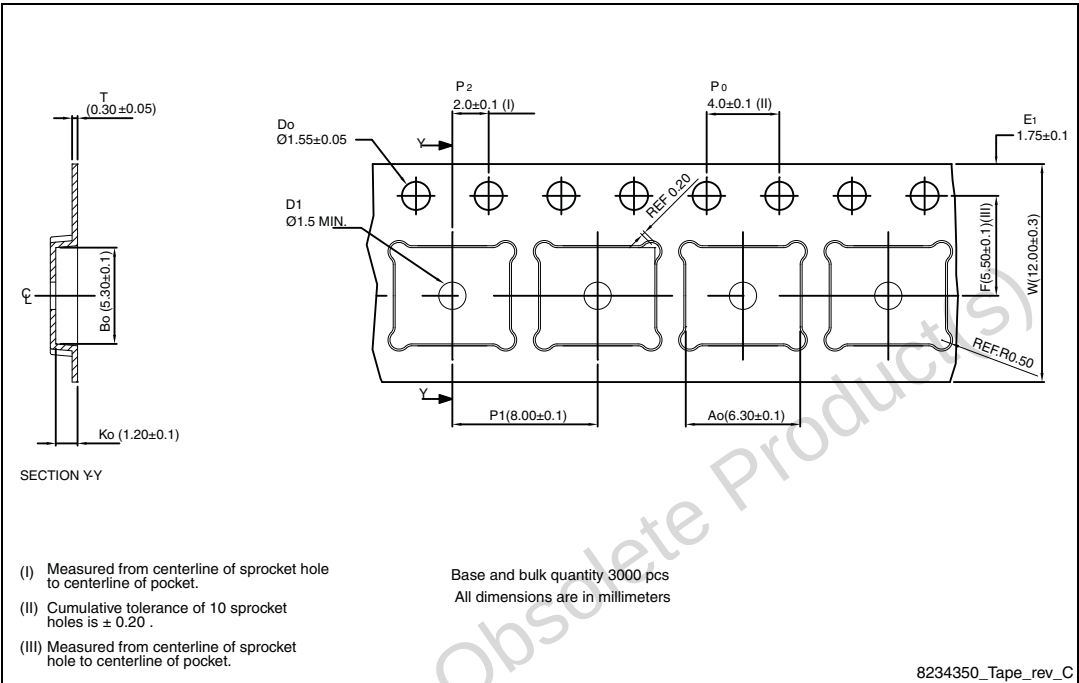


Figure 23. PowerFLAT™ 5x6 package orientation in carrier tape.

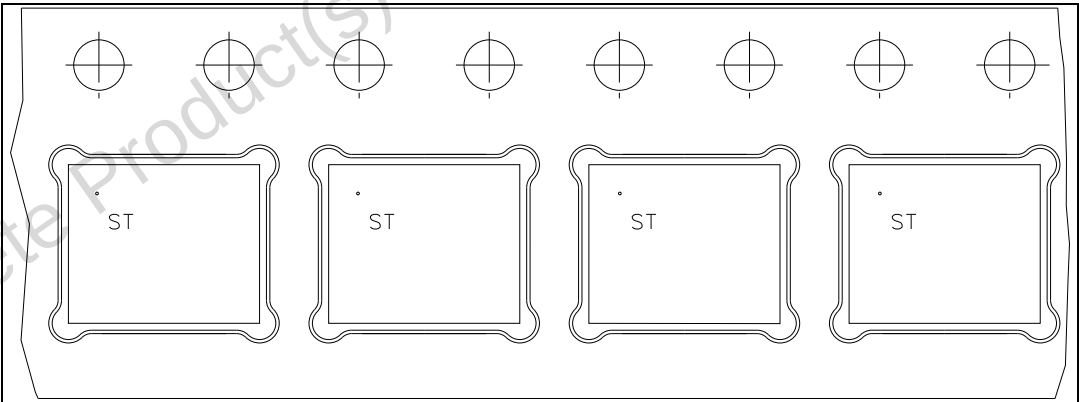
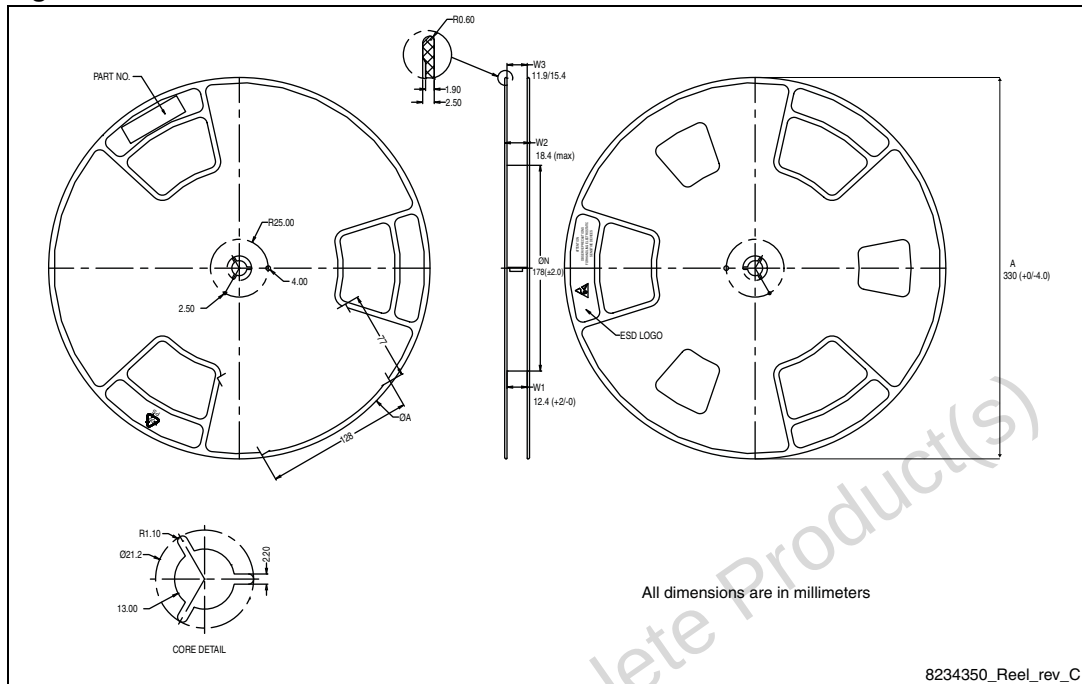


Figure 24. PowerFLAT™ 5x6 reel



6 Revision history

Table 10. Document revision history

Date	Revision	Changes
16-Mar-2011	1	Initial release.
10-May-2012	2	<i>Section 4: Package mechanical data</i> has been added. Minor text changes.

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