



STL6NK55Z

N-CHANNEL 550V - 1.2Ω - 5.2A PowerFLAT™
Zener-Protected SuperMESH™ Power MOSFET

TYPE	V _{DSS}	R _{DS(on)}	I _D (1)	P _w (1)
STL6NK55Z	550 V	< 1.4 Ω	5.2 A	75 W

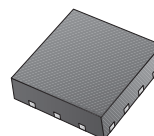
- TYPICAL R_{DS(on)} = 1.2 Ω
- EXTREMELY HIGH dv/dt CAPABILITY
- IMPROVED ESD CAPABILITY
- 100% AVALANCHE RATED
- GATE CHARGE MINIMIZED
- VERY LOW INTRINSIC CAPACITANCES
- VERY GOOD MANUFACTURING REPEATABILITY

DESCRIPTION

The SuperMESH™ series is obtained through an extreme optimization of ST's well established strip-based PowerMESH™ layout. In addition to pushing on-resistance significantly down, special care is taken to ensure a very good dv/dt capability for the most demanding applications. Such series complements ST full range of high voltage MOSFETs including revolutionary MDmesh™ products.

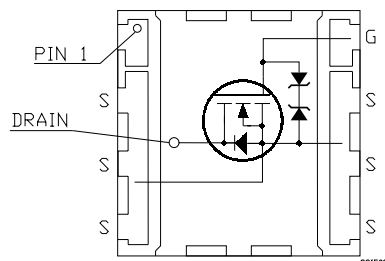
APPLICATIONS

- LIGHTING
- IDEAL FOR OFF-LINE POWER SUPPLIES, ADAPTORS AND PFC



**PowerFLAT™ (5x5)
(Chip Scale Package)**

INTERNAL SCHEMATIC DIAGRAM



ORDERING INFORMATION

SALES TYPE	MARKING	PACKAGE	PACKAGING
STL6NK55Z	L6NK55Z	PowerFLAT™ (5x5)	TAPE & REEL

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source Voltage ($V_{GS} = 0$)	550	V
V_{DGR}	Drain-gate Voltage ($R_{GS} = 20\text{ k}\Omega$)	550	V
V_{GS}	Gate- source Voltage	± 30	V
I_D (2)	Drain Current (continuous) at $T_C = 25^\circ\text{C}$ (Steady State) Drain Current (continuous) at $T_C = 100^\circ\text{C}$	0.86 0.54	A A
I_{DM} (2)	Drain Current (pulsed)	3.44	A
P_{TOT} (2)	Total Dissipation at $T_C = 25^\circ\text{C}$ (Steady State)	2.5	W
P_{TOT} (1)	Total Dissipation at $T_C = 25^\circ\text{C}$ (Steady State)	75	W
	Derating Factor (2)	0.02	W/ $^\circ\text{C}$
$V_{ESD}(G-S)$	Gate source ESD(HBM-C=100pF, R=1.5K Ω)	3000	V/ns
dv/dt (4)	Peak Diode Recovery voltage slope	4.5	V/ns
T_{stg}	Storage Temperature	-55 to 150	$^\circ\text{C}$
T_j	Max. Operating Junction Temperature		

THERMAL DATA

Symbol	Parameter	Max.	Unit
R_{thj-F}	Thermal Resistance Junction-Foot (Drain)	1.67	$^\circ\text{C}/\text{W}$
$R_{thj-amb}$ (2)	Thermal Resistance Junction-ambient	50	$^\circ\text{C}/\text{W}$

Note: 1. The value is rated according to R_{thj-F} .
 2. When Mounted on FR-4 Board of 1inch², 2 oz Cu
 3. Pulse width limited by safe operating area
 4. $I_{SD} < 5.7\text{A}$, $di/dt < 300\text{A}/\mu\text{s}$, $V_{DD} < V_{(BR)DSS}$, $T_j < T_{JMAX}$

AVALANCHE CHARACTERISTICS

Symbol	Parameter	Max Value	Unit
I_{AR}	Avalanche Current, Repetitive or Not-Repetitive (pulse width limited by T_j max)	5.2	A
E_{AS}	Single Pulse Avalanche Energy (starting $T_j = 25^\circ\text{C}$, $I_D = I_{AR}$, $V_{DD} = 50\text{ V}$)	160	mJ

GATE-SOURCE ZENER DIODE

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
BV_{GSO}	Gate-Source Breakdown Voltage	$I_{GS} = \pm 1\text{mA}$ (Open Drain)	30			V

PROTECTION FEATURES OF GATE-TO-SOURCE ZENER DIODES

The built-in back-to-back Zener diodes have specifically been designed to enhance not only the device's ESD capability, but also to make them safely absorb possible voltage transients that may occasionally be applied from gate to source. In this respect the Zener voltage is appropriate to achieve an efficient and cost-effective intervention to protect the device's integrity. These integrated Zener diodes thus avoid the usage of external components.

ELECTRICAL CHARACTERISTICS (TCASE = 25°C UNLESS OTHERWISE SPECIFIED)
 ON/OFF

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source Breakdown Voltage	$I_D = 1 \text{ mA}$, $V_{GS} = 0$	550			V
I_{DSS}	Zero Gate Voltage Drain Current ($V_{GS} = 0$)	$V_{DS} = \text{Max Rating}$ $V_{DS} = \text{Max Rating}$, $T_C = 125^\circ\text{C}$			1 50	μA μA
I_{GSS}	Gate-body Leakage Current ($V_{DS} = 0$)	$V_{GS} = \pm 20\text{V}$			± 10	μA
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}$, $I_D = 50\mu\text{A}$	3	3.75	4.5	V
$R_{DS(on)}$	Static Drain-source On Resistance	$V_{GS} = 10\text{V}$, $I_D = 2.6 \text{ A}$		1.2	1.4	Ω

DYNAMIC

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$g_{fs} (1)$	Forward Transconductance	$V_{DS} = 10 \text{ V}$, $I_D = 2.6 \text{ A}$		3.5		S
C_{iss} C_{oss} C_{rss}	Input Capacitance Output Capacitance Reverse Transfer Capacitance	$V_{DS} = 25\text{V}$, $f = 1 \text{ MHz}$, $V_{GS} = 0$		695 88 20		pF pF pF
$C_{oss \text{ eq.}} (3)$	Equivalent Output Capacitance	$V_{GS} = 0\text{V}$, $V_{DS} = 0\text{V to } 440 \text{ V}$		48		pF
R_G	Gate Input Resistance	$f = 1 \text{ MHz}$ Gate DC Bias = 0 Test Signal Level = 20mV Open Drain		3		Ω

SWITCHING

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$ t_r $t_{d(off)}$ t_f	Turn-on Delay Time Rise time Turn-off Delay Time Fall Time	$V_{DD} = 275 \text{ V}$, $I_D = 2.6 \text{ A}$ $R_G = 4.7\Omega$ $V_{GS} = 10 \text{ V}$ (Resistive Load see, Figure 3)		14 20 31.5 18		ns ns ns ns
Q_g Q_{gs} Q_{gd}	Total Gate Charge Gate-Source Charge Gate-Drain Charge	$V_{DD} = 440\text{V}$, $I_D = 5.2 \text{ A}$, $V_{GS} = 10\text{V}$		25 4.5 14	35	nC nC nC

SOURCE DRAIN DIODE

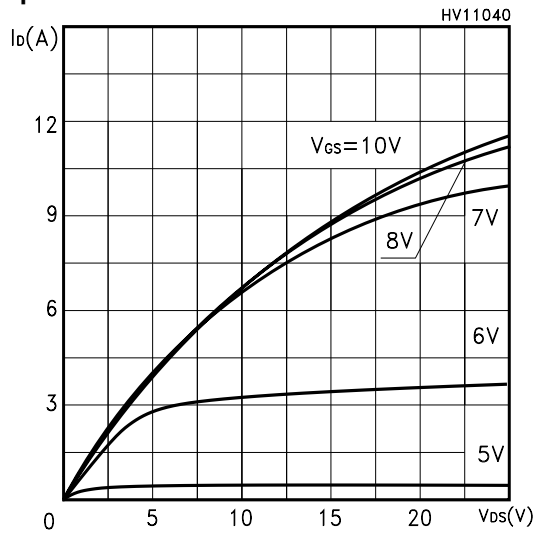
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_{SD} $I_{SDM} (2)$	Source-drain Current Source-drain Current (pulsed)				0.86 3.44	A A
$V_{SD} (1)$	Forward On Voltage	$I_{SD} = 5.2 \text{ A}$, $V_{GS} = 0$			1.6	V
t_{rr} Q_{rr} I_{RRM}	Reverse Recovery Time Reverse Recovery Charge Reverse Recovery Current	$I_{SD} = 5.2 \text{ A}$, $di/dt = 100\text{A}/\mu\text{s}$ $V_{DD} = 40\text{V}$, $T_j = 150^\circ\text{C}$ (see test circuit, Figure 5)		350 2.2 12.5		ns μC A

 Note: 1. Pulsed: Pulse duration = 300 μs , duty cycle 1.5 %.

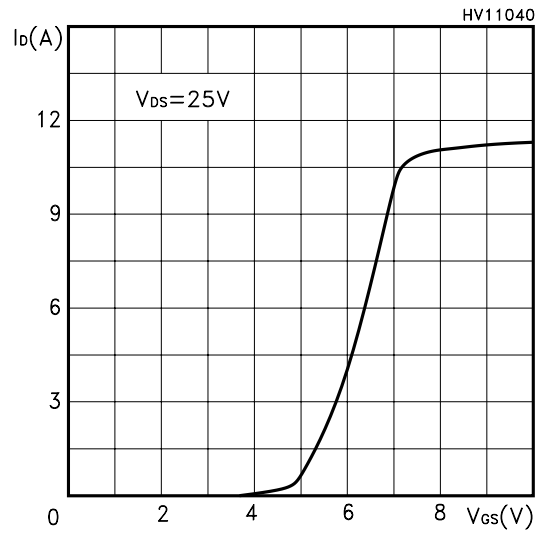
2. Pulse width limited by safe operating area.

 3. $C_{oss \text{ eq.}}$ is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS} .

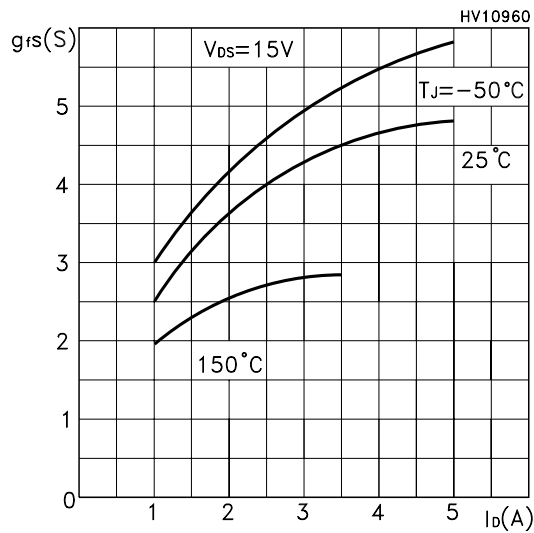
Output Characteristics



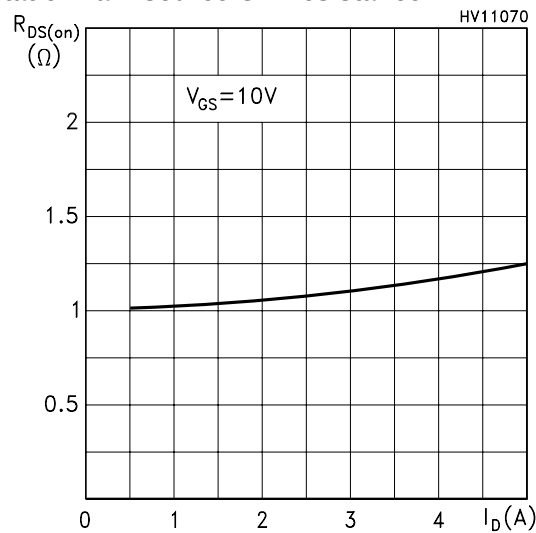
Transfer Characteristics



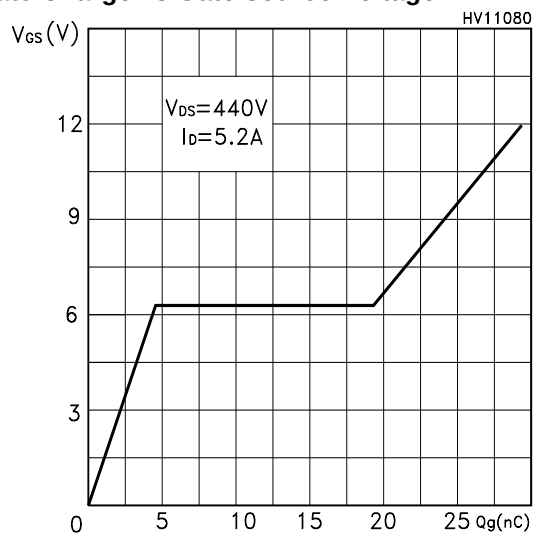
Transconductance



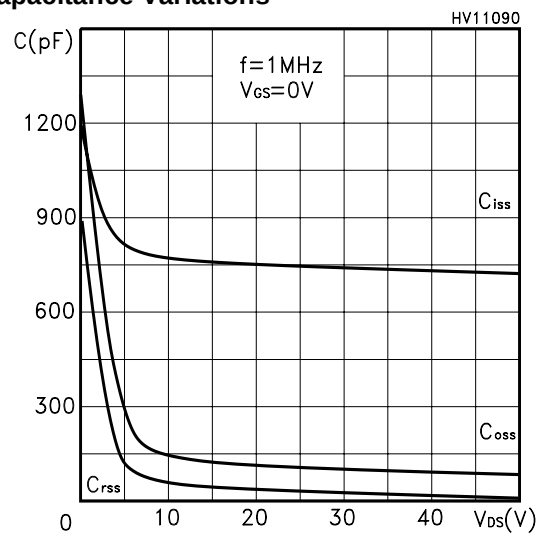
Static Drain-source On Resistance



Gate Charge vs Gate-source Voltage



Capacitance Variations



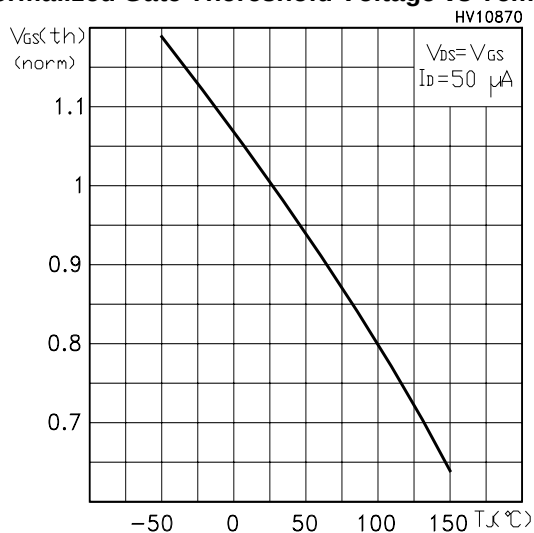
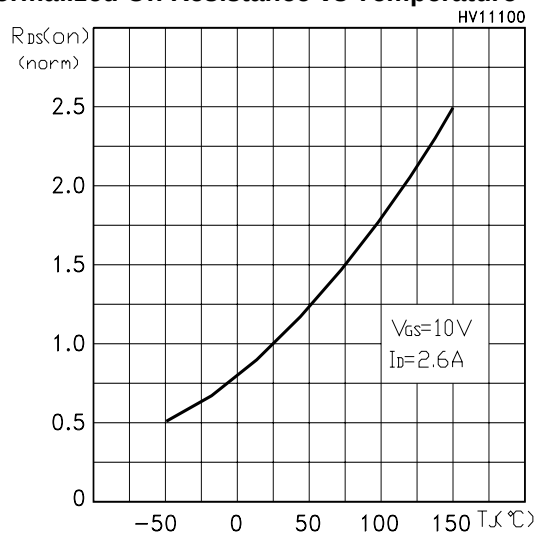
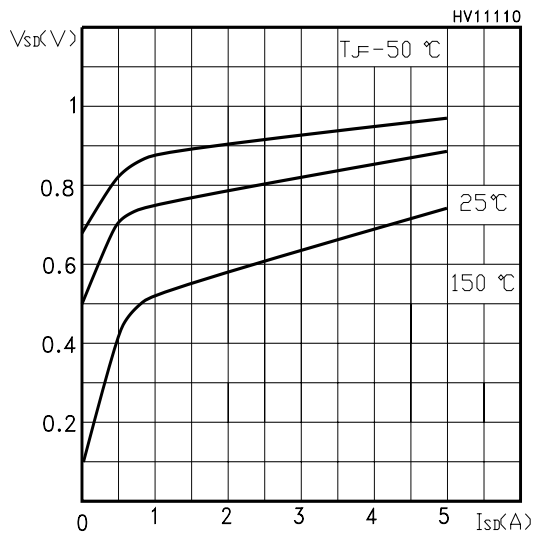
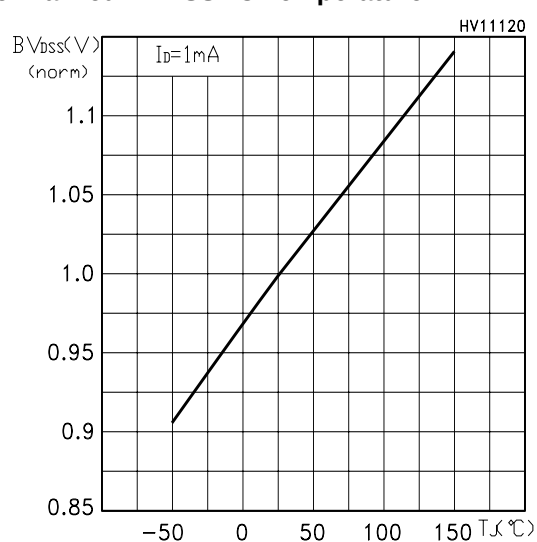
Normalized Gate Threshold Voltage vs Temp.**Normalized On Resistance vs Temperature****Source-drain Diode Forward Characteristics****Normalized BVDSS vs Temperature**

Fig. 1: Unclamped Inductive Load Test Circuit

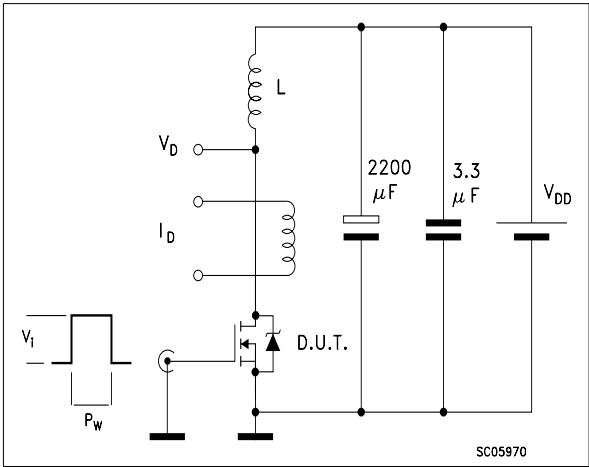


Fig. 2: Unclamped Inductive Waveform

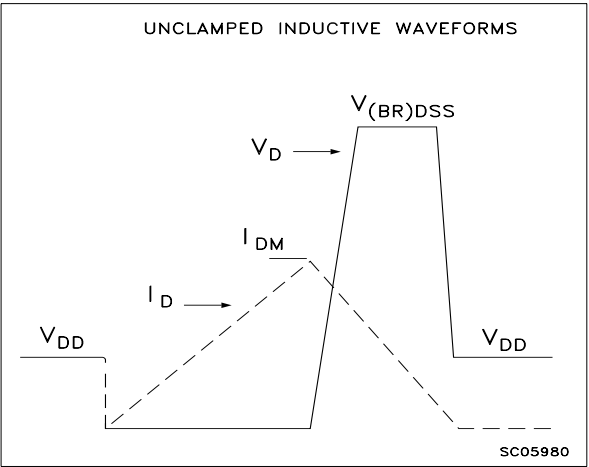


Fig. 3: Switching Times Test Circuit For Resistive Load

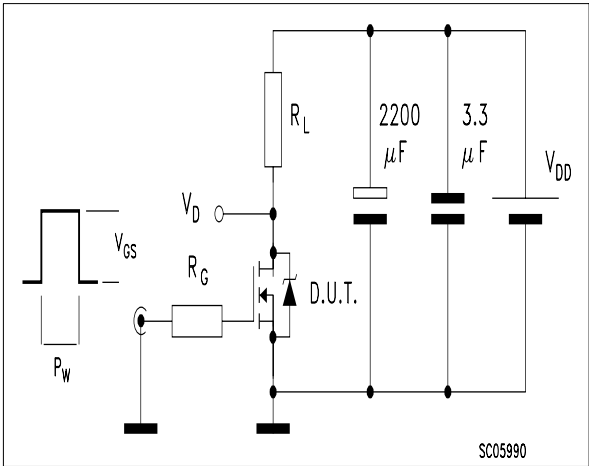


Fig. 4: Gate Charge test Circuit

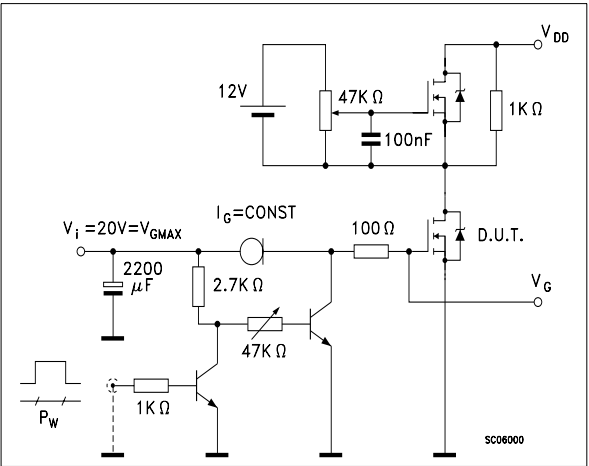
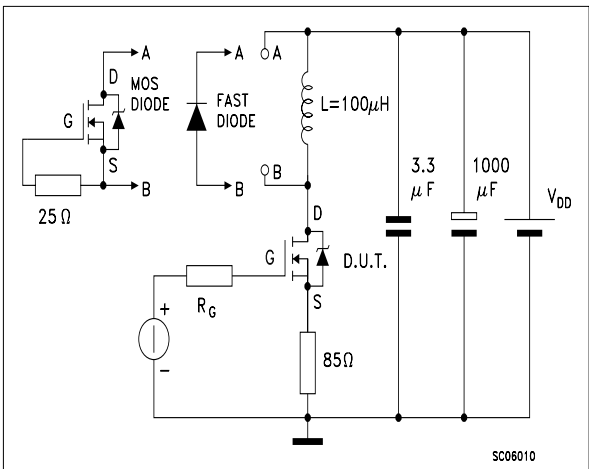
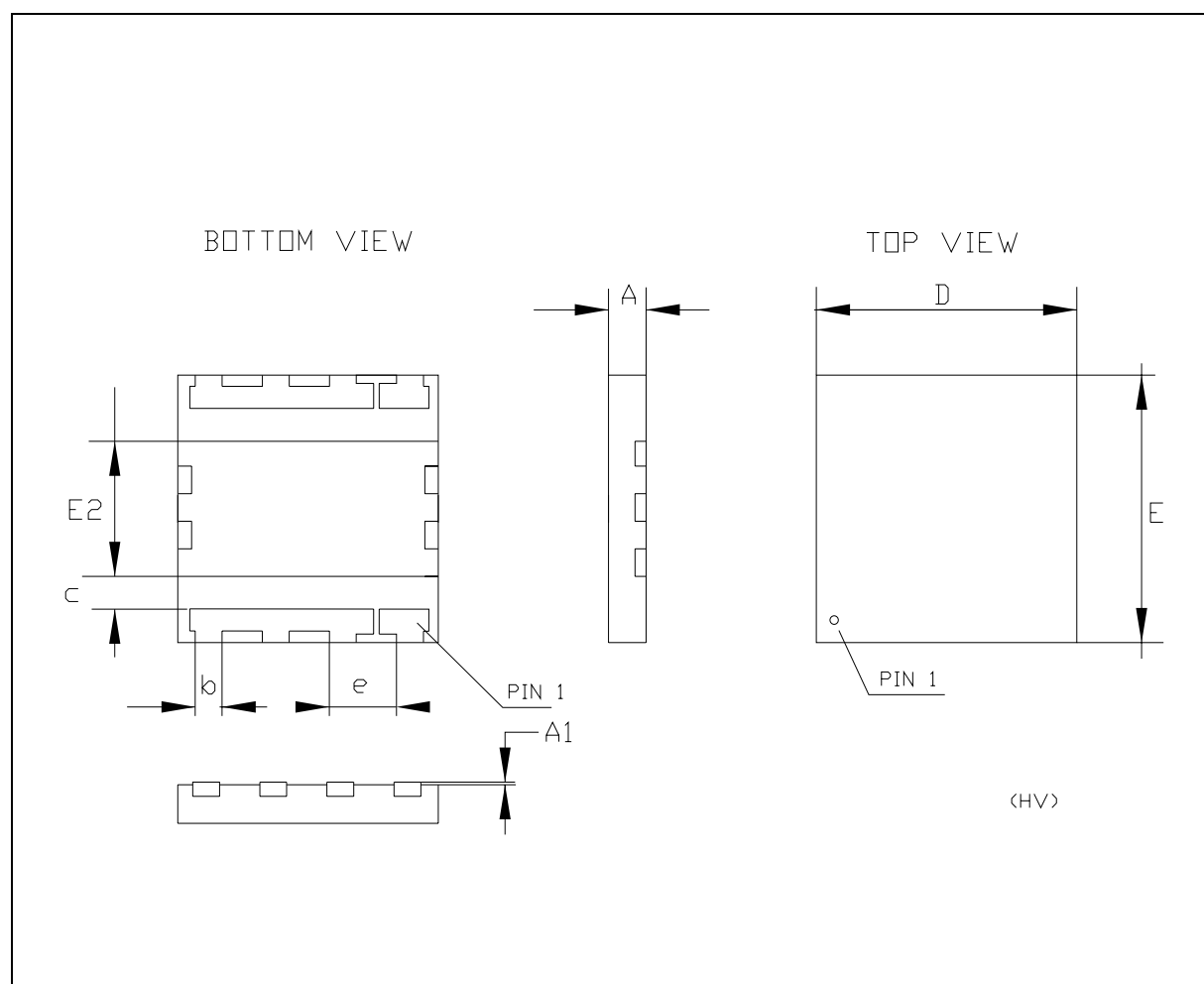


Fig. 5: Test Circuit For Inductive Load Switching And Diode Recovery Times



PowerFLAT™(5x5) MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A		0.90	1.00		0.035	0.039
A1		0.02	0.05		0.001	0.002
b	0.43	0.51	0.58	0.017	0.020	0.023
c	0.64	0.71	0.79	0.025	0.028	0.031
D		5.00			0.197	
E		5.00			0.197	
E2	2.49	2.57	2.64	0.098	0.101	0.104
e		1.27			0.050	



Information furnished is believed to be accurate and reliable. However, STMicroelectronics assumes no responsibility for the consequences of use of such information nor for any infringement of patents or other rights of third parties which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of STMicroelectronics. Specifications mentioned in this publication are subject to change without notice. This publication supersedes and replaces all information previously supplied. STMicroelectronics products are not authorized for use as critical components in life support devices or systems without express written approval of STMicroelectronics.

© The ST logo is a registered trademark of STMicroelectronics

© 2002 STMicroelectronics - Printed in Italy - All Rights Reserved
STMicroelectronics GROUP OF COMPANIES

Australia - Brazil - Canada - China - Finland - France - Germany - Hong Kong - India - Israel - Italy - Japan - Malaysia - Malta - Morocco
Singapore - Spain - Sweden - Switzerland - United Kingdom - United States.

© <http://www.st.com>