



# STL70N10F3

N-channel 100 V, 0.0078  $\Omega$ , 16 A STripFET™ III Power MOSFET  
in PowerFLAT™ 5x6 package

Datasheet — production data

## Features

| Order code | V <sub>DSS</sub> | R <sub>DS(on)</sub> max<br>@ V <sub>GS</sub> =10V | I <sub>D</sub> | P <sub>TOT</sub> |
|------------|------------------|---|----------------|------------------|
| STL70N10F3 | 100 V            | 0.0084 $\Omega$                                   | 16 A           | 136 W            |

- Improved die-to-footprint ratio
- Very low thermal resistance
- Low on-resistance

## Applications

- Switching applications

## Description

This device is an N-channel enhancement mode Power MOSFET produced using STMicroelectronics' STripFET™ III technology, which is specifically designed to minimize on-resistance and gate charge to provide superior switching performance.

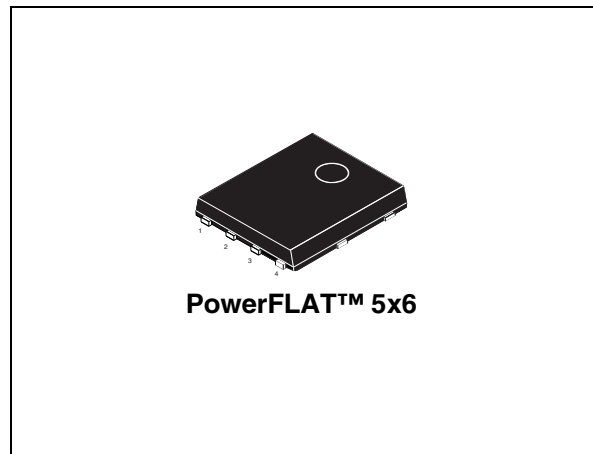


Figure 1. Internal schematic diagram

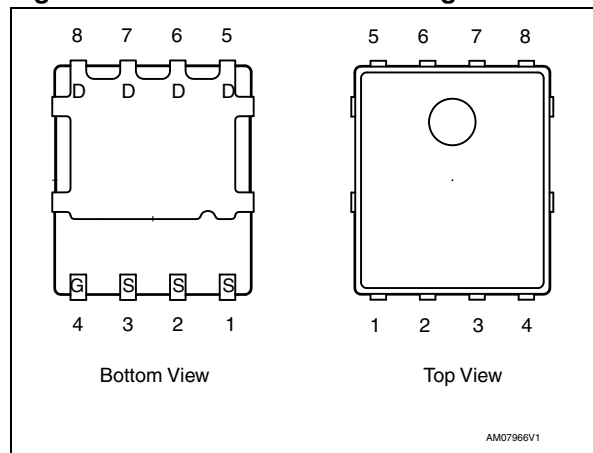


Table 1. Device summary

| Order code | Marking | Package        | Packaging     |
|------------|---------|----------------|---------------|
| STL70N10F3 | 70N10F3 | PowerFLAT™ 5x6 | Tape and reel |

## Contents

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# 1 Electrical ratings

**Table 2. Absolute maximum ratings**

| Symbol             | Parameter  | Value      | Unit             |
|--------------------|--|------------|------------------|
| $V_{DS}$           | Drain-source voltage   | 100        | V                |
| $V_{GS}$           | Gate-source voltage  | $\pm 20$   | V                |
| $I_D^{(1)}$        | Drain current (continuous) at $T_C = 25\text{ }^\circ\text{C}$     | 82         | A                |
| $I_D^{(1)}$        | Drain current (continuous) at $T_C = 100\text{ }^\circ\text{C}$    | 58         | A                |
| $I_D^{(2)}$        | Drain current (continuous) at $T_{pcb} = 25\text{ }^\circ\text{C}$ | 16         | A                |
| $I_{DM}^{(3),(2)}$ | Drain current (pulsed)   | 64         | A                |
| $P_{TOT}^{(1)}$    | Total dissipation at $T_C = 25\text{ }^\circ\text{C}$              | 136        | W                |
| $P_{TOT}^{(2)}$    | Total dissipation at $T_{pcb} = 25\text{ }^\circ\text{C}$          | 4          | W                |
| $T_J$<br>$T_{stg}$ | Operating junction temperature<br>Storage temperature              | -55 to 175 | $^\circ\text{C}$ |

1. The value is rated according to  $R_{thj-c}$ .
2. The value is rated according to  $R_{thj-pcb}$ .
3. Pulse width limited by safe operating area.

**Table 3. Thermal resistance**

| Symbol              | Parameter                        | Value | Unit               |
|---------------------|----------------------------------|-------|--------------------|
| $R_{thj-case}$      | Thermal resistance junction-case | 1.1   | $^\circ\text{C/W}$ |
| $R_{thj-pcb}^{(1)}$ | Thermal resistance junction-pcb  | 31    | $^\circ\text{C/W}$ |

1. When mounted on FR-4 board of 1inch<sup>2</sup>, 2oz Cu,  $t < 10\text{ sec}$

**Table 4. Avalanche data**

| Symbol   | Parameter   | Value | Unit |
|----------|---|-------|------|
| $I_{AV}$ | Not-repetitive avalanche current,<br>(pulse width limited by $T_J\text{ max}$ )   | 16    | A    |
| $E_{AS}$ | Single pulse avalanche energy<br>(starting $T_J = 25\text{ }^\circ\text{C}$ , $I_D = I_{AV}$ , $V_{DD} = 50\text{ V}$ ) | 770   | mJ   |

## 2 Electrical characteristics

( $T_{CASE} = 25\text{ °C}$  unless otherwise specified)

**Table 5. On/off states**

| Symbol        | Parameter  | Test conditions  | Min. | Typ.   | Max.      | Unit                           |
|---------------|--|--|------|--------|-----------|--------------------------------|
| $V_{(BR)DSS}$ | Drain-source breakdown voltage                   | $I_D = 250\text{ }\mu\text{A}$ , $V_{GS} = 0$                                | 100  | -      | -         | V                              |
| $I_{DSS}$     | Zero gate voltage drain current ( $V_{GS} = 0$ ) | $V_{DS} = 100\text{ V}$ ,<br>$V_{DS} = 100\text{ V}$ , $T_C = 125\text{ °C}$ | -    | -      | 10<br>100 | $\mu\text{A}$<br>$\mu\text{A}$ |
| $I_{GSS}$     | Gate body leakage current ( $V_{DS} = 0$ )       | $V_{GS} = \pm 20\text{ V}$   | -    | -      | $\pm 200$ | nA                             |
| $V_{GS(th)}$  | Gate threshold voltage                           | $V_{DS} = V_{GS}$ , $I_D = 250\text{ }\mu\text{A}$                           | 2    | -      | 4         | V                              |
| $R_{DS(on)}$  | Static drain-source on-resistance                | $V_{GS} = 10\text{ V}$ , $I_D = 8\text{ A}$                                  | -    | 0.0078 | 0.0084    | $\Omega$                       |

**Table 6. Dynamic**

| Symbol    | Parameter                    | Test conditions   | Min. | Typ. | Max. | Unit |
|-----------|------------------------------|---|------|------|------|------|
| $C_{iss}$ | Input capacitance            | $V_{DS} = 25\text{ V}$ , $f = 1\text{ MHz}$ ,<br>$V_{GS} = 0$ | -    | 3210 | -    | pF   |
| $C_{oss}$ | Output capacitance           |   |      | 450  |      | pF   |
| $C_{rss}$ | Reverse transfer capacitance |   |      | 16   |      | pF   |
| $Q_g$     | Total gate charge            | $V_{DD} = 50\text{ V}$ , $I_D = 16\text{ A}$                  | -    | 56   | -    | nC   |
| $Q_{gs}$  | Gate-source charge           | $V_{GS} = 10\text{ V}$  |      | 17   |      | nC   |
| $Q_{gd}$  | Gate-drain charge            | (see Figure 15)   |      | 16   |      | nC   |

**Table 7. Switching times**

| Symbol       | Parameter           | Test conditions  | Min. | Typ. | Max. | Unit |
|--------------|---------------------|--|------|------|------|------|
| $t_{d(on)}$  | Turn-on delay time  | $V_{DD} = 50\text{ V}$ , $I_D = 8\text{ A}$ ,<br>$R_G = 4.7\text{ }\Omega$ , $V_{GS} = 10\text{ V}$<br>(see Figure 14) | -    | 17   | -    | ns   |
| $t_r$        | Rise time           |  |      | 11   |      | ns   |
| $t_{d(off)}$ | Turn-off delay time |  |      | 43   |      | ns   |
| $t_f$        | Fall time           |  |      | 5.7  |      | ns   |

**Table 8. Source drain diode**

| Symbol          | Parameter                     | Test conditions   | Min | Typ. | Max. | Unit |
|-----------------|-------------------------------|---|-----|------|------|------|
| $I_{SD}$        | Source-drain current          |   | -   | -    | 16   | A    |
| $I_{SDM}^{(1)}$ | Source-drain current (pulsed) |   | -   | -    | 64   | A    |
| $V_{SD}^{(2)}$  | Forward on voltage            | $I_{SD} = 16 \text{ A}, V_{GS} = 0$   | -   | -    | 1.2  | V    |
| $t_{rr}$        | Reverse recovery time         | $I_{SD} = 16 \text{ A},$<br>$di/dt = 100 \text{ A}/\mu\text{s},$<br>$V_{DD} = 80 \text{ V}$ | -   | 56   | -    | ns   |
| $Q_{rr}$        | Reverse recovery charge       |   |     | 144  |      | nC   |
| $I_{RRM}$       | Reverse recovery current      |   |     | 5    |      | A    |

1. Pulse width limited by safe operating area.
2. Pulsed: pulse duration=300 $\mu$ s, duty cycle 1.5%.

## 2.1 Electrical characteristics (curves)

Figure 2. Safe operating area

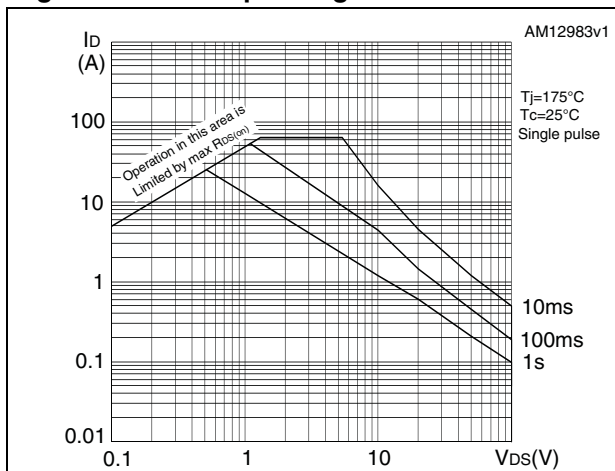


Figure 3. Thermal impedance

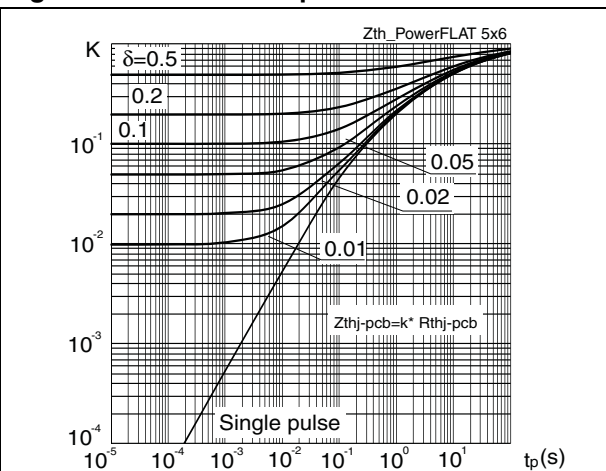


Figure 4. Output characteristics up to  $V_{DS} = 10\text{ V}$

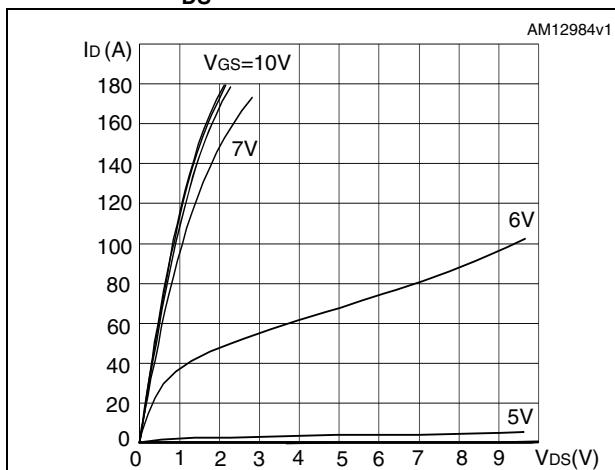


Figure 5. Output characteristics up to  $V_{DS} = 0.3\text{ V}$

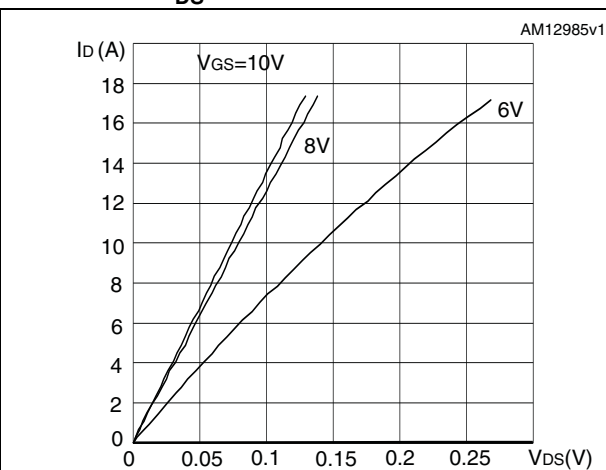


Figure 6. Transfer characteristics

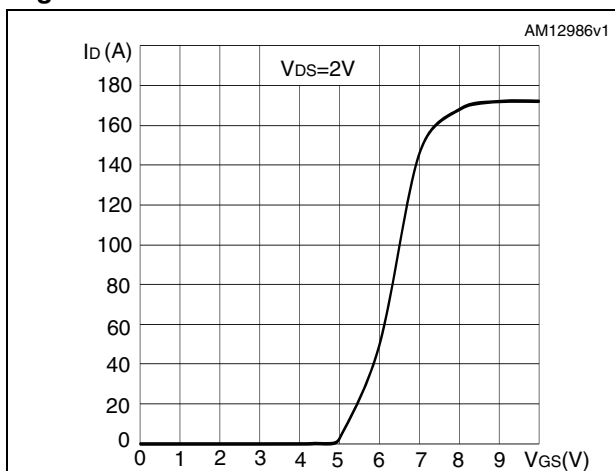
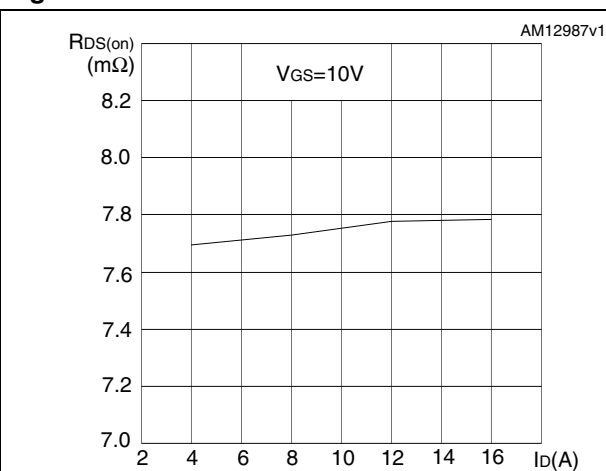
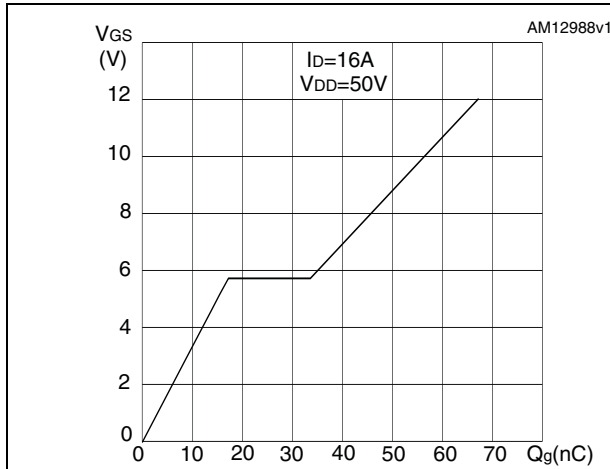


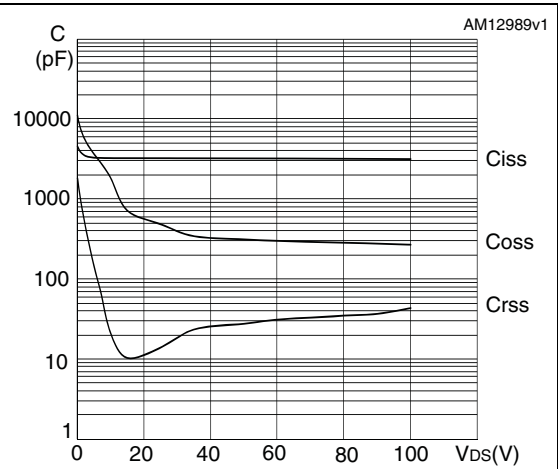
Figure 7. Static drain-source on-resistance



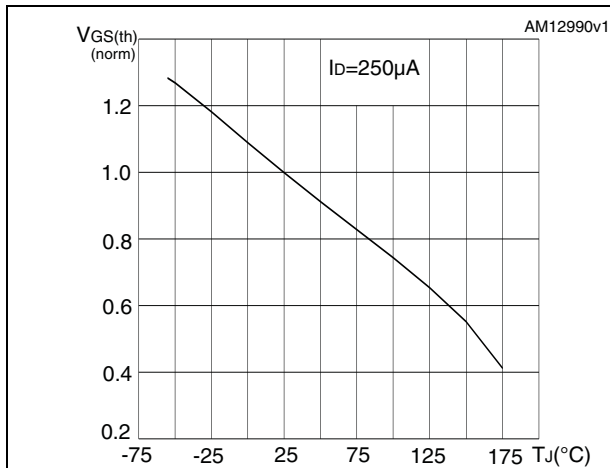
**Figure 8. Gate charge vs. gate-source voltage**



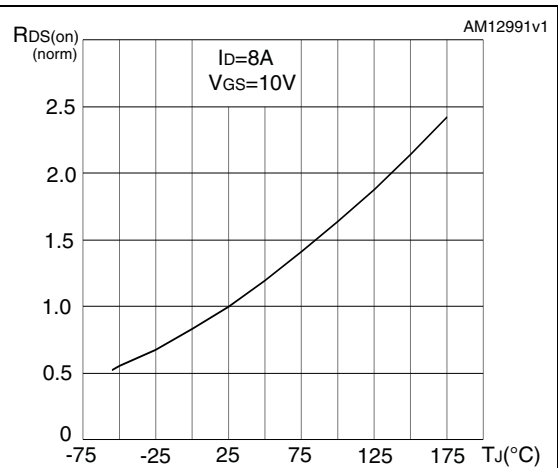
**Figure 9. Capacitance variations**



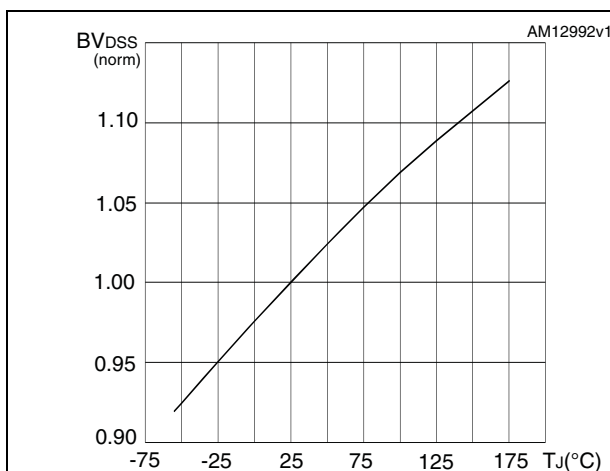
**Figure 10. Normalized gate threshold voltage vs. temperature**



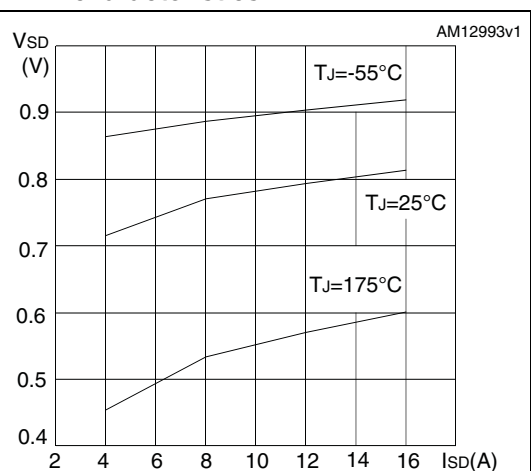
**Figure 11. Normalized on-resistance vs. temperature**



**Figure 12. Normalized BV<sub>DSS</sub> vs temperature**

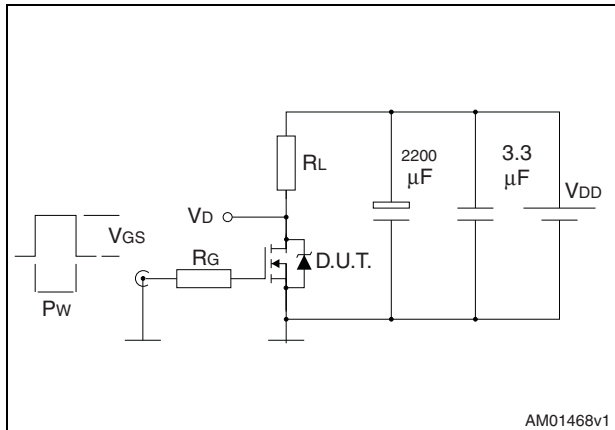


**Figure 13. Source-drain diode forward characteristics**

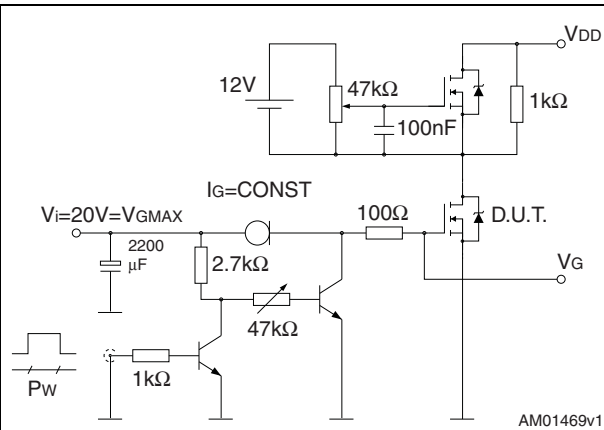


### 3 Test circuits

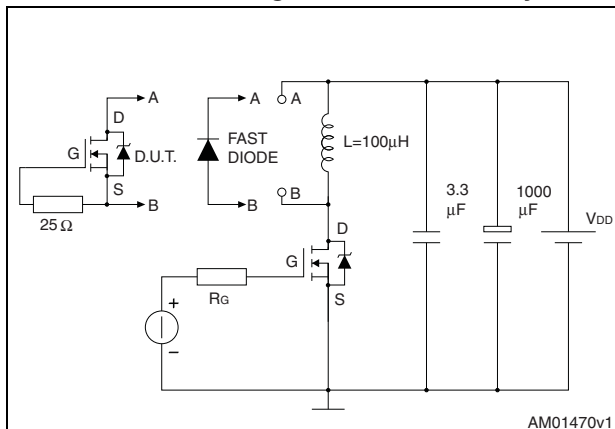
**Figure 14. Switching times test circuit for resistive load**



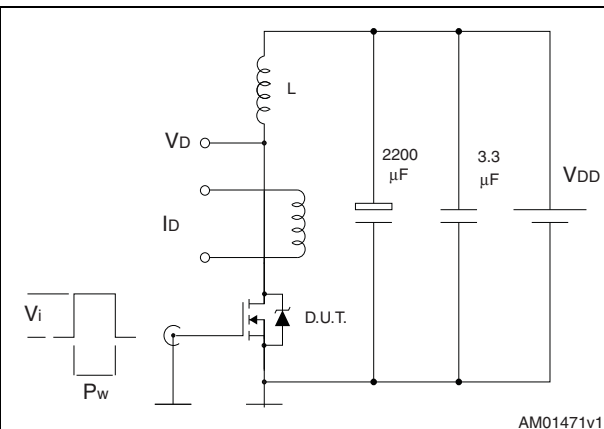
**Figure 15. Gate charge test circuit**



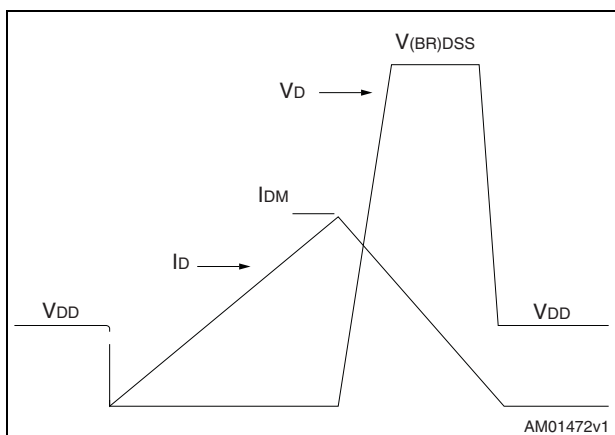
**Figure 16. Test circuit for inductive load switching and diode recovery times**



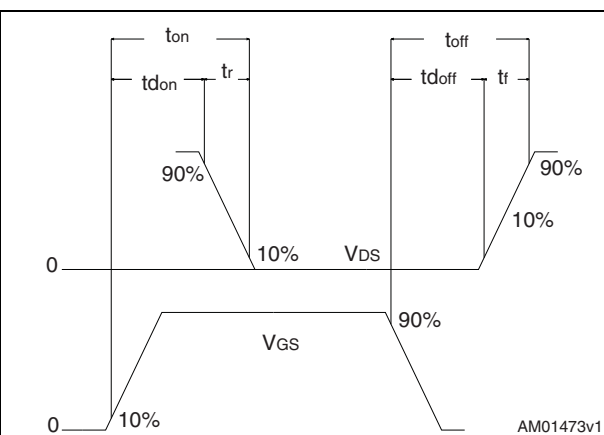
**Figure 17. Unclamped inductive load test circuit**



**Figure 18. Unclamped inductive waveform**



**Figure 19. Switching time waveform**





## 4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com). ECOPACK is an ST trademark.

**Table 9. PowerFLAT™ 5x6 type C-B mechanical data**

| Dim. | mm   |      |      |
|------|------|------|------|
|      | Min. | Typ. | Max. |
| A    | 0.80 | 0.83 | 0.93 |
| A1   | 0    | 0.02 | 0.05 |
| A3   |      | 0.20 |      |
| b    | 0.35 | 0.40 | 0.47 |
| D    |      | 5.00 |      |
| D1   |      | 4.75 |      |
| D2   | 4.15 | 4.20 | 4.25 |
| E    |      | 6.00 |      |
| E1   |      | 5.75 |      |
| E2   | 3.43 | 3.48 | 3.53 |
| E4   | 2.58 | 2.63 | 2.68 |
| e    |      | 1.27 |      |
| L    | 0.70 | 0.80 | 0.90 |

Figure 20. PowerFLAT™ 5x6 type C-B drawing

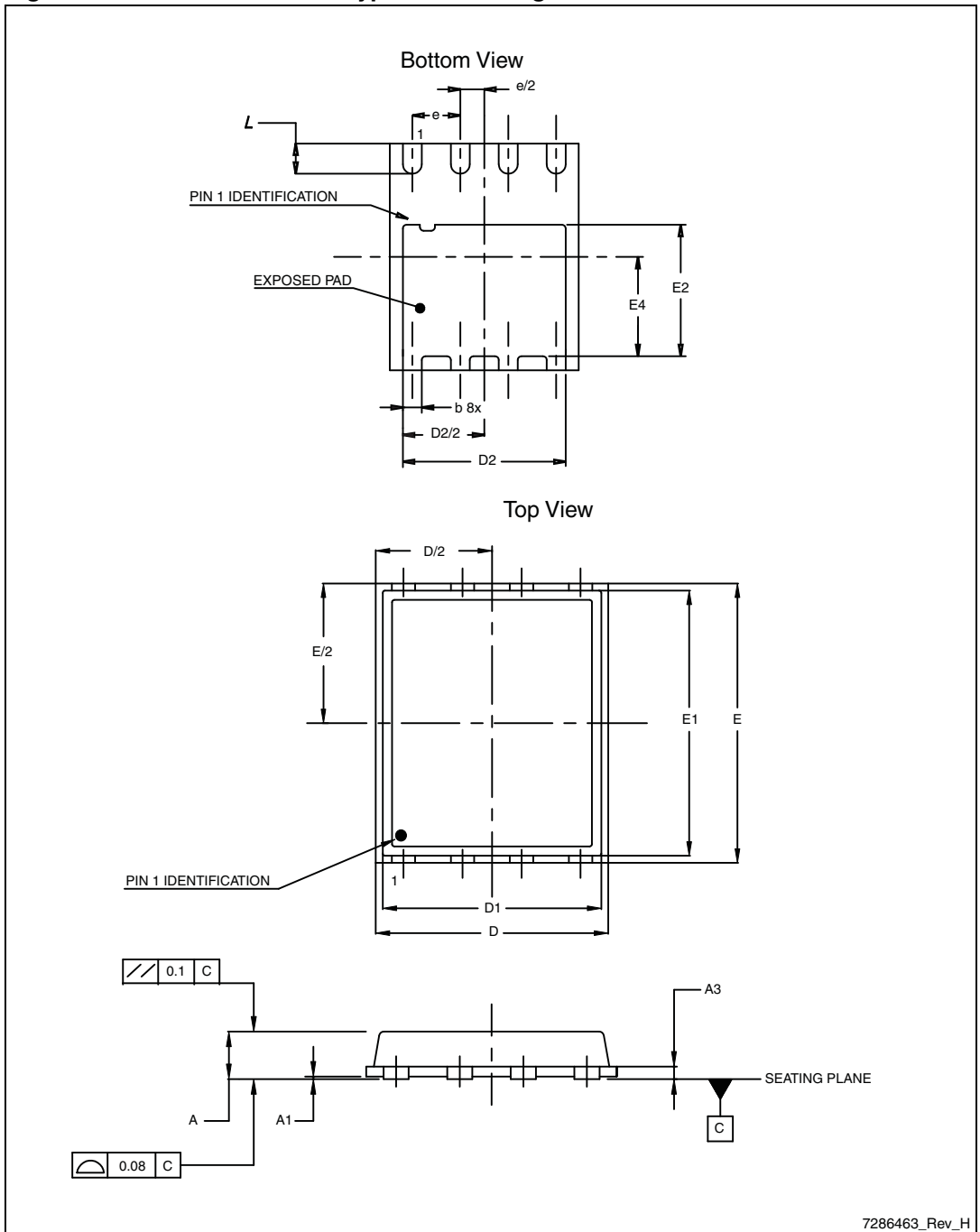


Table 10. PowerFLAT™ 5x6 type S-C mechanical data

| Dim. | mm    |      |       |
|------|-------|------|-------|
|      | Min.  | Typ. | Max.  |
| A    | 0.80  |      | 1.00  |
| A1   | 0.02  |      | 0.05  |
| A2   |       | 0.25 |       |
| b    | 0.30  |      | 0.50  |
| D    |       | 5.20 |       |
| E    |       | 6.15 |       |
| D2   | 4.11  |      | 4.31  |
| E2   | 3.50  |      | 3.70  |
| e    |       | 1.27 |       |
| e1   |       | 0.65 |       |
| L    | 0.715 |      | 1.015 |
| K    | 1.05  |      | 1.35  |

Figure 21. PowerFLAT™ 5x6 type S-C mechanical data

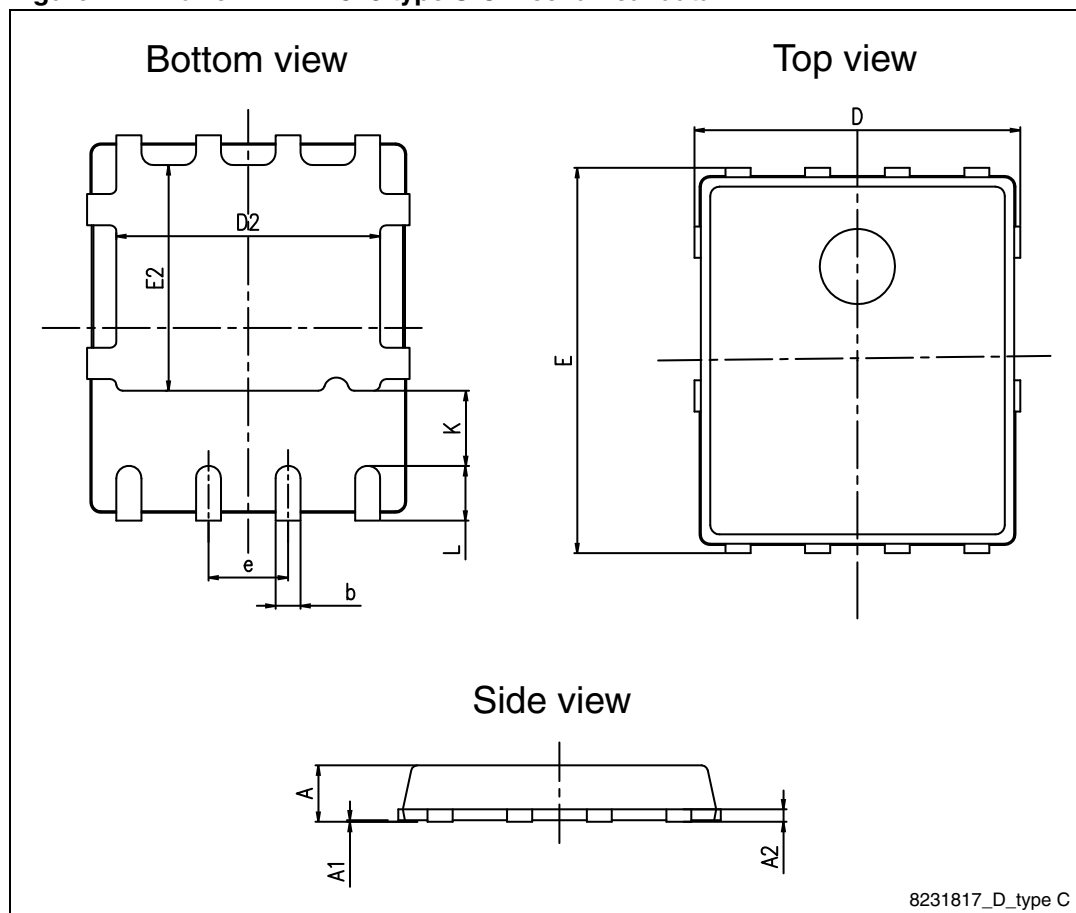
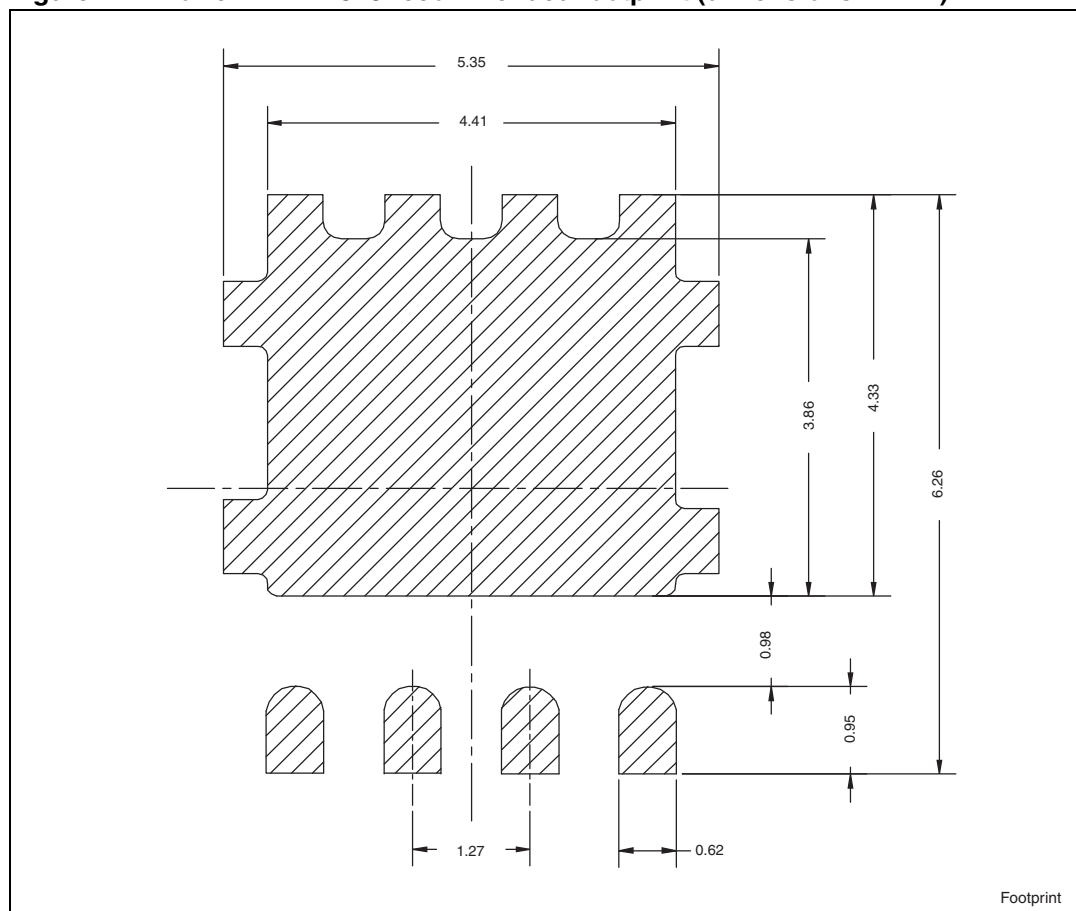


Figure 22. PowerFLAT™ 5x6 recommended footprint (dimensions in mm)



# 5 Packaging mechanical data

Figure 23. PowerFLAT™ 5x6 tape

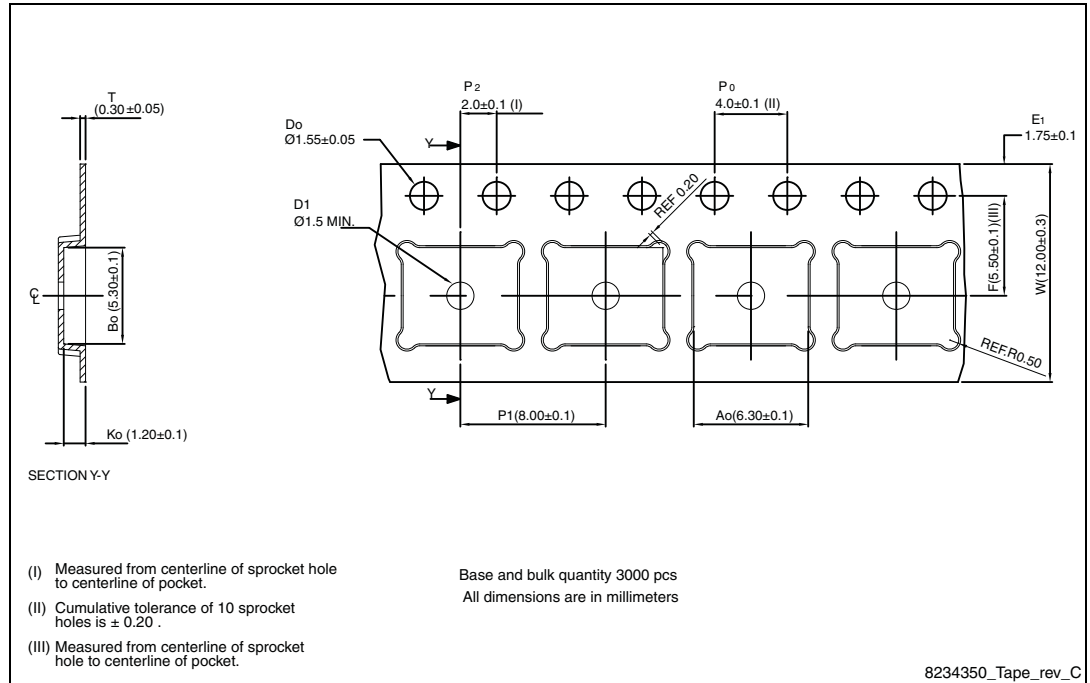


Figure 24. PowerFLAT™ 5x6 package orientation in carrier tape.

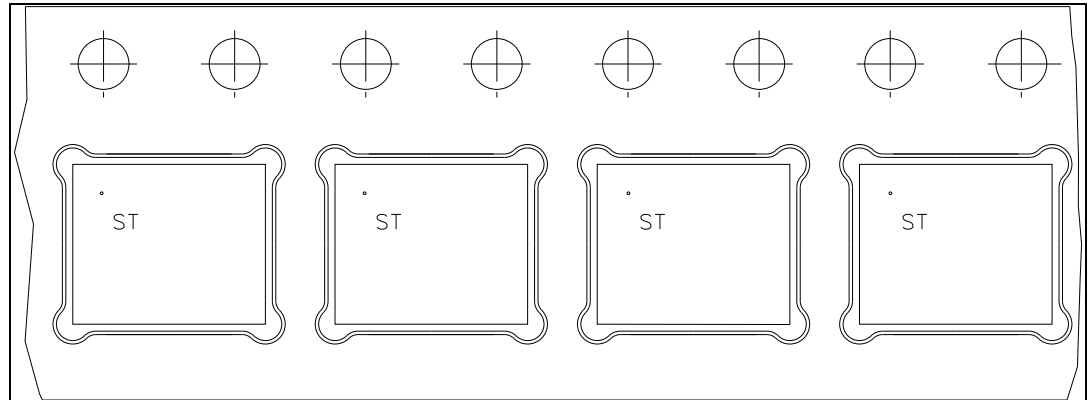
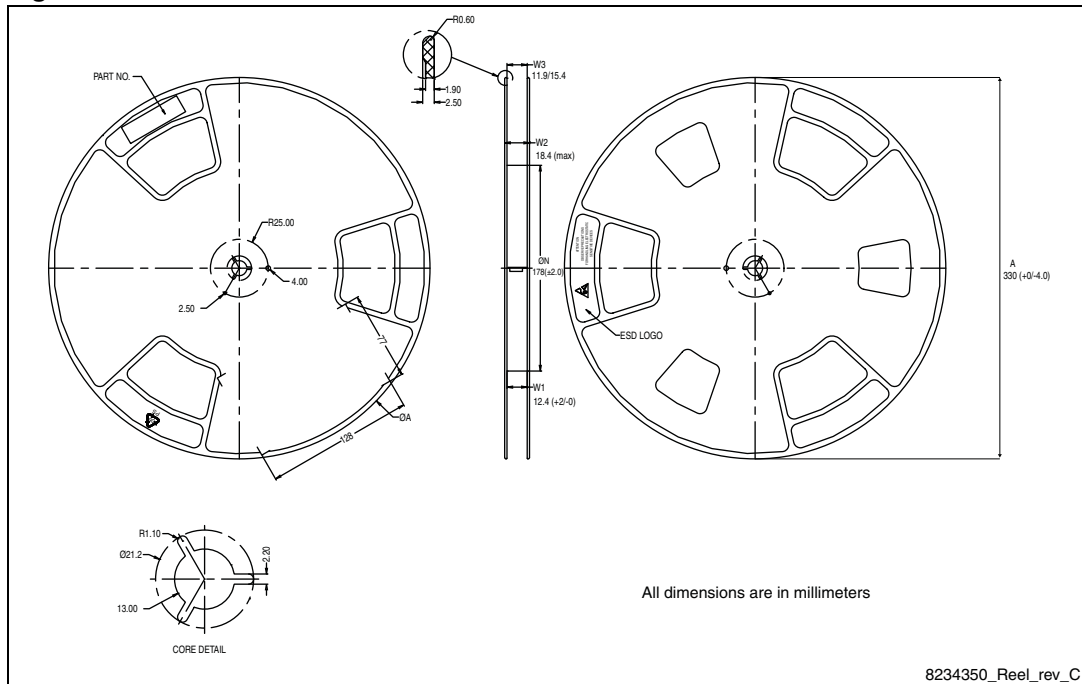


Figure 25. PowerFLAT™ 5x6 reel



## 6 Revision history

**Table 11. Document revision history**

| Date        | Revision | Changes  |
|-------------|----------|--|
| 02-Dec-2011 | 1        | First release.   |
| 13-Jan-2012 | 2        | $R_{DS(on)}$ values have been changed (see <a href="#">Table 5: On/off states</a> ). |
| 29-May-2012 | 3        | Document status promoted from preliminary data to production data.                   |



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