

## Automotive-grade N-channel 40 V, 6.1 mΩ typ., 18 A STripFET™ F5 Power MOSFET in a PowerFLAT™ 5x6 package

Datasheet - production data

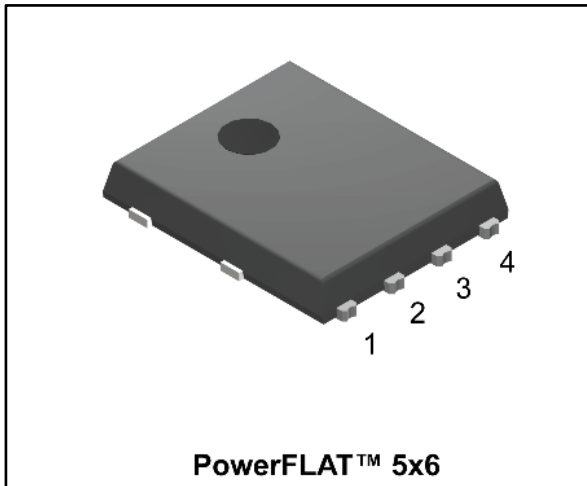
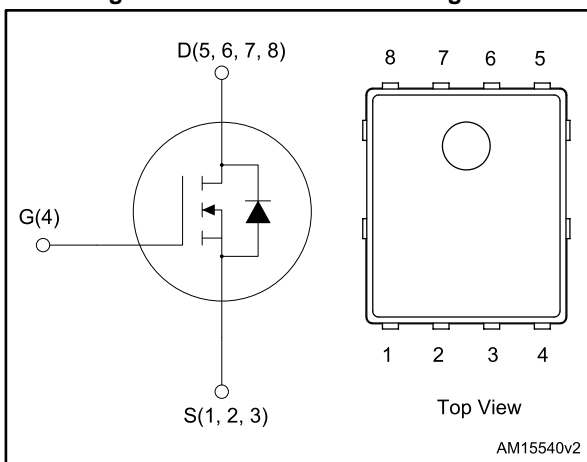


Figure 1: Internal schematic diagram



### Features

Order code	V <sub>DS</sub>	R <sub>DS(on)</sub> max.	I <sub>D</sub>
STL70N4LLF5	40 V	6.7 mΩ	18 A

- AEC-Q101 qualified
- Low on-resistance R<sub>DS(on)</sub>
- High avalanche ruggedness
- Low gate drive power loss
- Wettable flank package



### Applications

- Switching applications

### Description

This N-channel Power MOSFET is developed using the STripFET™ F5 technology and has been optimized to achieve very low on-state resistance, contributing to a FoM that is among the best in its class.

Table 1: Device summary

Order code	Marking	Package	Packing
STL70N4LLF5	70N4LLF5	PowerFLAT™ 5x6	Tape and reel

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# 1 Electrical ratings

**Table 2: Absolute maximum ratings**

Symbol	Parameter	Value	Unit
$V_{DS}$	Drain-source voltage	40	V
$V_{GS}$	Gate-source voltage	$\pm 22$	V
$I_D^{(1)}$	Drain current (continuous) at $T_C = 25\text{ }^\circ\text{C}$	70	A
$I_D^{(1)}$	Drain current (continuous) at $T_C = 100\text{ }^\circ\text{C}$	44	
$I_D^{(2)}$	Drain current (continuous) at $T_{pcb} = 25\text{ }^\circ\text{C}$	18	
$I_D^{(2)}$	Drain current (continuous) at $T_{pcb} = 100\text{ }^\circ\text{C}$	11.5	
$I_{DM}^{(1)(3)}$	Drain current (pulsed)	72	W
$P_{TOT}^{(1)}$	Total dissipation at $T_C = 25\text{ }^\circ\text{C}$	72	
$P_{TOT}^{(2)}$	Total dissipation at $T_{pcb} = 25\text{ }^\circ\text{C}$	4.8	
$T_{stg}$	Storage temperature range	-55 to 175	$^\circ\text{C}$
$T_J$	Operation junction temperature range		

**Notes:**

- (1)The value is rated according to  $R_{thj-c}$ .  
 (2)The value is rated according to  $R_{thj-pcb}$ .  
 (3)Pulse width limited by safe operating area

**Table 3: Thermal data**

Symbol	Parameter	Value	Unit
$R_{thj-case}$	Thermal resistance junction-case	2.08	$^\circ\text{C/W}$
$R_{thj-pcb}^{(1)}$	Thermal resistance junction-pcb	31.3	

**Notes:**

- (1)When mounted on FR-4 board of 1 inch<sup>2</sup>, 2oz Cu,  $t < 10\text{ s}$

**Table 4: Avalanche data**

Symbol	Parameter	Value	Unit
$I_{AV}$	Not-repetitive avalanche current (pulse width limited by $T_{jmax.}$ )	9	A
$E_{AS}$	Single pulse avalanche energy (starting $T_J = 25\text{ }^\circ\text{C}$ , $I_D = I_{AV}$ , $V_{DD} = 24\text{ V}$ )	470	mJ

## 2 Electrical characteristics

(T<sub>C</sub> = 25 °C unless otherwise specified)

**Table 5: On/off-states**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V <sub>(BR)DSS</sub>	Drain-source breakdown voltage	I <sub>D</sub> = 250 μA, V <sub>GS</sub> = 0 V	40			V
I <sub>DSS</sub>	Zero gate voltage drain current	V <sub>GS</sub> = 0 V V <sub>DS</sub> = 40 V			1	μA
I <sub>DSS</sub>	Zero gate voltage drain current	V <sub>GS</sub> = 0 V V <sub>DS</sub> = 40 V, T <sub>J</sub> = 125 °C <sup>(1)</sup>			10	
I <sub>GSS</sub>	Gate-body leakage current	V <sub>GS</sub> = ± 22 V, V <sub>DS</sub> = 0 V			±100	nA
V <sub>GS(th)</sub>	Gate threshold voltage	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250 μA	1		2.5	V
R <sub>DS(on)</sub>	Static drain-source on-resistance	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 9 A		6.1	6.7	mΩ
		V <sub>GS</sub> = 4.5 V, I <sub>D</sub> = 9 A		7.6	9.0	

**Notes:**

<sup>(1)</sup>Defined by design, not subject to production test

**Table 6: Dynamic**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C <sub>iss</sub>	Input capacitance	V <sub>DS</sub> = 25 V, f = 1 MHz, V <sub>GS</sub> = 0 V	-	1570	-	pF
C <sub>oss</sub>	Output capacitance		-	257	-	pF
C <sub>rss</sub>	Reverse transfer capacitance		-	32	-	pF
Q <sub>g</sub>	Total gate charge	V <sub>DD</sub> = 15 V, I <sub>D</sub> = 18 A, V <sub>GS</sub> = 4.5 V (see <a href="#">Figure 14: "Test circuit for gate charge behavior"</a> )	-	12.9	-	nC
Q <sub>gs</sub>	Gate-source charge		-	3.9	-	nC
Q <sub>gd</sub>	Gate-drain charge		-	5.3	-	nC
R <sub>G</sub>	Gate input resistance	f = 1 MHz, gate DC bias = 0 V, test signal level = 20 mV, I <sub>D</sub> = 0 A	-	1.5	-	Ω

**Table 7: Switching times**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
t <sub>d(on)</sub>	Turn-on delay time	V <sub>DD</sub> = 15 V, I <sub>D</sub> = 9 A, R <sub>G</sub> = 4.7 Ω, V <sub>GS</sub> = 10 V (see <a href="#">Figure 13: "Test circuit for resistive load switching times"</a> )	-	14	-	ns
t <sub>r</sub>	Rise time		-	42	-	ns
t <sub>d(off)</sub>	Turn-off delay time		-	37	-	ns
t <sub>f</sub>	Fall time		-	5.2	-	ns

Table 8: Source-drain diode

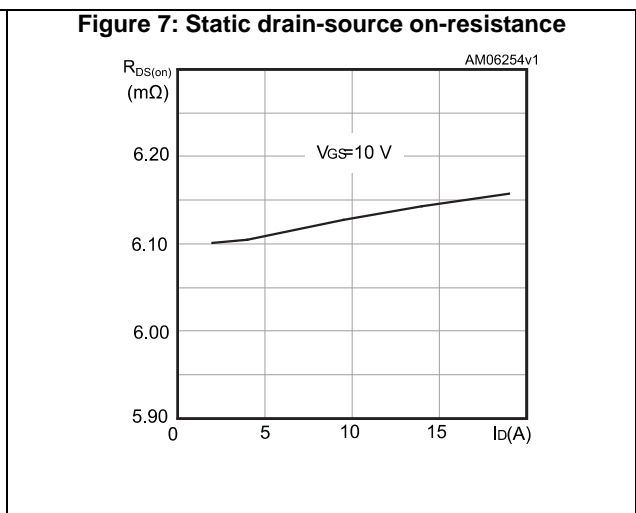
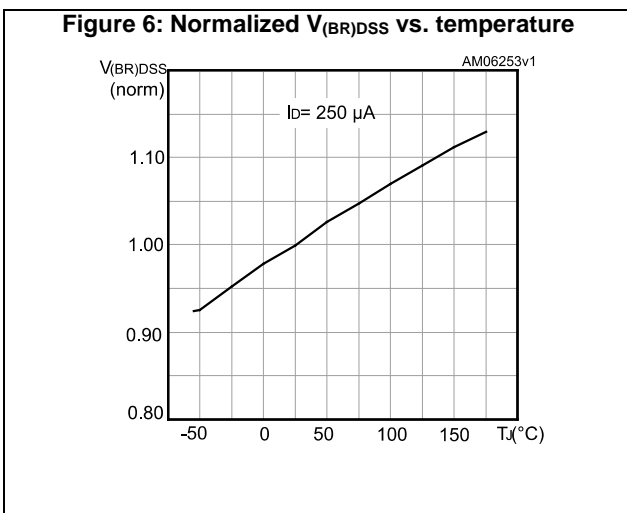
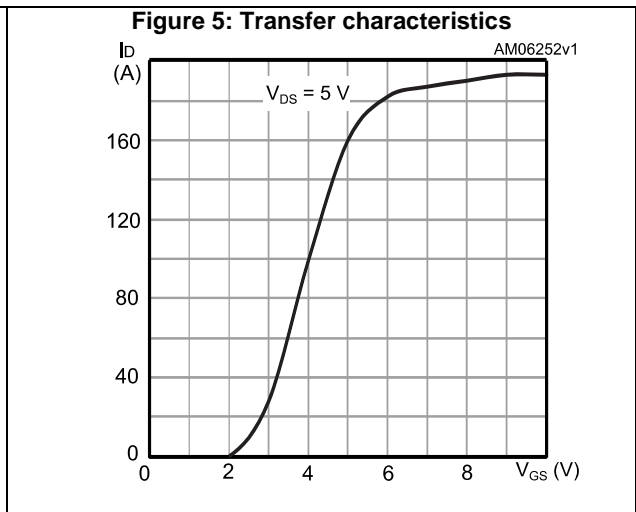
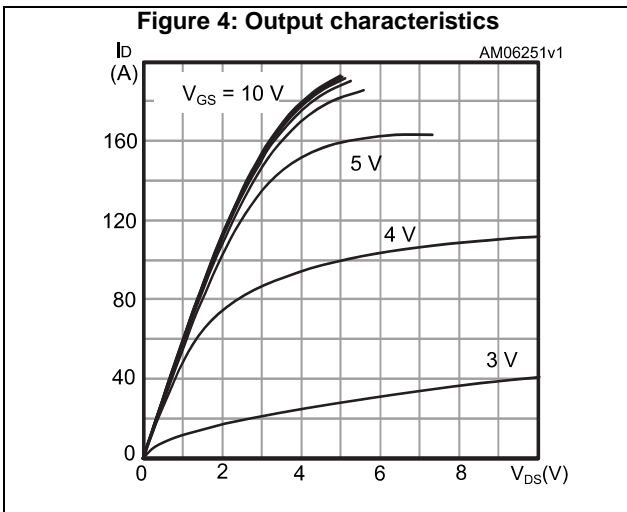
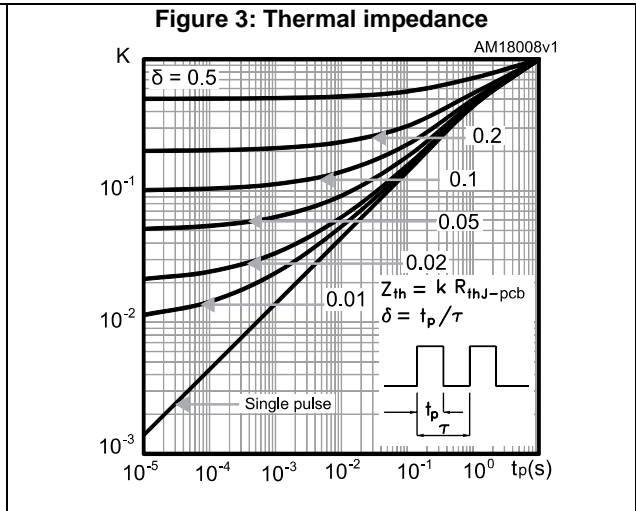
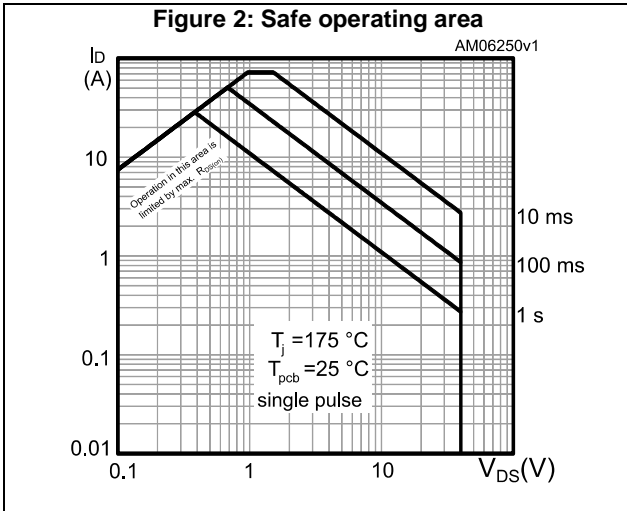
Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$I_{SD}$	Source-drain current		-		18	A
$I_{SDM}^{(1)}$	Source-drain current pulsed		-		72	A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD} = 18 \text{ A}$ , $V_{GS} = 0 \text{ V}$			1.1	V
$t_{rr}$	Reverse recovery time	$I_{SD} = 18 \text{ A}$ , $di/dt = 100 \text{ A}/\mu\text{s}$ , $V_{DD} = 25 \text{ V}$ , $T_J = 150 \text{ }^\circ\text{C}$	-	27.2		ns
$Q_{rr}$	Reverse recovery charge		-	24.5		nC
$I_{RRM}$	Reverse recovery current		-	1.8		A

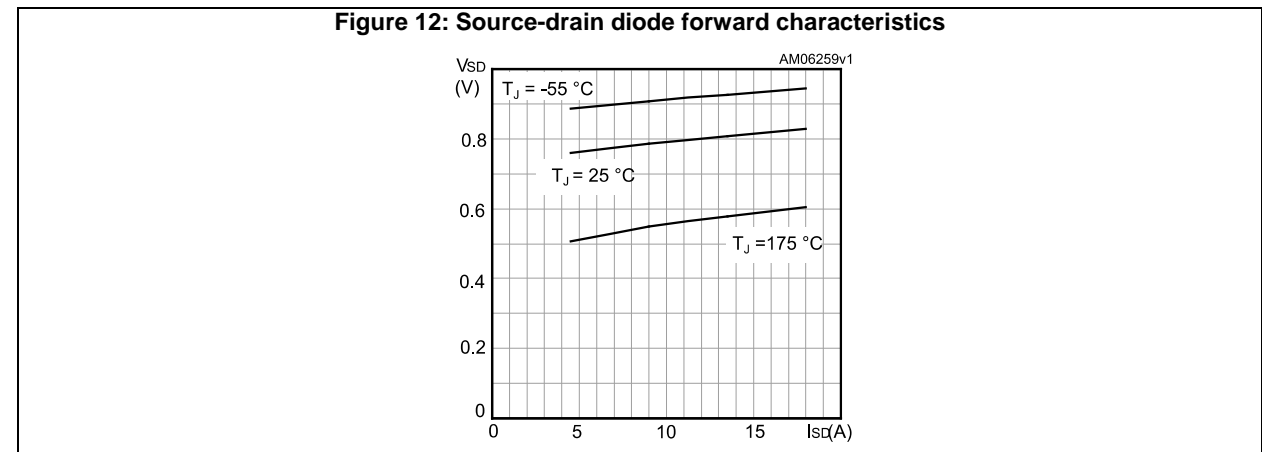
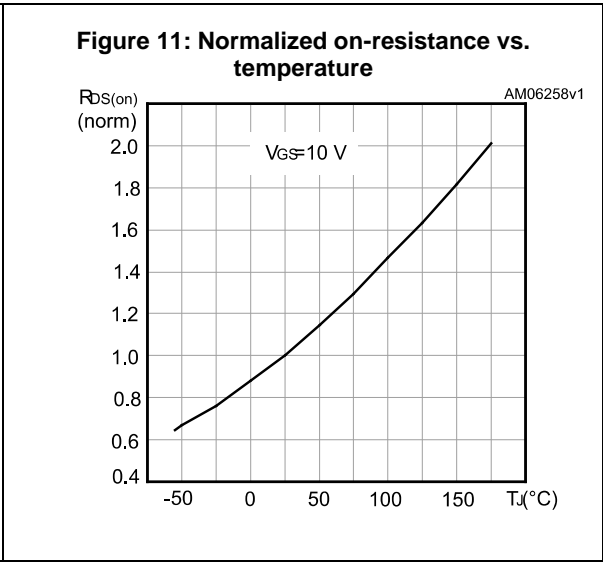
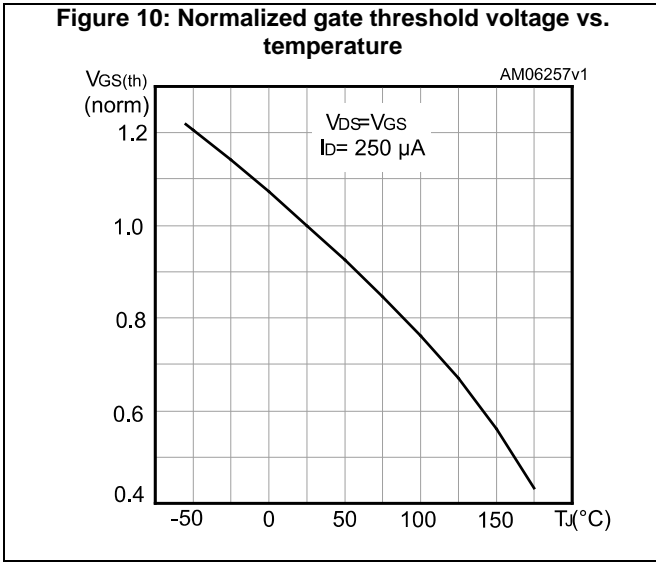
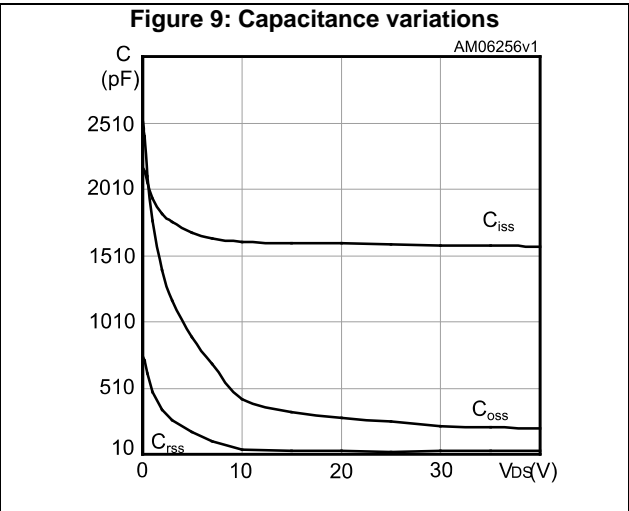
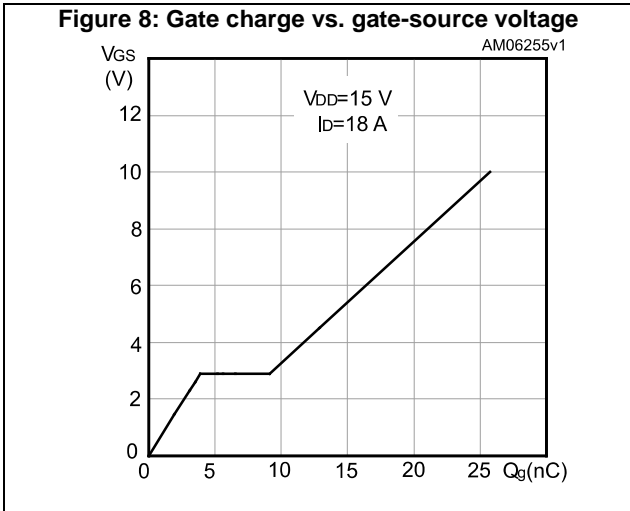
**Notes:**

(1)Pulse width limited by safe operating area.

(2)Pulsed: pulse duration = 300  $\mu\text{s}$ , duty cycle 1.5%

## 2.2 Electrical characteristics (curves)





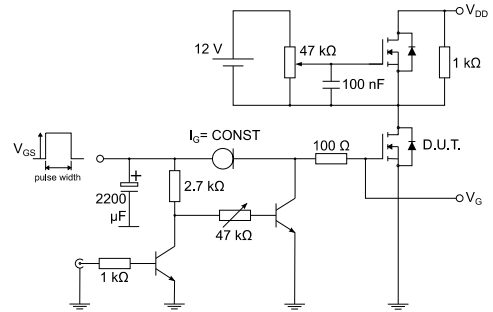
### 3 Test circuits

**Figure 13: Test circuit for resistive load switching times**



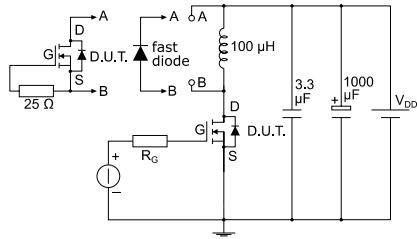
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**Figure 14: Test circuit for gate charge behavior**



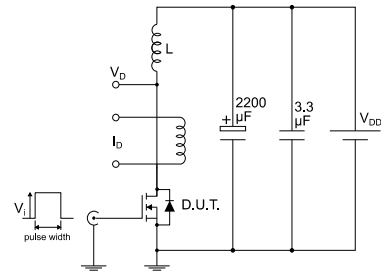
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**Figure 15: Test circuit for inductive load switching and diode recovery times**



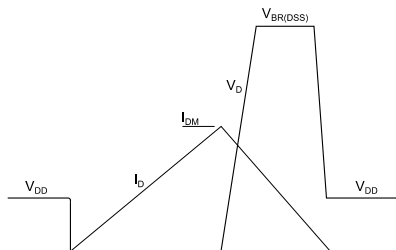
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**Figure 16: Unclamped inductive load test circuit**



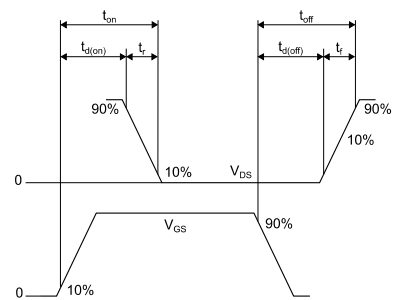
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**Figure 17: Unclamped inductive waveform**



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**Figure 18: Switching time waveform**



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## 4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com). ECOPACK® is an ST trademark.

### 4.1 PowerFLAT™ 5x6 single island WF type C package information

Figure 19: PowerFLAT™ 5x6 WF type C package outline

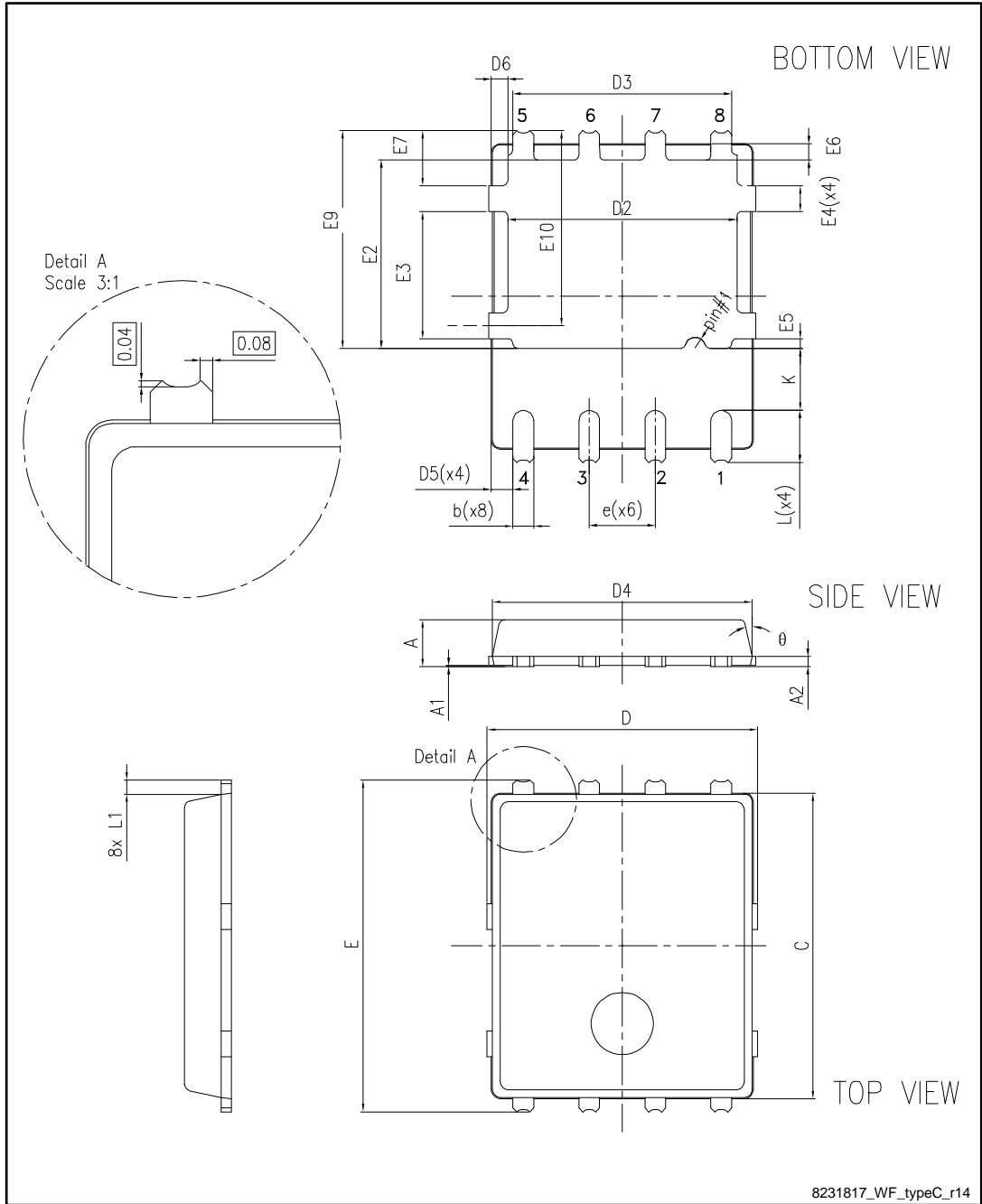
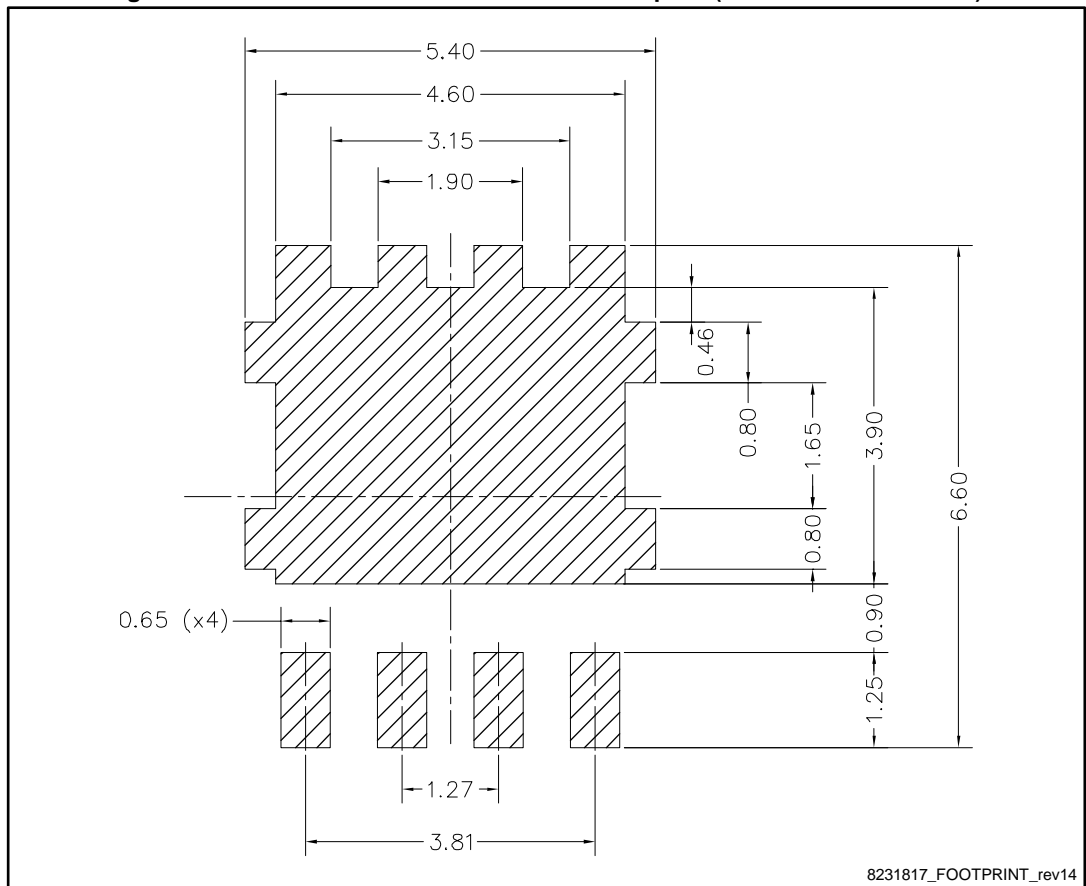


Table 9: PowerFLAT™ 5x6 WF type C mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	0.80		1.00
A1	0.02		0.05
A2		0.25	
b	0.30		0.50
C	5.80	6.00	6.10
D	5.00	5.20	5.40
D2	4.15		4.45
D3	4.05	4.20	4.35
D4	4.80	5.00	5.10
D5	0.25	0.40	0.55
D6	0.15	0.30	0.45
e		1.27	
E	6.20	6.40	6.60
E2	3.50		3.70
E3	2.35		2.55
E4	0.40		0.60
E5	0.08		0.28
E6	0.20	0.325	0.45
E7	0.85	1.00	1.15
E9	4.00	4.20	4.40
E10	3.55	3.70	3.85
K	1.05		1.35
L	0.90	1.00	1.10
L1	0.175	0.275	0.375
θ	0°		12°

Figure 20: PowerFLAT™ 5x6 recommended footprint (dimensions are in mm)



## 4.2 Packing information

Figure 21: PowerFLAT™ 5x6 WF tape (dimensions are in mm)

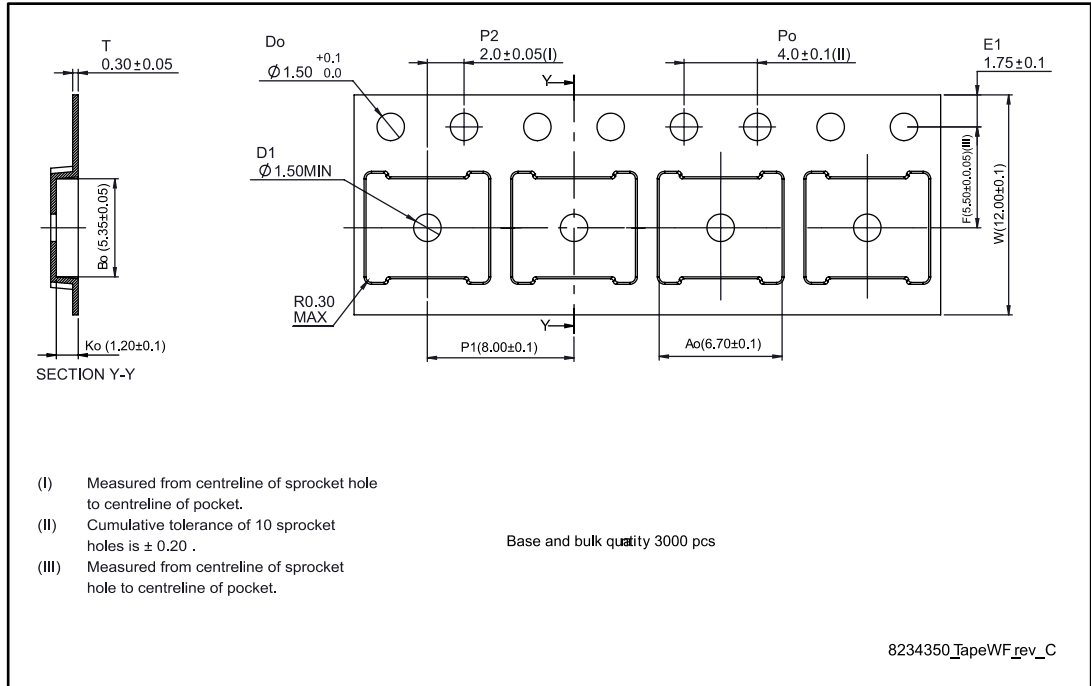


Figure 22: PowerFLAT™ 5x6 package orientation in carrier tape

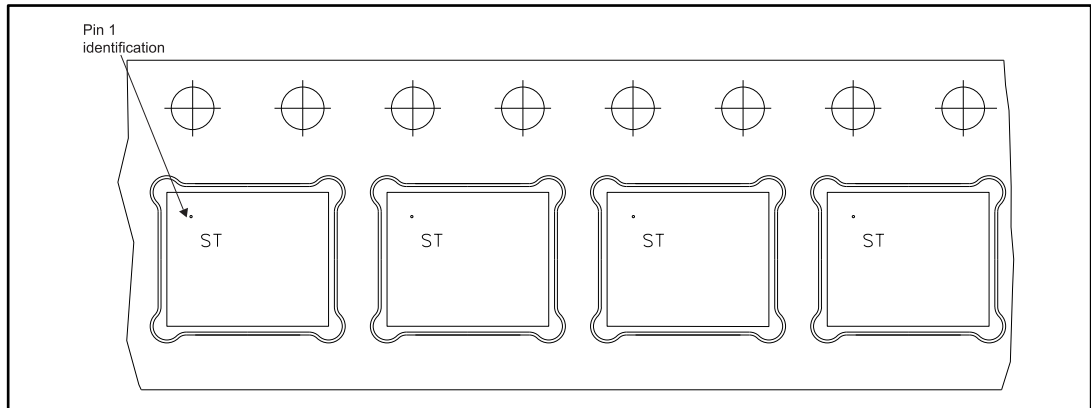
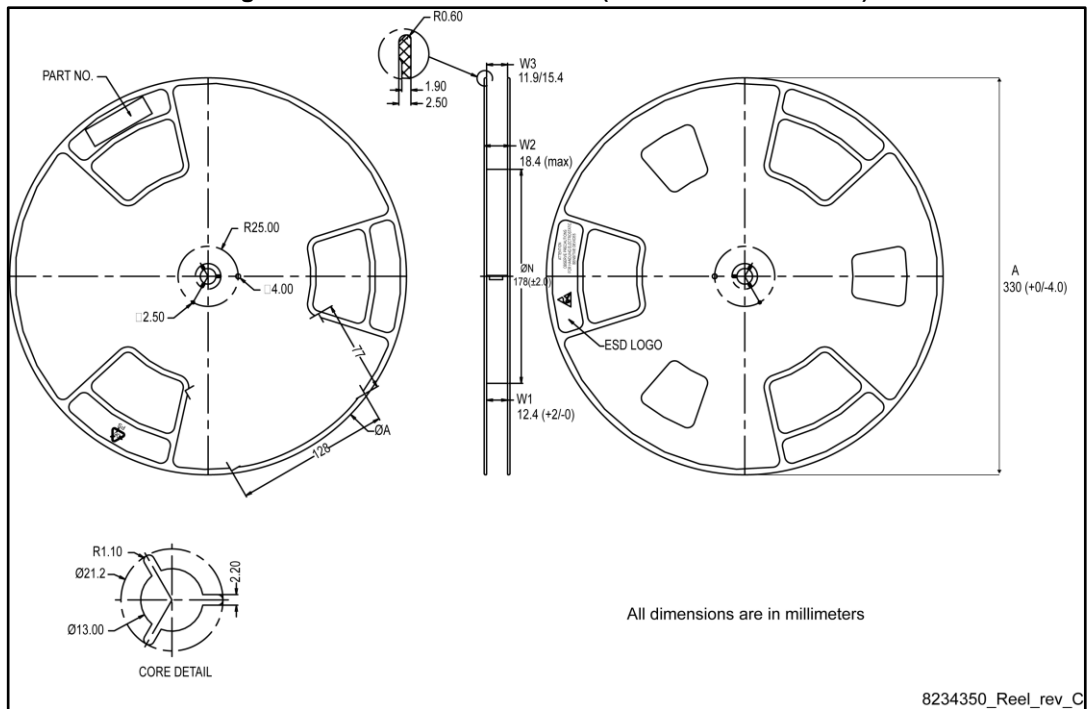


Figure 23: PowerFLAT™ 5x6 reel (dimensions are in mm)



## 5 Revision history

**Table 10: Document revision history**

Date	Revision	Changes
01-Dec-2008	1	First release.
18-Jul-2011	2	Section 4: Package mechanical data has been modified: <ul style="list-style-type: none"> <li>– Added <i>Table 9: PowerFLAT™ 5x6 type S-C mechanical data</i></li> <li>– Added <i>Figure 19: PowerFLAT™ 5x6 type S-C mechanical data</i></li> <li>– Added <i>PowerFLAT™ 5x6 type C-B mechanical data</i></li> <li>– Added <i>PowerFLAT™ 5x6 type C-B drawing</i> Minor text changes.</li> </ul>
21-Dec-2011	3	Section 4: Package mechanical data has been modified.
25-Jan-2013	4	<ul style="list-style-type: none"> <li>– Table 1: Device summary has been updated.</li> <li>-Minor text changes.</li> <li>–Changed: <i>Figure 1</i></li> <li>-Added <i>Section 5: Packaging mechanical data</i>.</li> </ul>
12-Feb-2013	5	<ul style="list-style-type: none"> <li>-Updated <math>T_J</math> and <math>T_{stg}</math> in Table 2: Absolute maximum ratings.</li> <li>– Updated <i>Section 4: Package mechanical data</i> and <i>Figure 22: PowerFLAT™ 5x6 package orientation in carrier tape</i>.</li> </ul>
24-May-2013	6	<ul style="list-style-type: none"> <li>– Modified: title and <i>Section 4: Package mechanical data</i></li> <li>- Minor text changes.</li> </ul>
17-Dec-2014	7	<ul style="list-style-type: none"> <li>– Modified: Figure 2 and 3</li> <li>– Updated: Figure 13, 14, 15 and 16</li> <li>– Updated: <i>Section 4: Package mechanical data</i> and <i>Section 5: Packaging mechanical data</i></li> <li>– Minor text changes.</li> </ul>
08-Apr-2016	8	<ul style="list-style-type: none"> <li>– Updated <i>Section 4: Package information</i> and <i>Section 4.1: Packing information</i></li> <li>-Minor text changes.</li> </ul>
22-Sep-2016	9	Updated $V_{GS(th)}$ in <a href="#">Table 5: "On/off-states"</a> .

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