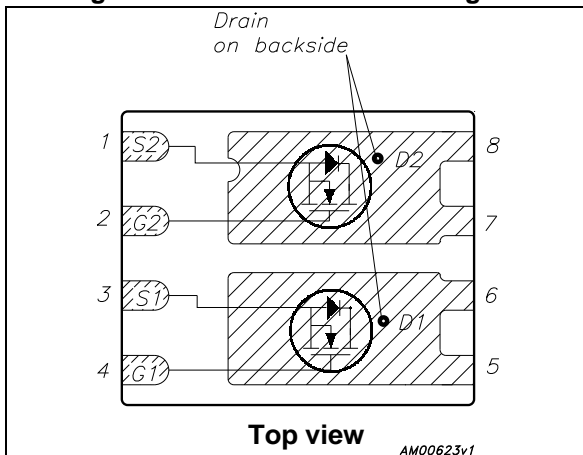


## Automotive-grade dual N-channel 60 V, 35 mΩ typ., 6.5 A STripFET™ F3 Power MOSFET in PowerFLAT™ 5x6 double island

Datasheet - production data



Figure 1. Internal schematic diagram



### Features

| Order code | V <sub>DS</sub> | R <sub>DS(on)</sub> max | I <sub>D</sub> |
|------------|-----------------|-------------------------|----------------|
| STL7DN6LF3 | 60 V            | 43 mΩ                   | 6.5 A          |

- Designed for automotive application and AEC-Q101 qualified
- Logic level V<sub>GS(th)</sub>
- 175 °C junction temperature
- 100% avalanche rated
- Wettable flank package

### Applications

- Switching applications

### Description

This device is a dual N-channel Power MOSFET developed using STripFET™ F3 technology. It is designed to minimize on-resistance and gate charge to provide superior switching performance.

Table 1. Device summary

| Order code | Marking | Package                                     | Packaging     |
|------------|---------|---|---------------|
| STL7DN6LF3 | 7DN6LF3 | PowerFLAT™ 5x6 double island <sup>(1)</sup> | Tape and reel |

1. For wettable flank option, please contact ST sale offices.

# Contents

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# 1 Electrical ratings

**Table 2. Absolute maximum ratings**

| Symbol             | Parameter   | Value      | Unit             |
|--------------------|---|------------|------------------|
| $V_{DS}$           | Drain-source voltage  | 60         | V                |
| $V_{GS}$           | Gate-source voltage   | $\pm 20$   | V                |
| $I_D^{(1),(2)}$    | Drain current (continuous) at $T_C = 25^\circ\text{C}$      | 20         | A                |
| $I_D^{(1)}$        | Drain current (continuous) at $T_C = 100^\circ\text{C}$     | 16         | A                |
| $I_D^{(4)}$        | Drain current (continuous) at $T_{pcb} = 25^\circ\text{C}$  | 6.5        | A                |
| $I_D^{(4)}$        | Drain current (continuous) at $T_{pcb} = 100^\circ\text{C}$ | 4.6        | A                |
| $I_{DM}^{(3),(4)}$ | Drain current (pulsed)                                      | 26         | A                |
| $P_{TOT}$          | Total dissipation at $T_C = 25^\circ\text{C}$               | 52         | W                |
| $P_{TOT}^{(4)}$    | Total dissipation at $T_{pcb} = 25^\circ\text{C}$           | 4.3        | W                |
| $I_{AV}$           | Not-repetitive avalanche current                            | 6.5        | A                |
| $E_{AS}^{(5)}$     | Single pulse avalanche energy                               | 190        | mJ               |
| $T_J$<br>$T_{stg}$ | Operating junction temperature<br>Storage temperature       | -55 to 175 | $^\circ\text{C}$ |

1. Specified by design. Not subject to production test.
2. Current is limited by bonding, with an  $R_{thJC} = 2.9^\circ\text{C/W}$  the chip is able to carry 22 A at  $25^\circ\text{C}$ .
3. Pulse width limited by safe operating area
4. When mounted on FR-4 board of  $1\text{inch}^2$ , 2oz Cu,  $t < 10\text{ sec}$
5. Starting  $T_J = 25^\circ\text{C}$ ,  $I_D = 8\text{ A}$ ,  $V_{DD} = 25\text{ V}$

**Table 3. Thermal resistance**

| Symbol              | Parameter                        | Value | Unit               |
|---------------------|----------------------------------|-------|--------------------|
| $R_{thj-case}$      | Thermal resistance junction-case | 2.9   | $^\circ\text{C/W}$ |
| $R_{thj-pcb}^{(1)}$ | Thermal resistance junction-pcb  | 35    | $^\circ\text{C/W}$ |

1. When mounted on FR-4 board of  $1\text{inch}^2$ , 2oz Cu,  $t < 10\text{ sec}$

## 2 Electrical characteristics

( $T_{CASE} = 25\text{ }^{\circ}\text{C}$  unless otherwise specified)

**Table 4. On/off states**

| Symbol        | Parameter  | Test conditions   | Min. | Typ.     | Max.      | Unit                                 |
|---------------|--|---|------|----------|-----------|--------------------------------------|
| $V_{(BR)DSS}$ | Drain-source breakdown voltage ( $V_{GS} = 0$ )  | $I_D = 250\text{ }\mu\text{A}$  | 60   |          |           | V                                    |
| $I_{DSS}$     | Zero gate voltage drain current ( $V_{GS} = 0$ ) | $V_{DS} = 60\text{ V}$  |      |          | 1         | $\mu\text{A}$                        |
| $I_{GSS}$     | Gate body leakage current ( $V_{DS} = 0$ )       | $V_{GS} = \pm 20\text{ V}$  |      |          | $\pm 100$ | nA                                   |
| $V_{GS(th)}$  | Gate threshold voltage                           | $V_{DS} = V_{GS}$ , $I_D = 250\text{ }\mu\text{A}$  | 1    |          | 2.5       | V                                    |
| $R_{DS(on)}$  | Static drain-source on-resistance                | $V_{GS} = 10\text{ V}$ , $I_D = 3\text{ A}$<br>$V_{GS} = 5\text{ V}$ , $I_D = 3\text{ A}$ |      | 35<br>48 | 43<br>60  | $\text{m}\Omega$<br>$\text{m}\Omega$ |

**Table 5. Dynamic**

| Symbol    | Parameter                    | Test conditions   | Min. | Typ. | Max. | Unit     |
|-----------|------------------------------|---|------|------|------|----------|
| $C_{iss}$ | Input capacitance            | $V_{DS} = 25\text{ V}$ , $f = 1\text{ MHz}$ ,<br>$V_{GS} = 0$                                       | -    | 432  | -    | pF       |
| $C_{oss}$ | Output capacitance           |   | -    | 93   | -    | pF       |
| $C_{rss}$ | Reverse transfer capacitance |   | -    | 10.5 | -    | pF       |
| $Q_g$     | Total gate charge            | $V_{DD} = 30\text{ V}$ , $I_D = 6.5\text{ A}$<br>$V_{GS} = 10\text{ V}$ , <a href="#">Figure 13</a> | -    | 8.7  | -    | nC       |
| $Q_{gs}$  | Gate-source charge           |   | -    | 1.9  | -    | nC       |
| $Q_{gd}$  | Gate-drain charge            |   | -    | 1.9  | -    | nC       |
| $R_G$     | Intrinsic gate resistance    | $f = 1\text{ MHz}$ open drain   | -    | 6.3  | -    | $\Omega$ |

**Table 6. Switching times**

| Symbol       | Parameter           | Test conditions  | Min. | Typ. | Max. | Unit |
|--------------|---------------------|--|------|------|------|------|
| $t_{d(on)}$  | Turn-on delay time  | $V_{DD} = 30\text{ V}$ , $I_D = 3\text{ A}$ ,<br>$R_G = 4.7\text{ }\Omega$ , $V_{GS} = 10\text{ V}$<br><a href="#">Figure 12</a> | -    | 6.7  | -    | ns   |
| $t_r$        | Rise time           |  | -    | 10.4 | -    | ns   |
| $t_{d(off)}$ | Turn-off delay time |  | -    | 32.4 | -    | ns   |
| $t_f$        | Fall time           |  | -    | 5.4  | -    | ns   |

Table 7. Source drain diode

| Symbol          | Parameter                     | Test conditions  | Min | Typ. | Max | Unit |
|-----------------|-------------------------------|--|-----|------|-----|------|
| $I_{SD}$        | Source-drain current          |  | -   |      | 6.5 | A    |
| $I_{SDM}^{(1)}$ | Source-drain current (pulsed) |  | -   |      | 26  | A    |
| $V_{SD}^{(2)}$  | Forward on voltage            | $I_{SD} = 6.5 \text{ A}, V_{GS} = 0$   | -   |      | 1.3 | V    |
| $t_{rr}$        | Reverse recovery time         | $I_{SD} = 6.5 \text{ A},$<br>$di/dt = 100 \text{ A}/\mu\text{s},$<br>$V_{DD} = 48 \text{ V}, T_j = 150 \text{ }^\circ\text{C}$ | -   | 24   | -   | ns   |
| $Q_{rr}$        | Reverse recovery charge       |  | -   | 23.3 | -   | nC   |
| $I_{RRM}$       | Reverse recovery current      |  | -   | 1.94 | -   | A    |

1. Pulse width limited by safe operating area
2. Pulsed: pulse duration= 300  $\mu\text{s}$ , duty cycle 1.5%

## 2.1 Electrical characteristics (curves)

Figure 2. Safe operating area

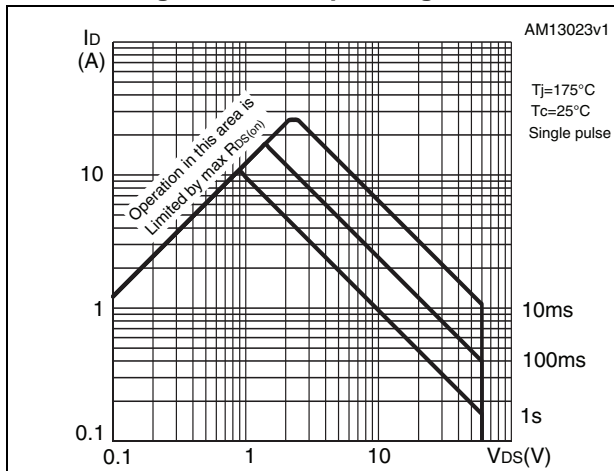


Figure 3. Thermal impedance

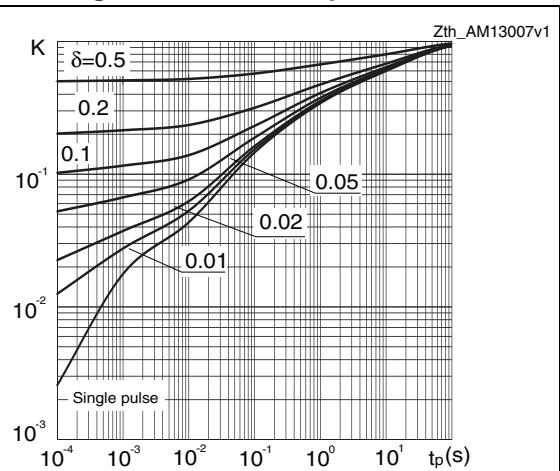


Figure 4. Output characteristics

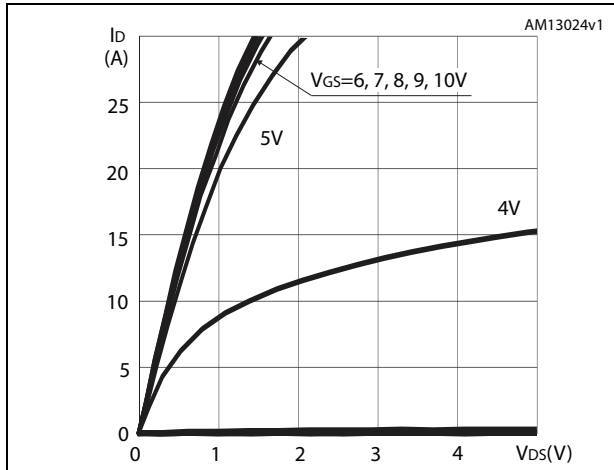


Figure 5. Transfer characteristics

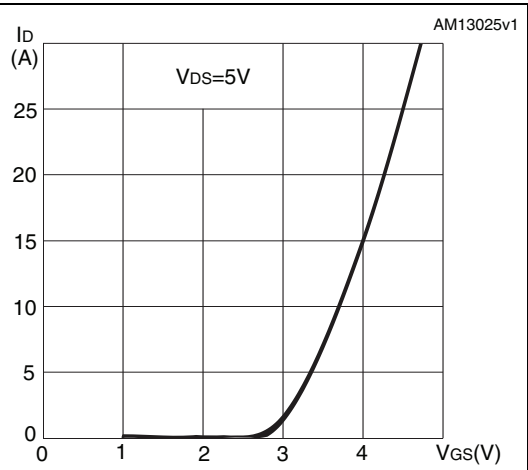


Figure 6. Normalized  $V_{(BR)DSS}$  vs temperature

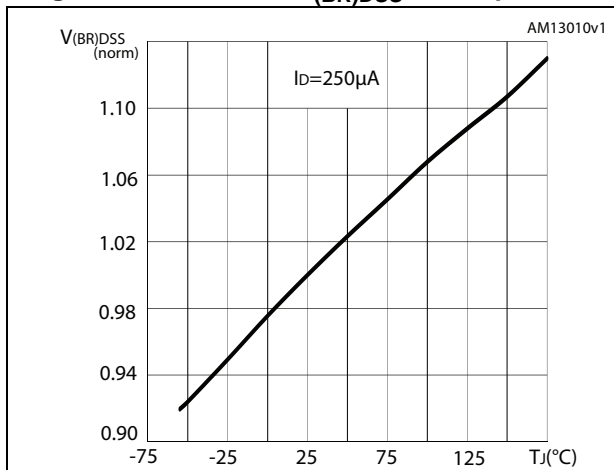


Figure 7. Static drain-source on-resistance

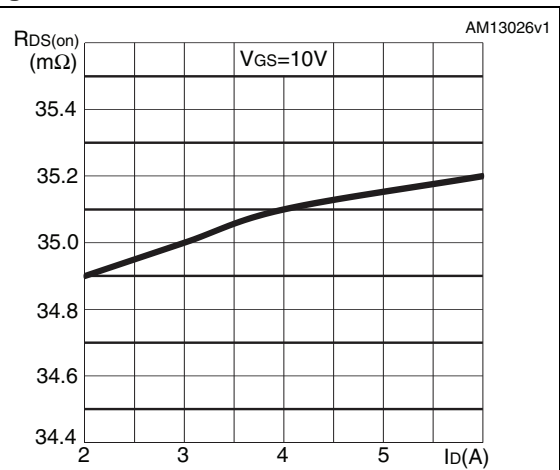


Figure 8. Gate charge vs gate-source voltage

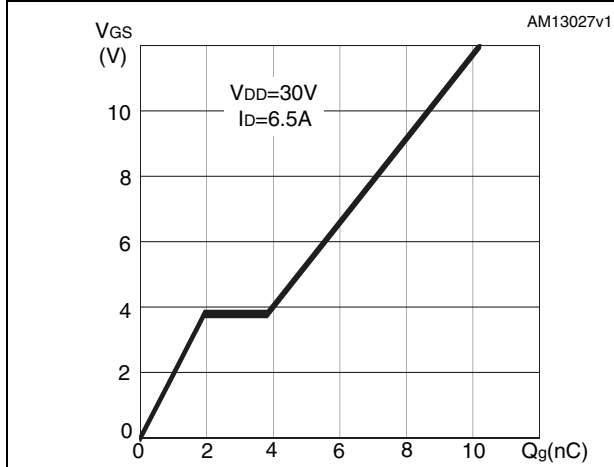


Figure 9. Capacitance variations

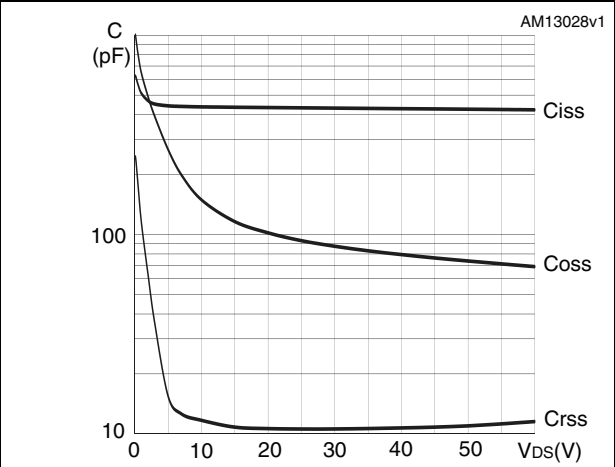


Figure 10. Normalized gate threshold voltage vs temperature

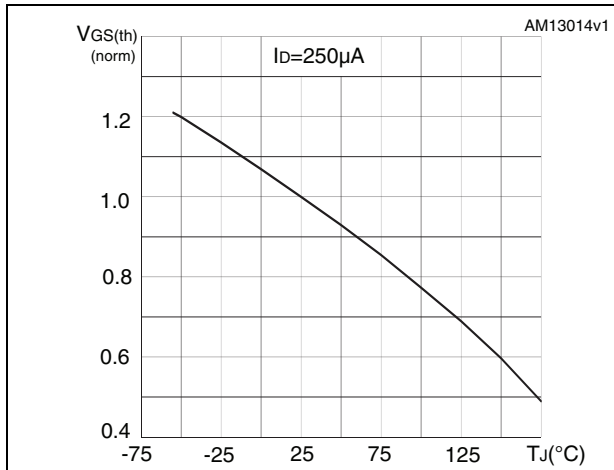
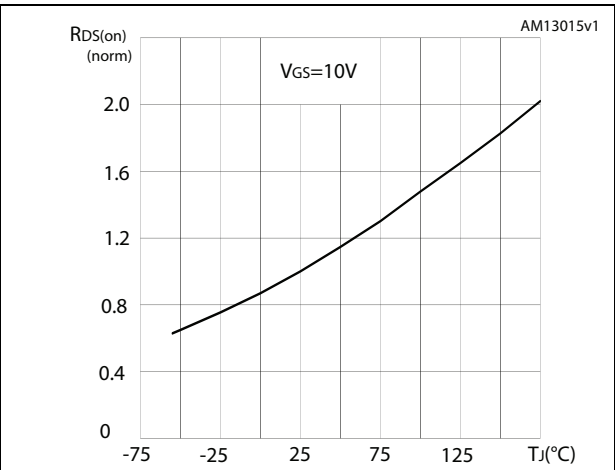
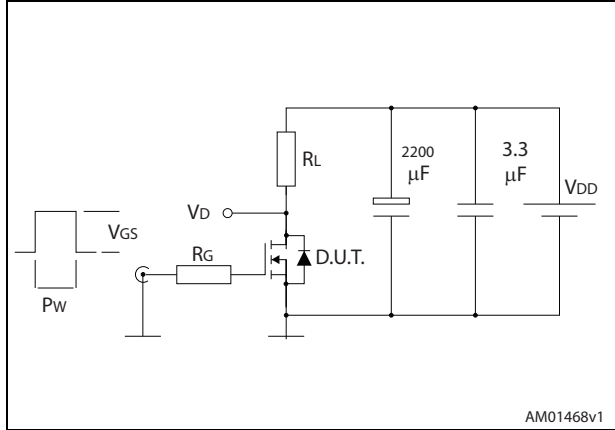


Figure 11. Normalized on-resistance vs temperature



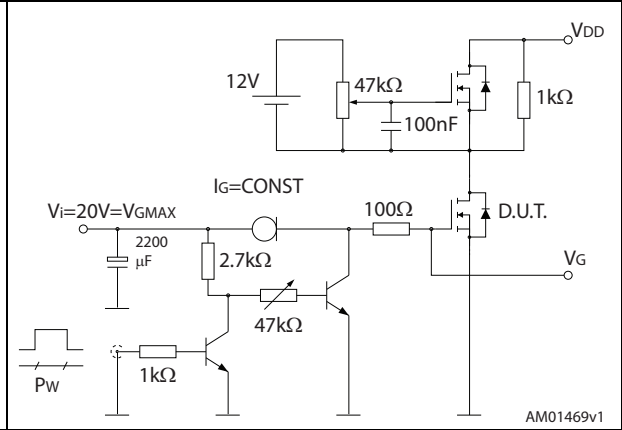
### 3 Test circuits

**Figure 12. Switching times test circuit for resistive load**



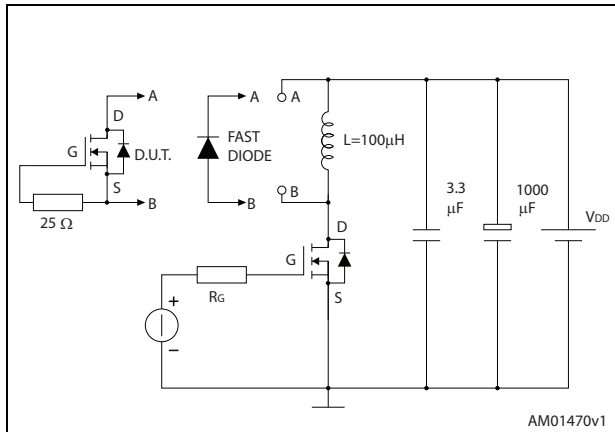
AM01468v1

**Figure 13. Gate charge test circuit**



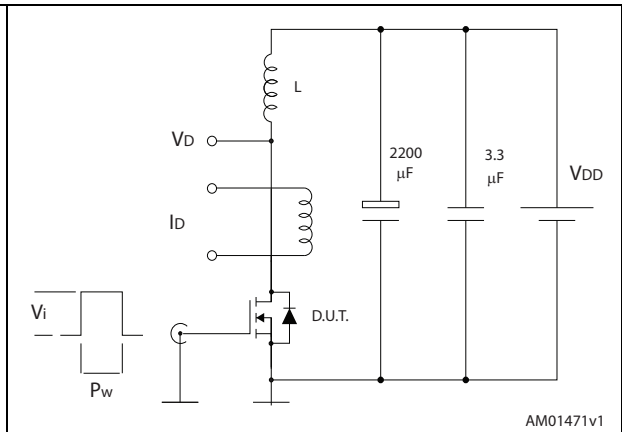
AM01469v1

**Figure 14. Test circuit for inductive load switching and diode recovery times**



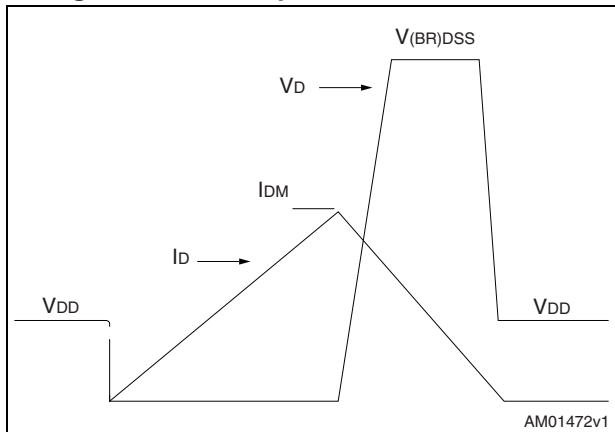
AM01470v1

**Figure 15. Unclamped inductive load test circuit**



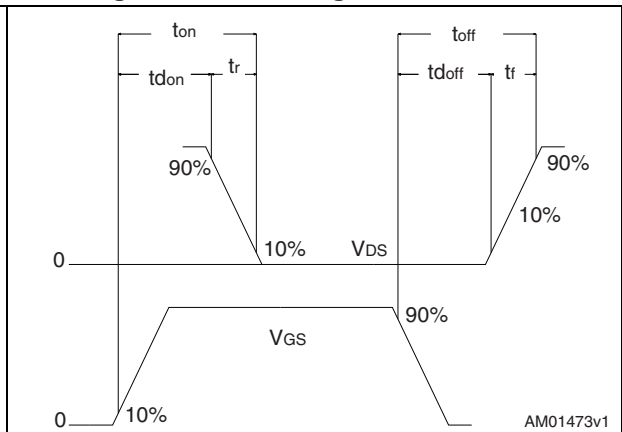
AM01471v1

**Figure 16. Unclamped inductive waveform**



AM01472v1

**Figure 17. Switching time waveform**



AM01473v1



## 4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK<sup>®</sup> packages, depending on their level of environmental compliance. ECOPACK<sup>®</sup> specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com). ECOPACK is an ST trademark.

Figure 18. PowerFLAT 5x6 double island type R outline

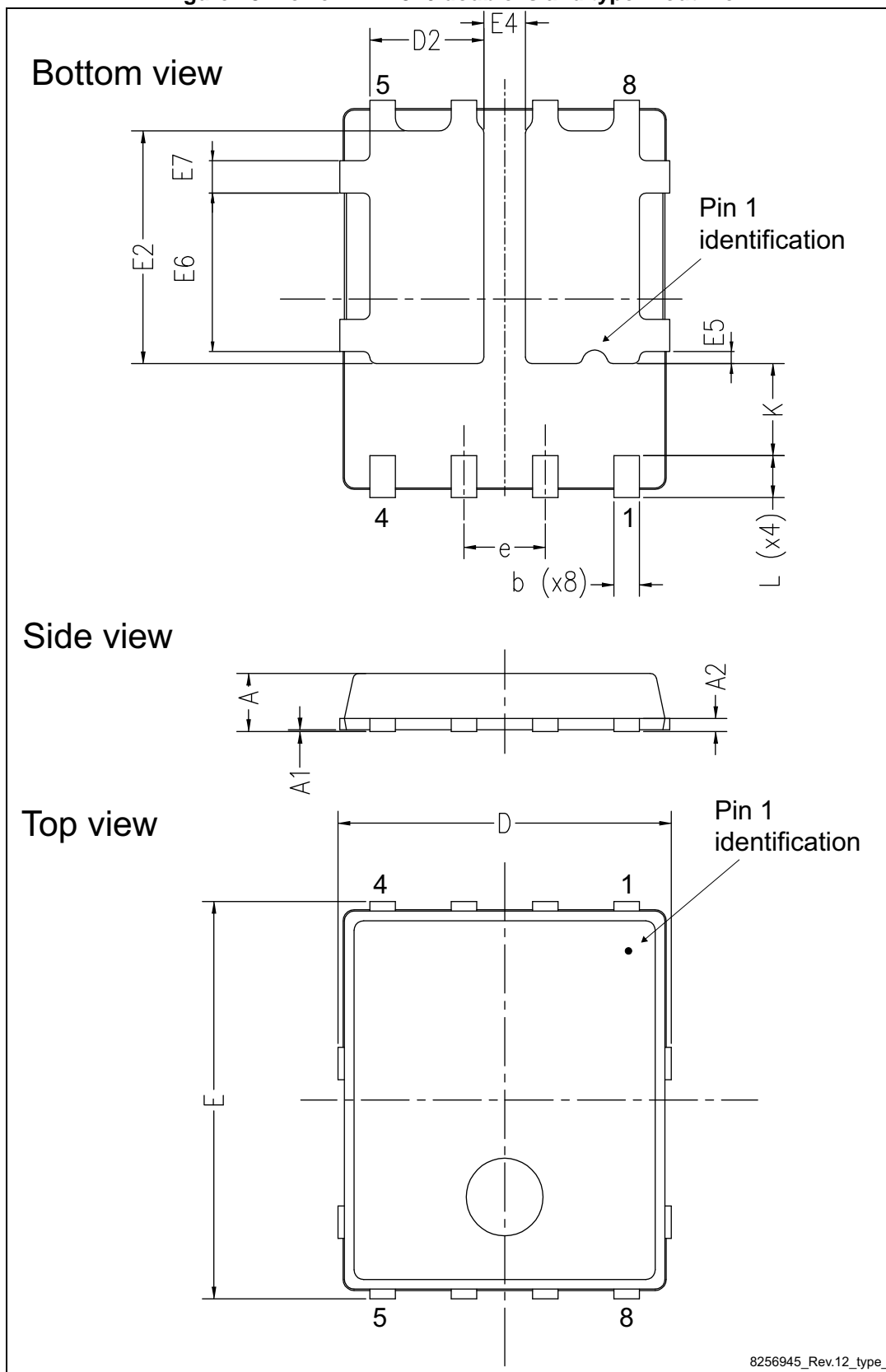


Table 8. PowerFLAT 5x6 double island type R mechanical data

| Ref. | Dimensions (mm) |      |       |
|------|-----------------|------|-------|
|      | Min.            | Typ. | Max.  |
| A    | 0.80            |      | 1.00  |
| A1   | 0.02            |      | 0.05  |
| A2   |                 | 0.25 |       |
| b    | 0.30            |      | 0.50  |
| D    | 5.00            | 5.20 | 5.40  |
| D2   | 1.68            |      | 1.88  |
| E    | 5.95            | 6.15 | 6.35  |
| E2   | 3.50            |      | 3.70  |
| E4   | 0.55            |      | 0.75  |
| E5   | 0.08            |      | 0.28  |
| E6   | 2.35            |      | 2.55  |
| E7   | 0.40            |      | 0.60  |
| e    |                 | 1.27 |       |
| L    | 0.60            |      | 0.80  |
| K    | 1.275           |      | 1.575 |

Figure 19. PowerFLAT 5x6 double island WF type R outline

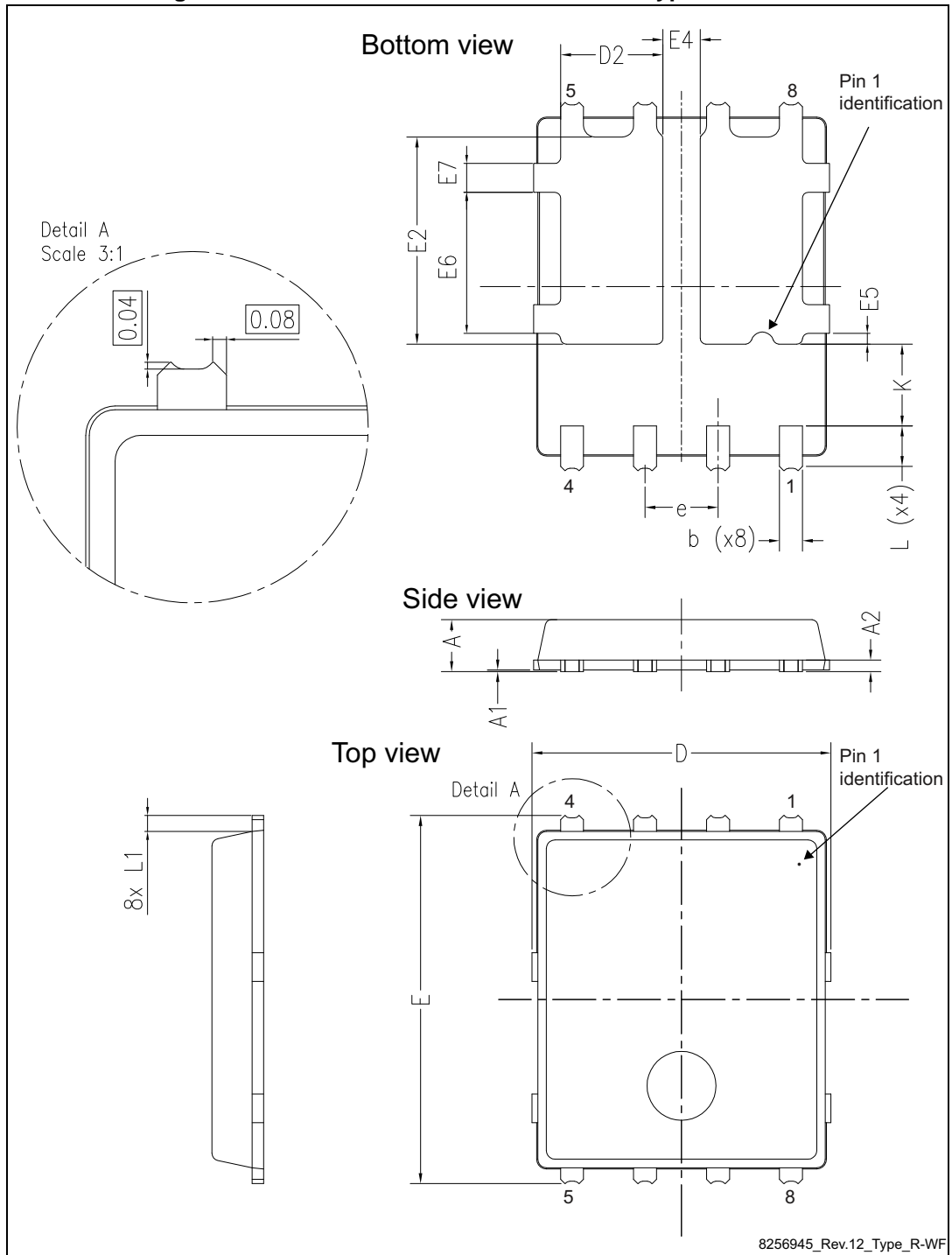
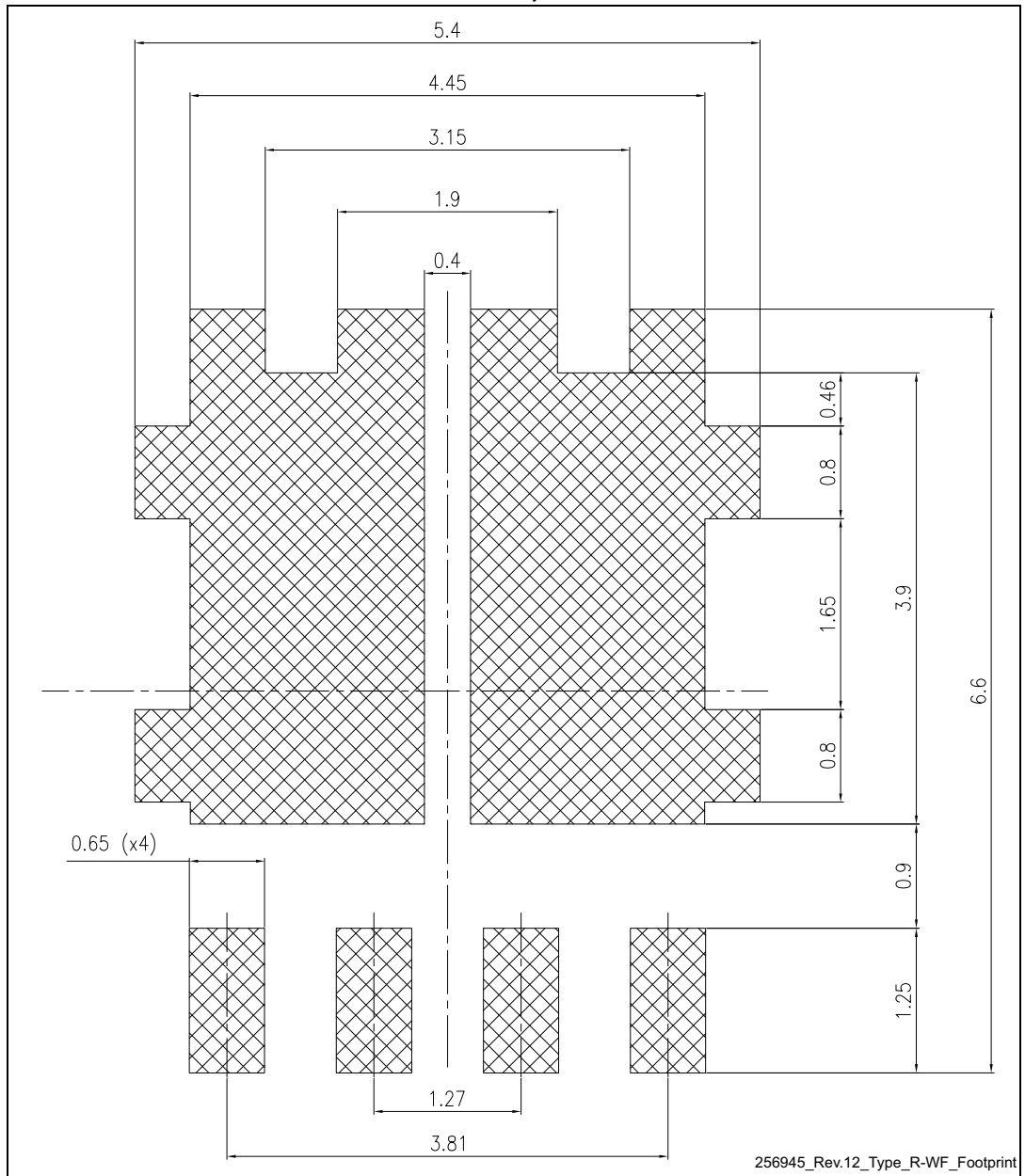


Table 9. PowerFLAT 5x6 double island WF type R mechanical data

| Ref. | Dimensions (mm) |       |       |
|------|-----------------|-------|-------|
|      | Min.            | Typ.  | Max.  |
| A    | 0.80            |       | 1.00  |
| A1   | 0.02            |       | 0.05  |
| A2   |                 | 0.25  |       |
| b    | 0.30            |       | 0.50  |
| D    | 5.00            | 5.20  | 5.40  |
| D2   | 1.68            |       | 1.88  |
| E    | 6.20            | 6.40  | 6.60  |
| E2   | 3.50            |       | 3.70  |
| E4   | 0.55            |       | 0.75  |
| E5   | 0.08            |       | 0.28  |
| E6   | 2.35            |       | 2.55  |
| E7   | 0.40            |       | 0.60  |
| e    |                 | 1.27  |       |
| L    | 0.70            |       | 0.90  |
| L1   |                 | 0.275 |       |
| K    | 1.275           |       | 1.575 |

Figure 20. PowerFLAT 5x6 double island recommended footprint (dimensions are in mm)



# 5 Packaging information

Figure 21. PowerFLAT™ 5x6 tape<sup>(a)</sup>

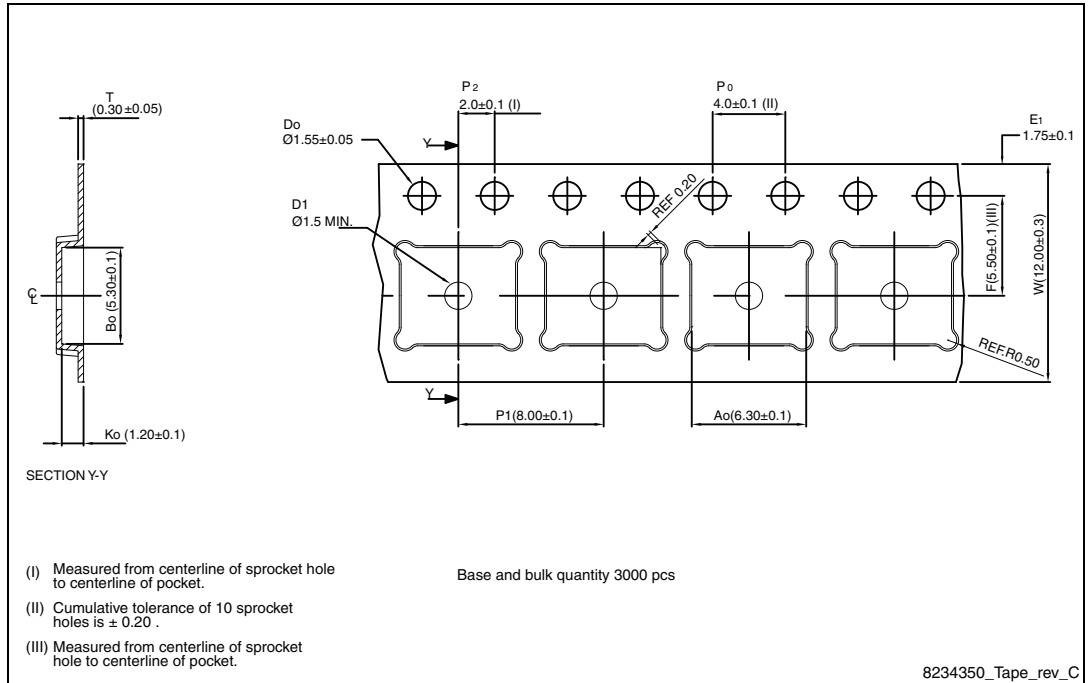
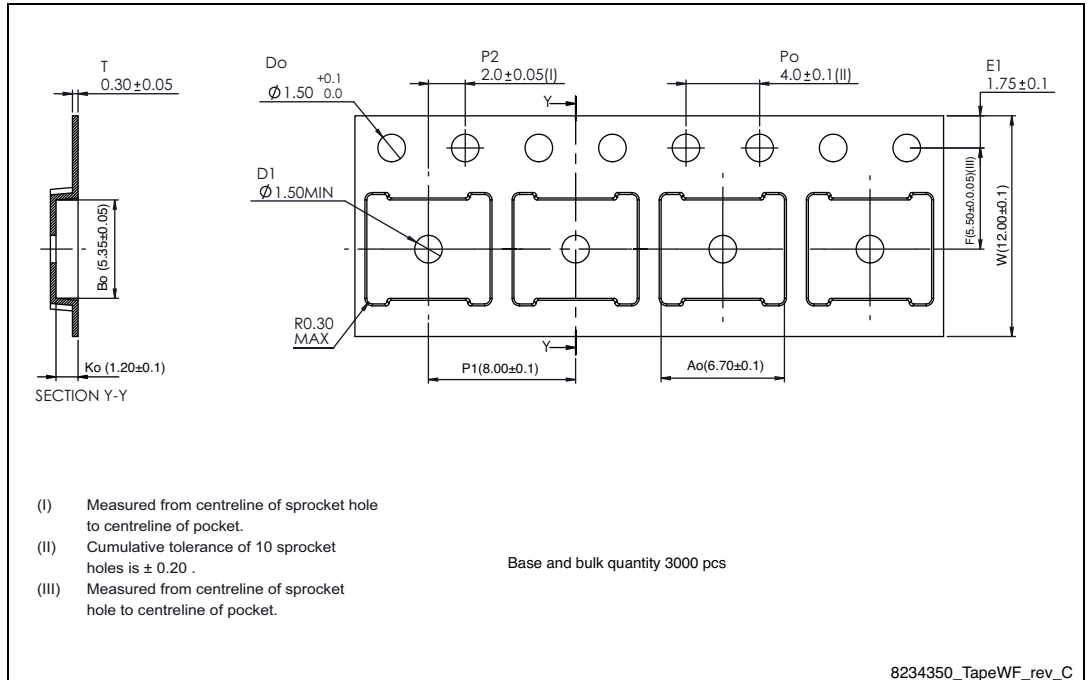


Figure 22. PowerFLAT 5x6 WF tape<sup>(a)</sup>



a. All dimensions are in millimeters.

Figure 23. PowerFLAT™ 5x6 package orientation in carrier tape

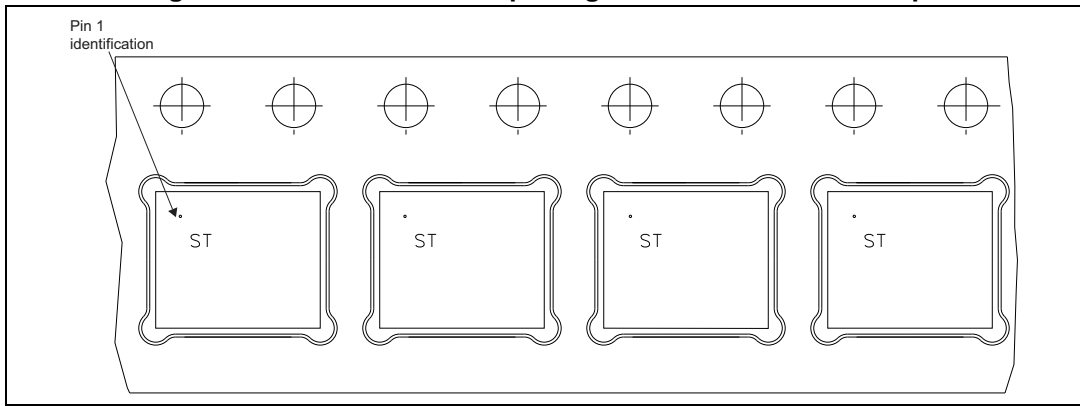
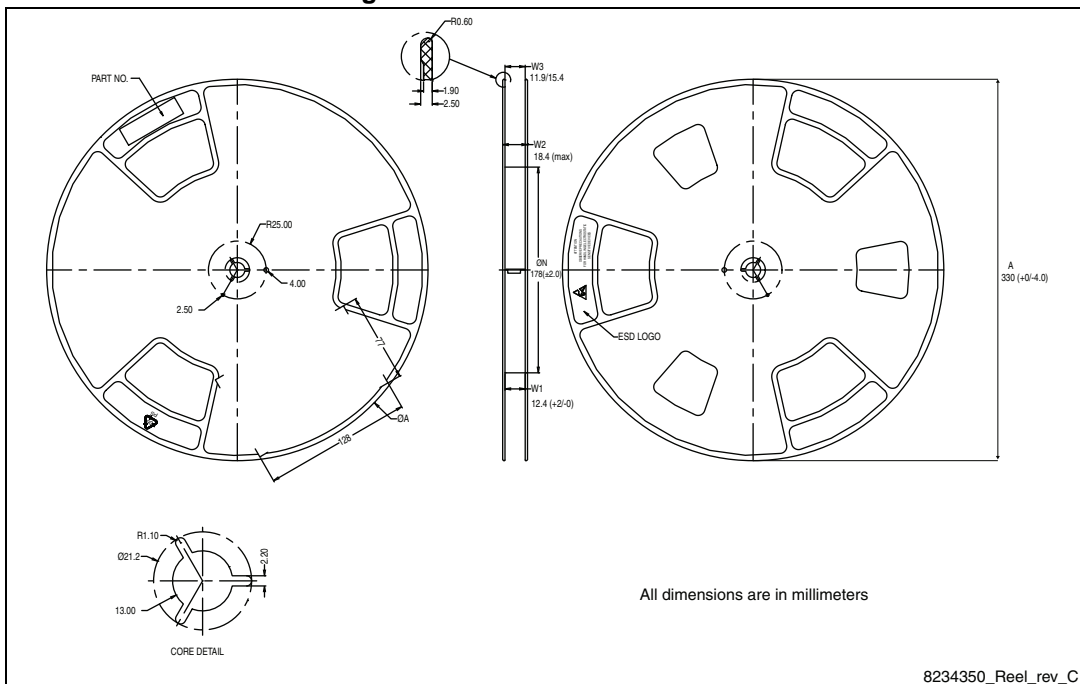


Figure 24. PowerFLAT™ 5x6 reel



8234350\_Reel\_rev\_C



## 6 Revision history

Table 10. Document revision history

| Date        | Revision | Changes   |
|-------------|----------|---|
| 28-Mar-2012 | 1        | First release.  |
| 19-Jun-2012 | 2        | <a href="#">Section 2.1: Electrical characteristics (curves)</a> has been added.<br>Updated <a href="#">Section 4: Package information</a> and tile on the coverpage.   |
| 26-Jun-2012 | 3        | Document status promoted from preliminary to production data.   |
| 23-Feb-2015 | 4        | Updated title, features and description in cover page.<br>Updated <a href="#">Table 5: Dynamic</a> , <a href="#">Table 6: Switching times</a> and <a href="#">Section 2.1: Electrical characteristics (curves)</a> .<br>Updated <a href="#">Section 4: Package information</a> .<br>Added <a href="#">Section 5: Packaging information</a> .<br>Minor text changes. |

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