

## N-channel 600 V, 0.92 $\Omega$ typ., 5 A MDmesh™ M2 Power MOSFET in a PowerFLAT™ 5x5 package

Datasheet - production data

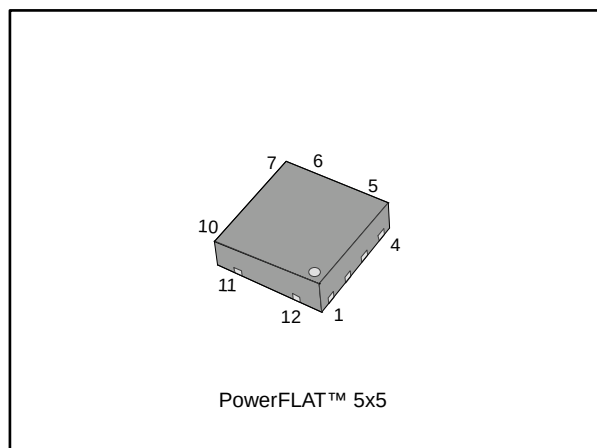
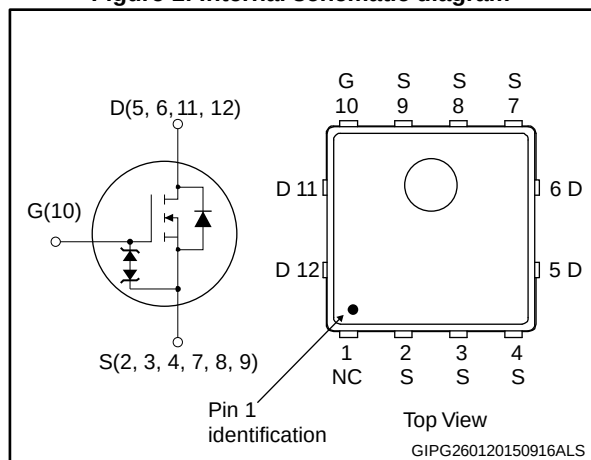


Figure 1: Internal schematic diagram



### Features

| Order code | $V_{DS} @ T_{jmax}$ | $R_{DS(on)}$ max | $I_D$ |
|------------|---------------------|------------------|-------|
| STL7N60M2  | 650 V               | 1.05 $\Omega$    | 5 A   |

- Extremely low gate charge
- Excellent output capacitance ( $C_{OSS}$ ) profile
- 100% avalanche tested
- Zener-protected

### Applications

- Switching applications

### Description

This device is an N-channel Power MOSFET developed using MDmesh™ M2 technology. Thanks to its strip layout and an improved vertical structure, the device exhibits low on-resistance and optimized switching characteristics, rendering it suitable for the most demanding high efficiency converters.

Table 1: Device summary

| Order code | Marking | Package       | Packaging     |
|------------|---------|---------------|---------------|
| STL7N60M2  | 7N60M2  | PowerFLAT 5x5 | Tape and reel |

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## Contents

|          |                                              |           |
|----------|----------------------------------------------|-----------|
| <b>1</b> | <b>Electrical ratings .....</b>              | <b>3</b>  |
| <b>2</b> | <b>Electrical characteristics .....</b>      | <b>4</b>  |
|          | 2.2 Electrical characteristics (curves)..... | 6         |
| <b>3</b> | <b>Test circuits .....</b>                   | <b>8</b>  |
| <b>4</b> | <b>Package mechanical data .....</b>         | <b>9</b>  |
|          | 4.1 Package mechanical data .....            | 10        |
| <b>5</b> | <b>Revision history .....</b>                | <b>12</b> |

# 1 Electrical ratings

Table 2: Absolute maximum ratings

| Symbol            | Parameter                                               | Value       | Unit |
|-------------------|---------------------------------------------------------|-------------|------|
| $V_{GS}$          | Gate-source voltage                                     | $\pm 25$    | V    |
| $I_D$             | Drain current (continuous) at $T_C = 25\text{ °C}$      | 5           | A    |
| $I_D$             | Drain current (continuous) at $T_C = 100\text{ °C}$     | 3.2         | A    |
| $I_{DM}^{(1)}$    | Drain current (pulsed)                                  | 20          | A    |
| $I_D^{(2)}$       | Drain current (continuous) at $T_{pcb} = 25\text{ °C}$  | 1.2         | A    |
| $I_D^{(2)}$       | Drain current (continuous) at $T_{pcb} = 100\text{ °C}$ | 0.8         | A    |
| $I_{DM}^{(1)(2)}$ | Drain current (pulsed)                                  | 4.8         | A    |
| $P_{TOT}$         | Total dissipation at $T_C = 25\text{ °C}$               | 67          | W    |
| $P_{TOT}^{(2)}$   | Total dissipation at $T_{pcb} = 25\text{ °C}$           | 4           | W    |
| $dv/dt^{(3)}$     | Peak diode recovery voltage slope                       | 15          | V/ns |
| $dv/dt^{(4)}$     | MOSFET $dv/dt$ ruggedness                               | 50          | V/ns |
| $T_{stg}$         | Storage temperature                                     | - 55 to 150 | °C   |
| $T_j$             | Max. operating junction temperature                     | 150         | °C   |

## Notes:

<sup>(1)</sup>Pulse width limited by safe operating area.

<sup>(2)</sup>When mounted on FR-4 Board of 1 inch<sup>2</sup>, 2 oz Cu ( $t < 10\text{ s}$ )

<sup>(3)</sup> $I_{SD} \leq 5\text{ A}$ ,  $di/dt \leq 400\text{ A}/\mu\text{s}$ ;  $V_{DS\text{ peak}} < V_{(BR)DSS}$ ,  $V_{DD} = 400\text{ V}$ .

<sup>(4)</sup> $V_{DS} \leq 480\text{ V}$

Table 3: Thermal data

| Symbol         | Parameter                            | Value | Unit |
|----------------|--------------------------------------|-------|------|
| $R_{thj-case}$ | Thermal resistance junction-case max | 0.83  | °C/W |
| $R_{thj-pcb}$  | Thermal resistance junction-pcb max  | 31.3  | °C/W |

Table 4: Avalanche characteristics

| Symbol   | Parameter                                                                                                | Value | Unit |
|----------|----------------------------------------------------------------------------------------------------------|-------|------|
| $I_{AR}$ | Avalanche current, repetitive or not repetitive (pulse width limited by $T_{jmax}$ )                     | 1     | A    |
| $E_{AS}$ | Single pulse avalanche energy (starting $T_j = 25\text{ °C}$ , $I_D = I_{AR}$ ; $V_{DD} = 50\text{ V}$ ) | 80    | mJ   |

## 2 Electrical characteristics

$T_C = 25\text{ }^{\circ}\text{C}$  unless otherwise specified

**Table 5: On/off states**

| Symbol        | Parameter                         | Test conditions                                                                          | Min. | Typ. | Max.     | Unit          |
|---------------|-----------------------------------|------------------------------------------------------------------------------------------|------|------|----------|---------------|
| $V_{(BR)DSS}$ | Drain-source breakdown voltage    | $V_{GS} = 0\text{ V}$ , $I_D = 1\text{ mA}$                                              | 600  |      |          | V             |
| $I_{DSS}$     | Zero gate voltage Drain current   | $V_{GS} = 0\text{ V}$ , $V_{DS} = 600\text{ V}$                                          |      |      | 1        | $\mu\text{A}$ |
|               |                                   | $V_{GS} = 0\text{ V}$ , $V_{DS} = 600\text{ V}$ ,<br>$T_C = 125\text{ }^{\circ}\text{C}$ |      |      | 100      | $\mu\text{A}$ |
| $I_{GSS}$     | Gate-body leakage current         | $V_{DS} = 0\text{ V}$ , $V_{GS} = \pm 25\text{ V}$                                       |      |      | $\pm 10$ | $\mu\text{A}$ |
| $V_{GS(th)}$  | Gate threshold voltage            | $V_{DS} = V_{GS}$ , $I_D = 250\text{ }\mu\text{A}$                                       | 2    | 3    | 4        | V             |
| $R_{DS(on)}$  | Static drain-source on-resistance | $V_{GS} = 10\text{ V}$ , $I_D = 2\text{ A}$                                              |      | 0.92 | 1.05     | $\Omega$      |

**Table 6: Dynamic**

| Symbol                     | Parameter                     | Test conditions                                                                                                                       | Min. | Typ. | Max. | Unit     |
|----------------------------|-------------------------------|---------------------------------------------------------------------------------------------------------------------------------------|------|------|------|----------|
| $C_{ISS}$                  | Input capacitance             | $V_{DS} = 100\text{ V}$ , $f = 1\text{ MHz}$ ,<br>$V_{GS} = 0\text{ V}$                                                               | -    | 271  | -    | pF       |
| $C_{OSS}$                  | Output capacitance            |                                                                                                                                       | -    | 15.7 | -    | pF       |
| $C_{RSS}$                  | Reverse transfer capacitance  |                                                                                                                                       | -    | 0.68 | -    | pF       |
| $C_{OSS\text{ eq.}}^{(1)}$ | Equivalent output capacitance | $V_{DS} = 0\text{ to }480\text{ V}$ , $V_{GS} = 0\text{ V}$                                                                           | -    | 75.5 | -    | pF       |
| $R_G$                      | Intrinsic gate resistance     | $f = 1\text{ MHz}$ , $I_D = 0\text{ A}$                                                                                               | -    | 7.2  | -    | $\Omega$ |
| $Q_g$                      | Total gate charge             | $V_{DD} = 480\text{ V}$ , $I_D = 5\text{ A}$ , $V_{GS} = 10\text{ V}$<br>(see <a href="#">Figure 15: "Gate charge test circuit"</a> ) | -    | 8.8  | -    | nC       |
| $Q_{gs}$                   | Gate-source charge            |                                                                                                                                       | -    | 1.8  | -    | nC       |
| $Q_{gd}$                   | Gate-drain charge             |                                                                                                                                       | -    | 4.3  | -    | nC       |

**Notes:**

<sup>(1)</sup> $C_{OSS\text{ eq.}}$  is defined as a constant equivalent capacitance giving the same charging time as  $C_{OSS}$  when  $V_{DS}$  increases from 0 to 80%  $V_{DSS}$

**Table 7: Switching times**

| Symbol       | Parameter           | Test conditions                                                                                                                                                                                                                                      | Min. | Typ. | Max. | Unit |
|--------------|---------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------|------|------|------|
| $t_{d(on)}$  | Turn-on delay time  | $V_{DD} = 300\text{ V}$ , $I_D = 2.5\text{ A}$<br>$R_G = 4.7\text{ }\Omega$ , $V_{GS} = 10\text{ V}$<br>(see <a href="#">Figure 14: "Switching times test circuit for resistive load"</a> and <a href="#">Figure 19: "Switching time waveform"</a> ) | -    | 7.6  | -    | ns   |
| $t_r$        | Rise time           |                                                                                                                                                                                                                                                      | -    | 7.2  | -    | ns   |
| $t_{d(off)}$ | Turn-off-delay time |                                                                                                                                                                                                                                                      | -    | 19.3 | -    | ns   |
| $t_f$        | Fall time           |                                                                                                                                                                                                                                                      | -    | 15.9 | -    | ns   |

Table 8: Source drain diode

| Symbol          | Parameter                     | Test conditions                                                                                                                                                                               | Min. | Typ. | Max. | Unit          |
|-----------------|-------------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------|------|------|---------------|
| $I_{SD}$        | Source-drain current          |                                                                                                                                                                                               | -    |      | 5    | A             |
| $I_{SDM}^{(1)}$ | Source-drain current (pulsed) |                                                                                                                                                                                               | -    |      | 20   | A             |
| $V_{SD}^{(2)}$  | Forward on voltage            | $V_{GS} = 0 \text{ V}$ , $I_{SD} = 5 \text{ A}$                                                                                                                                               | -    |      | 1.6  | V             |
| $t_{rr}$        | Reverse recovery time         | $I_{SD} = 5 \text{ A}$ , $di/dt = 100 \text{ A}/\mu\text{s}$ ,<br>$V_{DD} = 60 \text{ V}$ (see <a href="#">Figure 19: "Switching time waveform"</a> )                                         | -    | 275  |      | ns            |
| $Q_{rr}$        | Reverse recovery charge       |                                                                                                                                                                                               | -    | 1.55 |      | $\mu\text{C}$ |
| $I_{RRM}$       | Reverse recovery current      |                                                                                                                                                                                               | -    | 11   |      | A             |
| $t_{rr}$        | Reverse recovery time         | $I_{SD} = 5 \text{ A}$ , $di/dt = 100 \text{ A}/\mu\text{s}$ ,<br>$V_{DD} = 60 \text{ V}$ , $T_J = 150 \text{ }^\circ\text{C}$<br>(see <a href="#">Figure 19: "Switching time waveform"</a> ) | -    | 376  |      | ns            |
| $Q_{rr}$        | Reverse recovery charge       |                                                                                                                                                                                               | -    | 2.1  |      | $\mu\text{C}$ |
| $I_{RRM}$       | Reverse recovery current      |                                                                                                                                                                                               | -    | 11   |      | A             |

**Notes:**

<sup>(1)</sup> Pulse width is limited by safe operating area

<sup>(2)</sup> Pulsed: pulse duration = 300  $\mu\text{s}$ , duty cycle 1.5%

## 2.2 Electrical characteristics (curves)

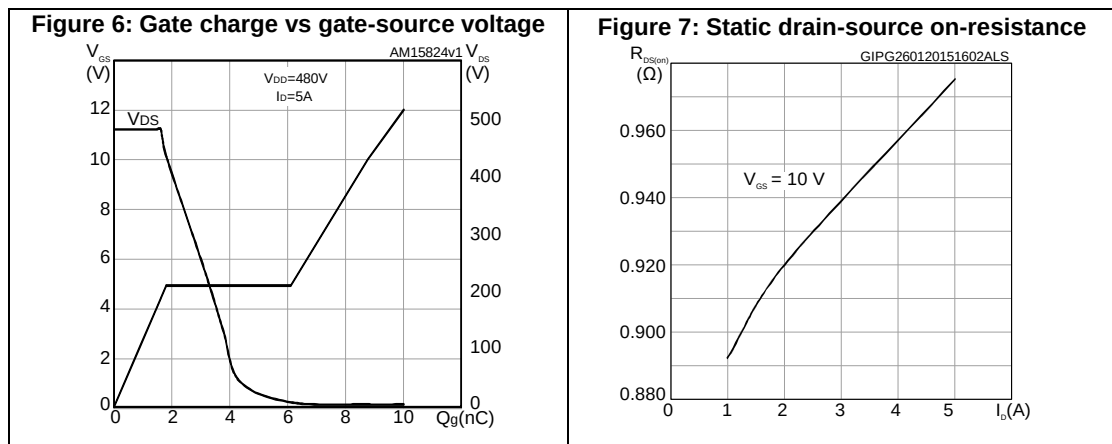
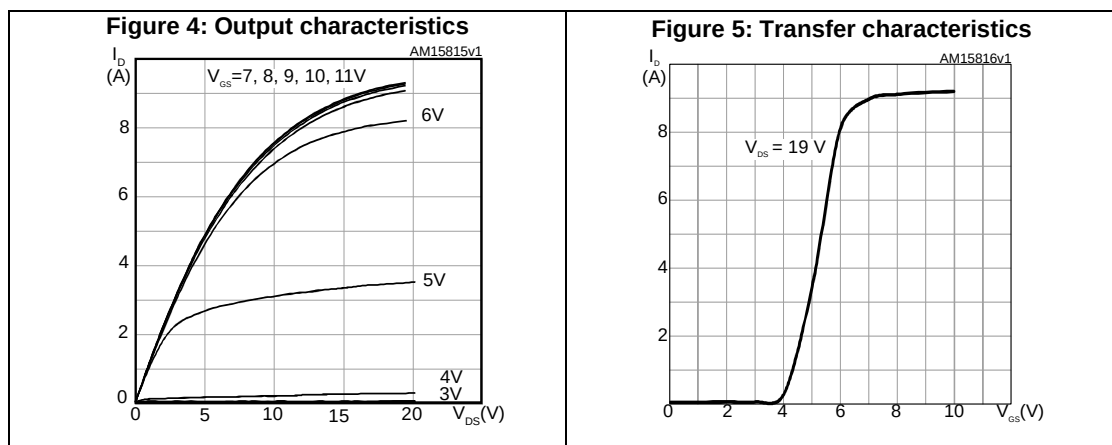
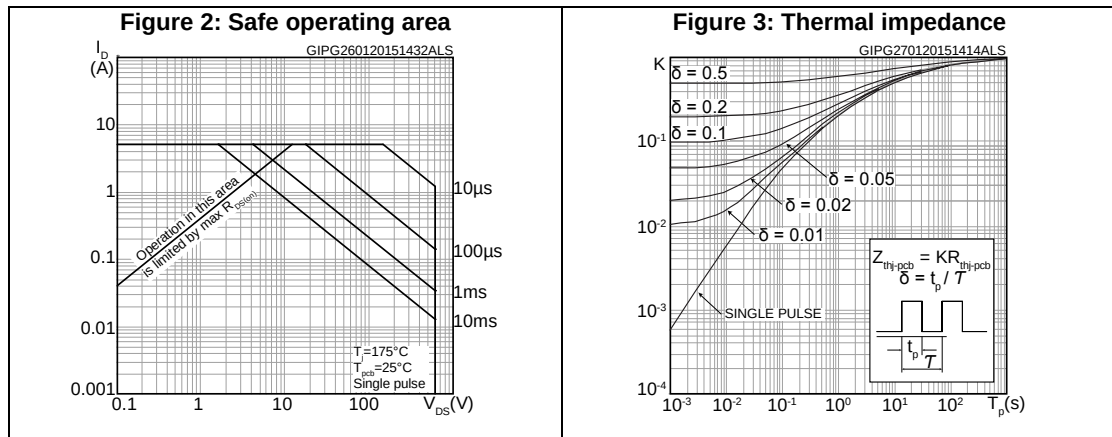


Figure 8: Capacitance variations

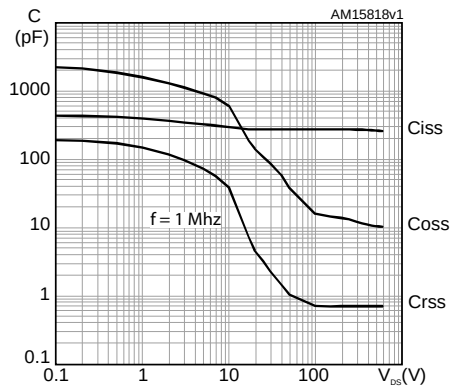


Figure 9: Output capacitance stored energy

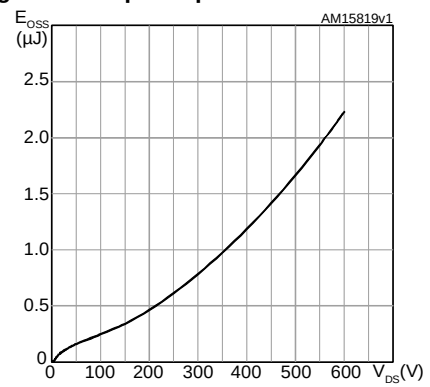


Figure 10: Normalized gate threshold voltage vs temperature

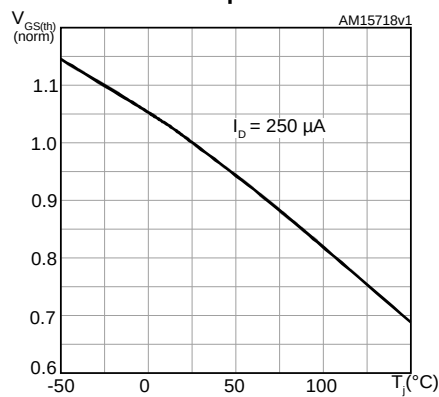


Figure 11: Normalized on-resistance vs temperature

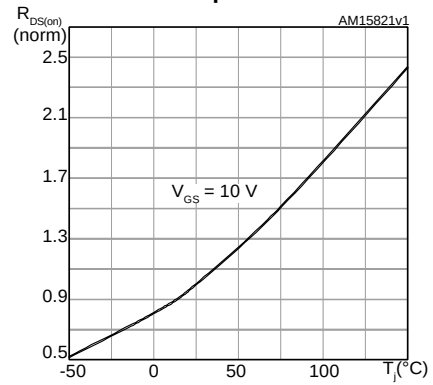


Figure 12: Source-drain diode forward characteristics

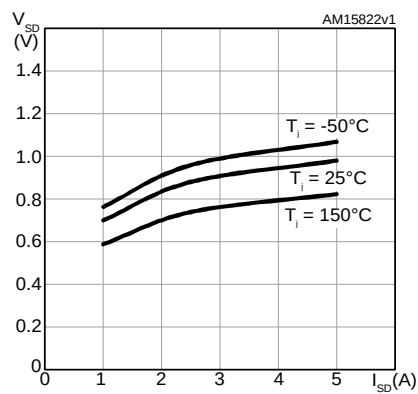
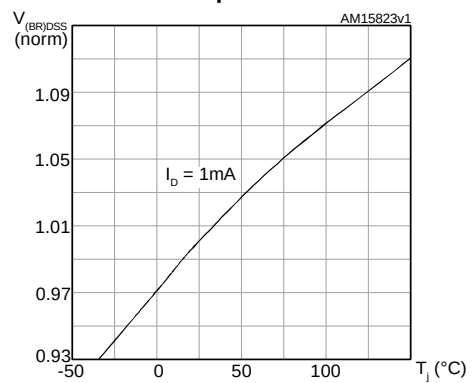
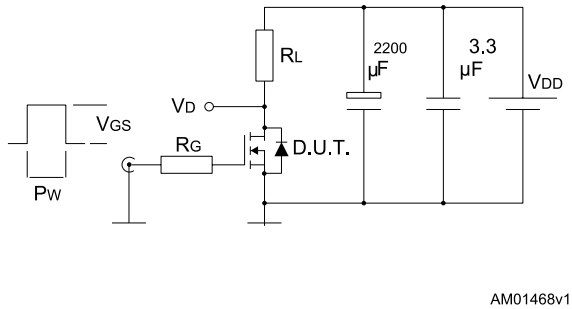


Figure 13: Normalized V(BR)DSS vs temperature

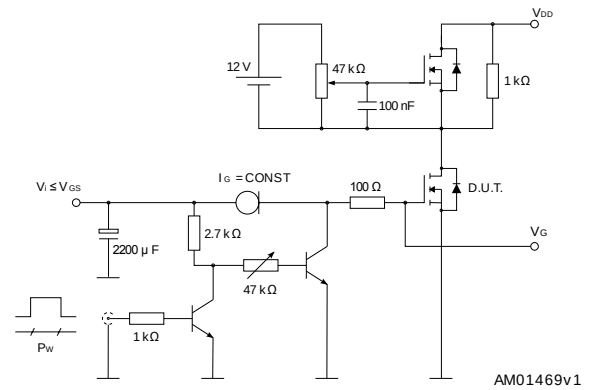


### 3 Test circuits

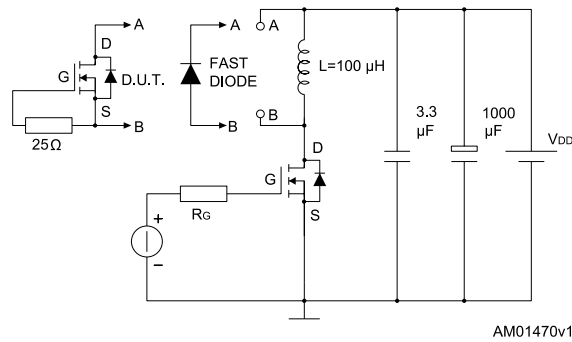
**Figure 14: Switching times test circuit for resistive load**



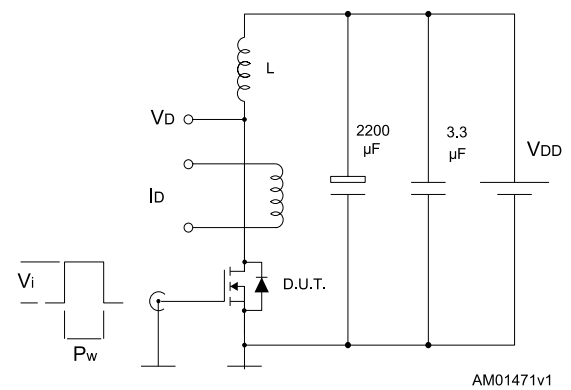
**Figure 15: Gate charge test circuit**



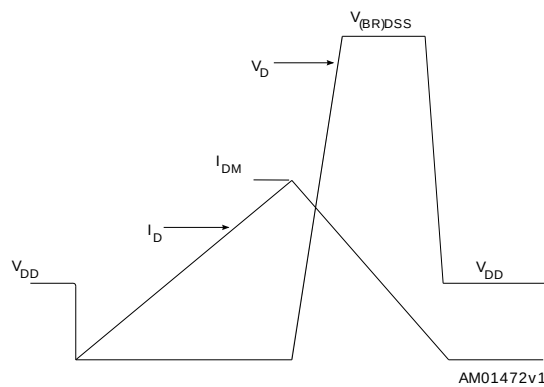
**Figure 16: Test circuit for inductive load switching and diode recovery times**



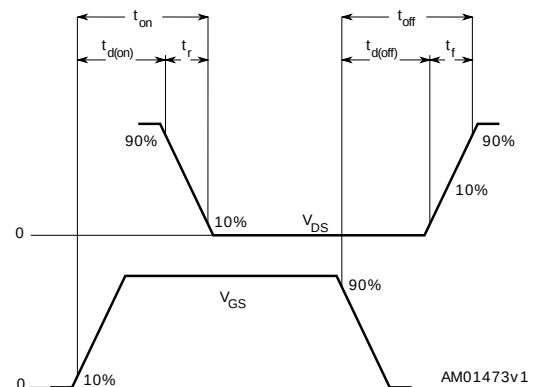
**Figure 17: Unclamped inductive load test circuit**



**Figure 18: Unclamped inductive waveform**



**Figure 19: Switching time waveform**





## 4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK<sup>®</sup> packages, depending on their level of environmental compliance. ECOPACK<sup>®</sup> specifications, grade definitions and product status are available at: **[www.st.com](http://www.st.com)**. ECOPACK<sup>®</sup> is an ST trademark.

## 4.1 Package mechanical data

Figure 20: PowerFLAT™ 5x5 drawings

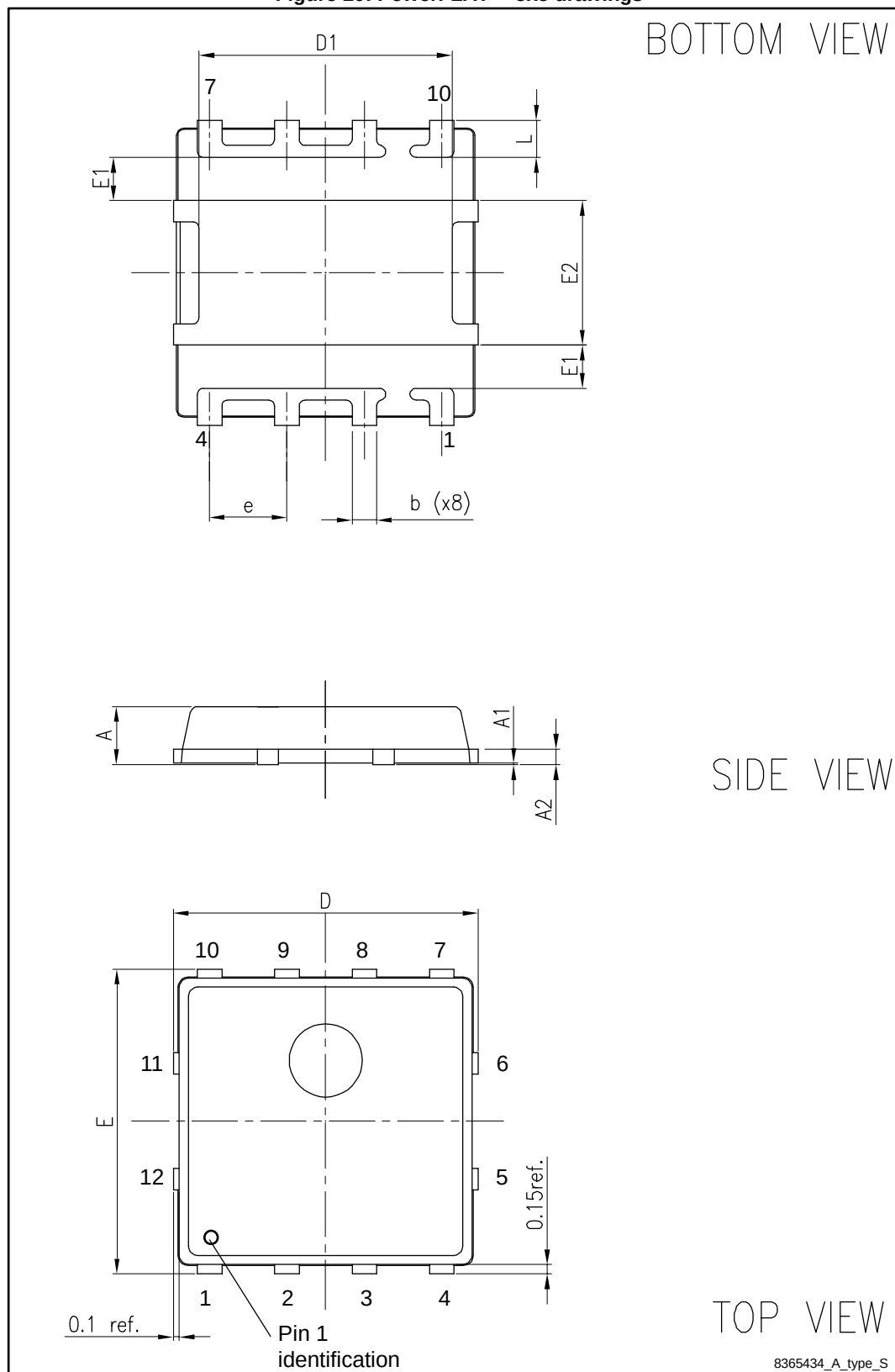
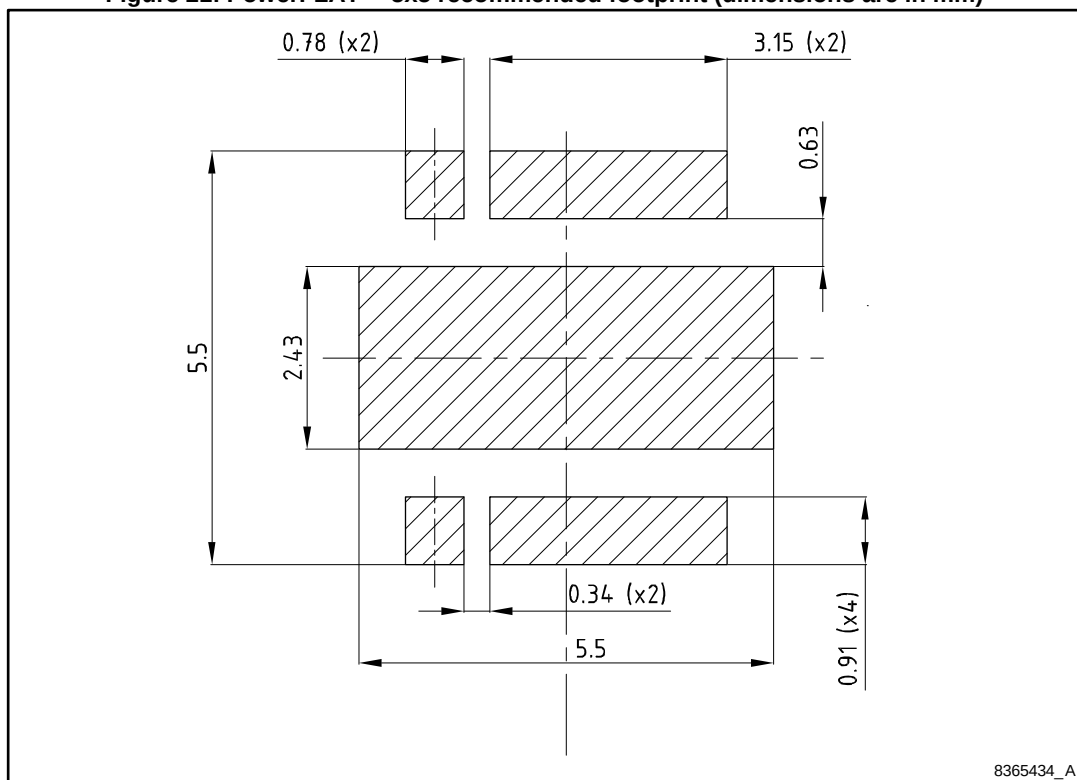


Table 9: PowerFLAT 5x5 mechanical data

| Dim. | mm   |      |      |
|------|------|------|------|
|      | Min. | Typ. | Max. |
| A    | 0.80 |      | 1.0  |
| A1   | 0.02 |      | 0.05 |
| A2   |      | 0.25 |      |
| b    | 0.30 |      | 0.50 |
| D    |      | 5.00 |      |
| D1   | 4.05 |      | 4.25 |
| E    |      | 5.00 |      |
| E1   | 0.64 |      | 0.79 |
| E2   | 2.25 |      | 2.45 |
| e    |      | 1.27 |      |
| L    | 0.45 |      | 0.75 |

Figure 21: PowerFLAT™ 5x5 recommended footprint (dimensions are in mm)



## 5 Revision history

Table 10: Document revision history

| Date        | Revision | Changes        |
|-------------|----------|----------------|
| 26-Jan-2015 | 1        | First release. |

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